HEWLETT PACKARD

HP 1630A/D/G and HP 1631A/D Logic Analyzers

HEWLETT PACKARD

SERVICE MANUAL

HP 1630A/D/G and HP 1631A/D LOGIC ANALYZERS

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed:

1630A; 2812A
1630D; 2812A
1630G; 2812A
1631A; 2811A
1631D; 2811A

With changes described within, this manual also applies to instruments with serial prefixes:

1630A; 2242A through 2715A
1630D; 2234A through 2720A
1630G; 2415A through 2602A
1631A; 2451A through 2714A
1631D; 2446A through 2713A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

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CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

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For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

The product related to this manual is no longer in production at Hewlett Packard Co. As a service to our customers, we are supplying you with a photocopy of the original document.

SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

TABLE OF CONTENTS

Section		Page
I.	**GENERAL INFORMATION**	1-1
1-1.	Introduction	1-1
1-2.	Manual Organization	1-1
1-3.	Instruments Covered By This Manual	1-2
1-4.	Description	1-2
1-5.	Accessories Supplied	1-3
1-6.	Specifications	1-4
1-7.	Recommended Test Equipment	1-7
II.	**INSTALLATION**	2-1
2-1.	Introduction	2-1
2-2.	Preparation For Use	2-1
2-3.	Power Requirements	2-1
2-4.	Line Voltage Selection	2-1
2-5.	Power Cable	2-1
2-6.	Operating Environment	2-2
2-7.	Cleaning Requirements	2-2
2-8.	Storage and Shipment	2-2
2-9.	Environment	2-2
2-10.	Packaging	2-2
2-11.	Tagging For Service	2-2
2-12.	Original Packaging	2-2
2-13.	Other Packaging	2-2
III.	**OPERATION**	3-1
3-1.	Introduction	3-1
IV.	**CONFIDENCE TESTS**	4-1
4-1.	Introduction	4-1
4-2.	Equipment Required	4-1
4-3.	Self Test Function Verification	4-1
4-4.	Initiating 1630/1631 Self Test (ST)	4-1
4-5.	Self Test RAM Test Procedure	4-2
4-6.	Self Test ROM Test Procedure	4-3
4-7.	Self Test Acquisition Test Procedure	4-4
4-8.	1631A/D Analog Acquisition Self Test	4-9
4-9.	1630G Internal Storage Test and Reset	4-12

TABLE OF CONTENTS (Cont'd)

Section		Page
V.	**ADJUSTMENTS**	5-1
5-1.	Introduction	5-1
5-2.	Equipment Required	5-1
5-3.	Power Supply Adjustment	5-1
5-4.	CPU Adjustment	5-2
5-5.	Display System Adjustments	5-2
5-6.	Timing Master Adjustment (200 MHz Oscillator)	5-7
5-7.	State Master Board Adjustment	5-8
5-8.	State Slave Board Adjustment	5-9
5-9.	Analog Board Adjustment	5-9
5-10.	DAC Zero Adjustment	5-9
5-11.	Skew Adjustment	5-9
VI.	**REPLACEABLE PARTS**	6-1
6-1.	Introduction	6-1
6-2.	Abbreviations	6-1
6-3.	Parts List	6-1
6-4.	Ordering Information	6-1
6-5.	Direct Mail Order System	6-1
VI.	**INSTRUMENT CHANGES**	7-1
7-1.	Introduction	7-1
7-2.	Manual Changes	7-1
7-3.	HP 1630A/D/G, 1631A/D Instrument Changes	7-1
7-4.	Instrument Family History	7-4

TABLE OF CONTENTS (Cont'd)

Section — Page

VIII. SERVICE 8-1

8-1. Introduction 8-1
8-2. Safety Considerations 8-1
8-3. Block Diagram Theory 8-2
8-4. Logic Convention 8-4
8-5. ECL Attributes 8-4
8-6. Removal and Installation of Mainframe Components 8-9
8-7. Acquisition Board Removal (State and Timing) 8-9
8-8. CPU Board Removal 8-9
8-9. Power Supply Board Removal 8-10
8-10. Motherboard Removal 8-10
8-11. Keyboard Removal 8-17
8-12. CRT Removal 8-17
8-13. Display Driver Removal 8-18
8-14. Analog Board Removal 8-22

NOTE

Service and circuit information for the individual assemblies is located in separate sections. Tables of Contents for each section are located at the front of the section. The sections are divided as follows:

SECTION	ASSEMBLY
8A	A1 Power Supply and A2 Motherboard
8B	A3 CPU, A6 Display, and A7 Keyboard
8C	A4 State Master
8D	A5 Timing Master
8E	A8 Timing Slave (1630D and 1631D Only)
8F	A11 State Slave (1630G Only)
8G	A13 Analog (1631A/D Only)

APPENDIXES

The appendixes provide additional information for instrument service. A Table of Contents is provided at the front of each appendix.

Appendix A — 1630A/D/G, 1631A/D Repair and Verification Procedures

Appendix B — 1630A/D/G, 1631A/D Special Case Node Testing

Appendix C — 1631A/D Analog Acquisition Performance Tests

LIST OF ILLUSTRATIONS

Figure		Page
2-1.	Power Cord Configurations	2-1
3-1.	Front Panel Controls	3-1
3-2.	HP-IB System Configuration	3-2
3-3.	HP-IL System Configuration	3-2
5-1.	Yoke Centering Adjustment	5-3
5-2.	Display Adjustment Locations	5-5
5-3.	Display Size Test Pattern	5-5
5-4.	Display Brightness Test Pattern	5-6
5-5.	Strobe Signals	5-8
6-1.	Mainframe Mechanical Parts Locations	6-5
8-1.	System Block Diagram	8-3

LIST OF TABLES

Table		Page
1-1.	Specifications	1-4
1-2.	Supplemental Characteristics	1-6
1-3.	Recommended Test Equipment	1-7
4-1.	1630A/D, 1631A/D Error Message Interpretation	4-6
4-2.	1630G Error Message Interpretation	4-7
4-3.	Earlier 1630A/D Error Message Interpretation	4-8
6-1.	Reference Designators and Abbreviations	6-3
6-2.	Replaceable Parts List	6-9
6-3.	List of Manufacturers' Codes	6-50
7-1.	Board Complements vs. Serial Prefixes	7-2
7-2.	Part Changes Quick-reference Table	7-3
8-1.	Logic Symbols	8-5
8-2.	Schematic Diagram Notes	8-8

SECTION I
GENERAL INFORMATION

WARNING

The information in this manual is for the use of trained service personnel. To avoid electrical shock, do not perform any procedures in the manual or do any servicing to the logic analyzer unless you are qualified.

1-1. INTRODUCTION

This manual contains technical information concerning the installation, operation, maintenance, and servicing of the HP 1630A/D/G and HP 1631A/D Logic Analyzers. Information refers to all logic analyzers in the family unless otherwise specified.

1-2. MANUAL ORGANIZATION

SECTION I, GENERAL INFORMATION. This section contains a description of this manual and the HP 163X logic analyzer family. This section also gives specifications and recommended test equipment for the logic analyzers.

SECTION II, INSTALLATION. Section II explains how to prepare the Logic Analyzers for use.

SECTION III, OPERATION. Operation of the HP 1630A/D/G and HP 1631A/D is outside the scope of this service manual. Section III does give a brief description of front panel controls and information about configuration of the logic analyzers for HP-IB and HP-IL operation. For complete operating instructions see the Operating Manual.

SECTION IV, CONFIDENCE TESTS. This section concerns the execution of software-based function verification Self Test (ST) tests, which includes the interpretation of status codes to verify correct operation.

SECTION V, ADJUSTMENTS. The logic analyzers require several adjustments that can be done with an oscilloscope, voltmeter, programmable signal source and controller; these adjustments are covered this section.

SECTION VI, REPLACEABLE PARTS. This section contains ordering information and a parts list for all models of the family.

SECTION VII, INSTRUMENT CHANGES. This section has information which describes changes to the instruments and how to find proper documentation for the instrument being serviced.

SECTION VIII, SERVICE. The Service section is divided into eight subsections. The first subsection covers the overall system. This includes system theory, and which service group to reference with a failure. The service groups focus on individual subsystems. Information in these groups includes block and component level theory, mnemonics, and schematics relating to that subsystem. Each subsystem and its service group designator is as follows:

8 - Introduction and General Information
8A - A1 Power Supply and A2 Motherboard
8B - A3 CPU, A7 Keyboard and Display
8C - A4 State Master
8D - A5 Timing Master
8E - A8 Timing Slave
8F - A11 State Slave
8G - A13 Analog

APPENDIXES. Three appendixes provide additional information for servicing the 163X family. Appendix A provides an overall view of the troubleshooting and testing routine, including Guided Probe. Guided Probe is a software driven troubleshooting technique used to find faults in the analyzer systems. Appendix B provides supplementary special-case testing which accompanies Guided Probe. Appendix C covers performance tests for the analog channels and analog trigger input.

1-3. INSTRUMENTS COVERED BY THIS MANUAL

Attached to the instrument is a serial number sticker. The serial number is in the form 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five are the suffix. The prefix is the same for all identical instruments; it only changes when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual applies to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page.

An instrument manufactured after the printing of this manual may have a serial number prefix not listed on the title page. This unlisted serial number prefix indicates the instrument is different from those described in this manual. To cover this instrument, a yellow Manual Changes supplement is needed. The supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available on request.

Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. DESCRIPTION

The Hewlett-Packard 1630 and 1631 Logic Analyzers are interactive state and timing analyzers for use in the design and troubleshooting of digital systems. Many functions of the systems are the same. The HP 1630A and 1631A have 27 state channels with three clocks and 8 timing channels. The HP 1630D and 1631D have an additional 8 timing channels. The HP 1630G has an additional 30 state channels. The HP 1631A and 1631D have two analog signal channels and an analog trigger channel. All models feature a menu system for defining measurements which simplifies setup time by reducing the number and complexity of front panel keys. Following is a listing of the key features of the HP 163X systems.

STATE PERFORMANCE FEATURES

- external clock rates to 25 MHz
- two phase demultiplexing
- 1024 deep acquisition memory per channel
- pattern, sequence, and occurrence count triggering
- storage qualification
- state and time interval histogramming

TIMING PERFORMANCE FEATURES

- 100 MHz sample rate on up to 16 channels (8 channels 1630/31A)
- 1024 deep acquisition memory per channel
- pattern, edge, and glitch triggering
- waveform or list displays of acquired data
- x and o cursor system for waveform time interval measurements
- post acquisition processing for auto answers and statistical characterization

ANALOG PERFORMANCE FEATURES
(1631A/D)

- 200 MHz sample rate
- 50MHz analog bandwidth
- 2 channel simultaneous acquisition
- 1024 deep acquisition memory per channel
- analog triggering - slope/level on internal or external
- analog waveform displayed in full pixel graphics
- x and o cursor system for waveform time and voltage measurements
- post acquisition processing for auto answers and statistical characterization
- cumulative display mode for infinite persistence applications

1-5. ACCESSORIES SUPPLIED

The following accessories are supplied with the HP 1630/1631 in the quantities shown in the box below:

HP 10271A: state data probe with HP 10271-63201 lead set
HP 10272A: timing probe with HP 10272-63201 lead set
HP 10273A: 10 channel state data probe with HP 10271-63201 lead set
HP 10435A: 10:1 divider probe

	10271A	10272A	10273A	10435A
1630A	3	1		
1630D	3	2		
1630G	3	1	3	
1631A	3	1		2
1631D	3	2		2

All instruments include the following:

One 2.3 meter (7.5 ft) power cord.
One Hewlett-Packard Interface Loop (HP-IL) cable.
One Operating Manual.

In addition, the HP 1631A and 1631D each include one HP 10230-62101 probe tip and one HP P/N 1250-1454 BNC-to-probe adapter.

1-6. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics, not specifications but typical characteristics included as additional information.

Table 1-1. Specifications

STATE/TIMING INPUT SPECIFICATIONS (HP 1630A/D/G and 1631A/D)

Probes

Input RC: 100K ohms ± 2% shunted by approximately 5 pf at probe body.
Minimum swing: 600 mV p-p
Minimum input overdrive (Above pod threshold): 250 mV or 30% of input amplitude, whichever is greater.
Maximum voltage: ± 40 volts peak
Threshold range: -9.9 to +9.9 volts in 0.1 volt increments, Accuracy 2.5% ±120 mV.
Dynamic range: ± 10 volts about threshold.

State Mode

Clock repetition rate:

Single Phase: 25 MHz with single clock and single edge specified. 20 MHz with any ORed combination of clocks and edges.
Multiplexed: Master-slave clock timing; Master clock must follow slave clock by at least 10 ns and precede next slave clock by 50 ns or more.

Clock pulse width: ≥ 20 ns at threshold.
Setup time: Time data must be present prior to clock transition, ≥20 ns
Hold time: Time data must be present after clock transition, 0 ns

Time Mode

Glitch: Minimum detectable glitch is 5 ns width at threshold.

ANALOG SPECIFICATIONS (HP 1631A/D ONLY)

Channels 1 and 2 (Vertical)

Probe Factors: 1:1, 10:1, or 50:1 probe attenuation factors may be entered to scale the HP 1631A/D to input voltages at the probe tip. All vertical specifications relate to a 1:1 probe factor.

Range: 40 mV to 2.5 V full-scale, automatically calibrated internally with two-digit resolution with each change in format specification.

Bandwidth (-3 dB) dc coupled: dc to 50 MHz
Dc gain accuracy: ±2.5% of full-scale
Channel isolation: 55 dB from dc to 50 MHz
Analog-to-digital conversion (ADC) resolution: ±1 LSB, which is ±1.6% of full scale.
Dc offset range/resolution:

Offset Range	*Offset Resolution*
±1.5 V	approximately 1 mV

Transition time: ≤5.25 ns, 20% to 80% of full-scale.
Input coupling: dc
Input RC: 1 Megohm ±2%, shunted by approximately 14 pF
Maximum safe input voltage: ±40V (dc + peak ac)

Table 1-1. Specifications (cont.)

Trigger (Analog)

Sources: channel 1, channel 2, or external trigger input.
Edge: rising or falling edge may be selected for any source.
Sensitivity: (square wave up to 10 MHz)
-.2 of full scale for channels 1 and 2
50 mV p-to-p for external
Up to 50 MHz
.3 of full-scale for channels 1 and 2
100 mV p-to-p for external
Level range/resolution:
internal: within the display window/approximately 1% of full scale
external: ±2 V in 1 mV steps
External trigger input:
Maximum safe input voltage: ±40 V (dc + peak ac)
Input coupling: dc
Input RC: 1 Megohm ±2%, shunted by approximately 14 PF

Time Base (Horizontal)

Sample period: 5 ns to 500 ms in a 1-2-5 sequence.
Range: 125 ns to 500 s full-scale (10 divisions).
Time base accuracy:
Sample period: ± .01%
Time-interval measurement accuracy: (equal rise and fall times)
Single-shot: ≤ ±1.5 ns for 5 ns sample period
≤ ±1 sample period for sample periods of 10 ns or greater
Continuous: ≤ ±.15 times sample period, based on 100 averages

Delay

Tracepoint: equals trigger plus delay; trace point can be delayed from 0 to 262, 143 sample periods after the trigger.
Tracepoint placement accuracy: within ±1 sample period ±.1 times full-scale voltage divided by the slew rate of the input signal.
Tracepoint position: can be set approximately 50 sample periods from the start, end, or near the center of the data record. A 1024-sample record can be positioned with about 950 samples before the tracepoint, or with the entire data record beginning up to 262,074 samples after the trigger.

Note: Specifications apply after a 30 minute warm up period. Single-shot reconstruction uncertainty = +/-1 ns (applies for time ranges of 50 ns thru 2 us).

Table 1-2. Supplemental Characteristics

POWER:

115/230 Vac, -22% to +10%, 48-66 Hz, 275 W max for HP 1630A/D/G, 300 W max for HP 1631A/D

OPERATING ENVIRONMENT:

Temperature: 0 to +55° C (32 to 131° F)
Humidity: Up to 95% relative humidity at +40° C (non-condensing)
Altitude: To 4600 meters (15 000 feet)
Vibration: Vibrated in three planes for 15 minutes each with 0.3mm excursions at 5 to 55 Hz.

WEIGHT:

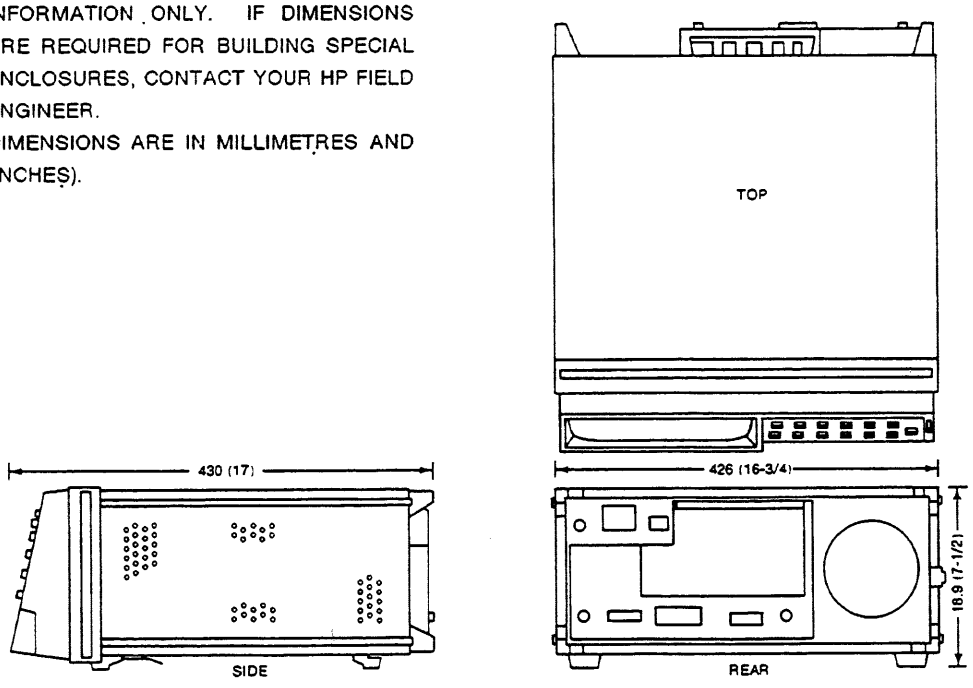
HP 1630A: net 12.6 kg (28 lbs); shipping 17 kg (38 lbs).
HP 1630D: net 13.2 kg (29 lbs); shipping 17.7 kg (39 lbs).
HP 1630G: net 13.6 kg (30 lbs); shipping 18.1 kg (40 lbs).

HP 1631A: net 13.2 kg (29 lbs); shipping 17.7 kg (39 lbs).
HP 1631D: net 13.8 kg (30 lbs); shipping 18.4 kg (40 lbs).

DIMENSIONS:

NOTES:

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



1-7. RECOMMENDED TEST EQUIPMENT

Table 1-3 lists the equipment required to adjust and troubleshoot the HP 1630A/D/G and HP 1631A/D. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 1-3.

Table 1-3. Recommended Test Equipment

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
EQUIPMENT USED FOR ALL MODELS			
1630/31 Product Support Package	No substitute		P,A,T
Desktop Computer	HP 200 Series Compatible BASIC HP-IB Interface	HP 9826A HP 9836A	P,A,T
Signature Multimeter	HP-IB Controllable, with DVM	HP 5005B	T
Oscilloscope	Dual channel, delayed sweep. Bandwidth: dc to 275 MHz. Time Interval Measurements and ±500 picosecond accuracy	HP 54100A/D with (2) 54003 pods (2) 54003-61617 probes	P,A,T
Current Tracer	No substitute	HP 547A	T
Portable Fan	Supplies moving air to cool PC Boards in the service slot. (REQUIRED)		A,T
ADDITIONAL EQUIPMENT NEEDED FOR 1631A/D TESTING			
Programmable Signal Source	1 to 50 MHz at 0.001% accuracy, Distortion: <36dB	HP 8165A	P,A,T
Pulse Generator	Transition time: ≤1ns Repetition rate: 1Mhz 0-2 Volt Output Offset Output	HP 8082A	P
Function Generator	Sine and Square Wave 10KHz to 50MHz Amplitude: 2 Volts 0 to ±2 Volt Offset Output **	HP 8116A	P
RF Voltmeter	Accuracy: ±3% at 50 MHz	HP 3406A	P
Time Mark Generator	Time Marks: 100 ns Accuracy: ≤1%	Tektronix TG 501	P

* P=Performance Testing, A=Adjustments, T=Troubleshooting ** See note on following page.

Table 1-3. Recommended Test Equipment cont.

EQUIPMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
EQUIPMENT USED FOR 1631A/D (CONT)			
50Ω Sampling Tee	----------	HP Model 10221A	P
50Ω Terminaton (2)	Accuracy ≤1%	HP 10100C	P
Adapter (2)	GR874-to-BNC(f)	HP Part No. 1250-0850	P
Adapter	BNC(m)-to-BNC(m)	HP Part No. 1250-0216	P
BNC Cable	48-inch	HP 10503A	P

* P=Performance Testing, A=Adjustments, T=Troubleshooting

NOTE: If a substitute function generator does not have offset, a power supply and DVM can be used for the test requiring DC voltage (see appendix C).

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section contains the initial operation information for the HP 1630A/D/G and 1631A/D logic analyzers. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

2-2. PREPARATION FOR USE

2-3. POWER REQUIREMENTS. The logic analyzers require a power source of either 115 or 230 VAC -22% to +10%; single phase, 48 to 66 Hz; 300 watts maximum.

CAUTION

The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input line voltage.

2-4. LINE VOLTAGE SELECTION. Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage. The 6 Amp fuse installed satisfies both voltage settings of 115 and 230 VAC.

2-5. POWER CABLE. This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See figure 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are listed in the parts list in Section VI.

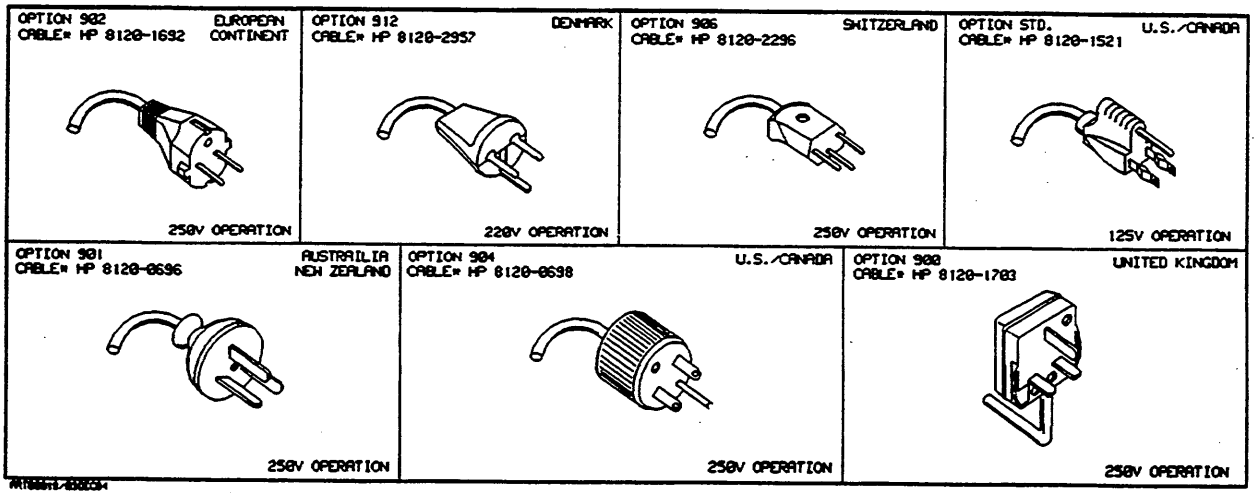


Figure 2-1. Power Cord Configurations

2-6. OPERATING ENVIRONMENT

The operating environment is noted in table 1-2. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

The logic analyzer will operate to all specifications, within the temperature and humidity range given in table 1-2. However, reliability is enhanced by operating the instrument within the following recommended ranges:

Temperature: 20 to 35° C (68 to 95° F)

Humidity: 20 to 80% non-condensing

High temperature and humidity combinations should be avoided.

2-7. CLEANING REQUIREMENTS

When cleaning the logic analyzer, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys.

2-8. STORAGE AND SHIPMENT

2-9. Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature: -40° C to +75° C
Humidity: Up to 90% at 65° C
Altitude: Up to 15 300 metres (50 000 feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

2-10. Packaging

2-11. TAGGING FOR SERVICE. If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-12. ORIGINAL PACKAGING. If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-13. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

SECTION III
OPERATION

3-1. INTRODUCTION.

The operation of the 1630A/D/G and 1631A/D is outside the scope of this service manual. However, a brief explanation of the operation of each key is given below. For more complete operating instructions refer to the Operators Manual.

1 **BLUE KEY:** This key activates the blue **SHIFT** function assigned to each keyboard key. A momentary press activates the **SHIFT** function for the next keystroke. The **SHIFT** function continues if the key is kept depressed.

2 **INPUT DISPLAYS:** Three keys that select menu sets. **SYSTEM** calls up menus that define instrument configuration, set up secondary configurations and outputs for peripherals, and control disk or tape operations (if connected and active). **FORMAT** has three menus that determine how data is collected and interpreted on the display. **TRACE** is a series of menus that specify the measurement mode and parameters for collecting data.

3 **OUTPUT DISPLAYS:** Three keys that select a state display **(LIST)** timing display **(WFORM)**, or performance overview chart **(CHART)**.

4 **LINE** turns on operating power.

5 **RUN** initiates a new measurement. **RESUME** continues an incomplete measurement that was halted by the **STOP** key.

6 **STOP** terminates a measurement. **RETURN TO LOCAL** overrides an HP-IB or HP-IL controller to return control of the 1631 to the keyboard.

7 **PRINT** commands the current display to be printed on a graphics printer. **PRINT ALL** prints the entire contents of the displayed menu or list, including all on- and off-screen information.

8 Hex keyboard for data entry.

9 **NEXT [ ]** and **PREV [ ]** keys cycle through all the menu selections available for fields enclosed in brackets, [ ].

10 **CHS** is used to change +/- signs when specifying memory locations in either direction from the trigger event, and when specifying polarities. **CHS** prints a dash when used in a text field.

11 **DON'T CARE** enters an "X" in lieu of a number, to indicate "any value will serve".

12 **CURSOR**: These keys move the cursor from field to field in the menus. The blue **SHIFT** function allows these keys to rearrange the order of labels in the menus, and to move the cursor from pod to pod in the label lines of the FORMAT [Assignment] menu. The **CURSOR** keys can also move the configuration bar in the SYSTEM [Configuration] menu, and the "x" and "o" markers on the waveform and chart displays.

13 **ROLL** keys move timing displays left or right, state lists up or down, and the configuration bar in the SYSTEM [Configuration] menu.

14 **INSERT/DELETE** are used to add or delete fields and labels.

15 **CLEAR ENTRY:** This is the field eraser key. **DEFAULT** returns all fields in the displayed menu to power-up conditions.

ANALOG INPUTS

The following features are part of the 1631A/D only.

16 **INPUT 1:** Analog Channel 1 input BNC connector. Input RC is 1MΩ ≈14pF. Do not apply more than ±40V.

17 **INPUT 2:** Analog Channel 2 input BNC connector. Input RC is 1MΩ ≈14pF. Do not apply more than ±40V.

18 **EXT TRIG:** Analog External Trigger input BNC connector. Input RC is 1MΩ ≈14pF. Do not apply more than ±40V.

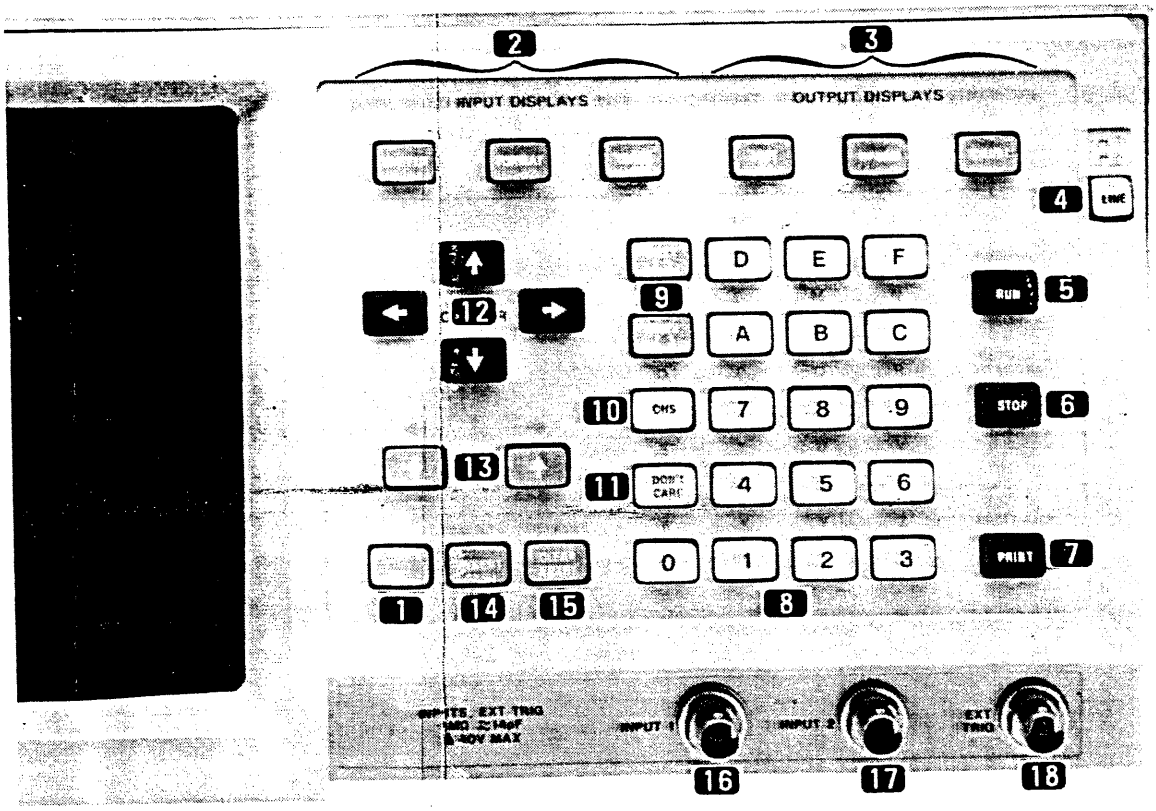


Figure 3-1. Front Panel Controls

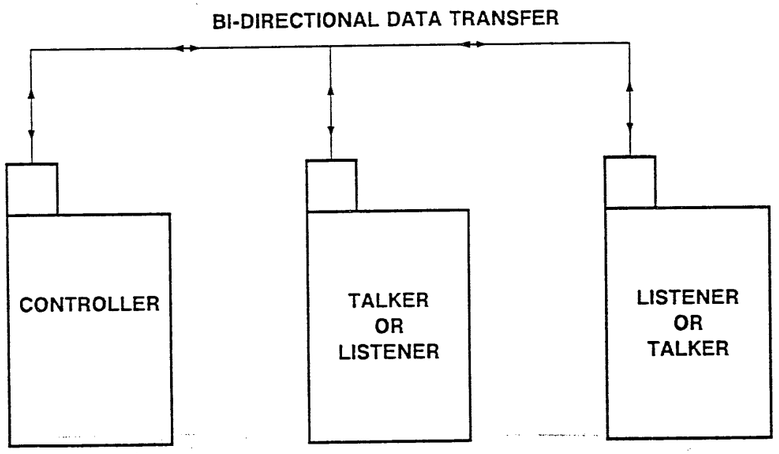


Figure 3-2. HP-IB System Configuration

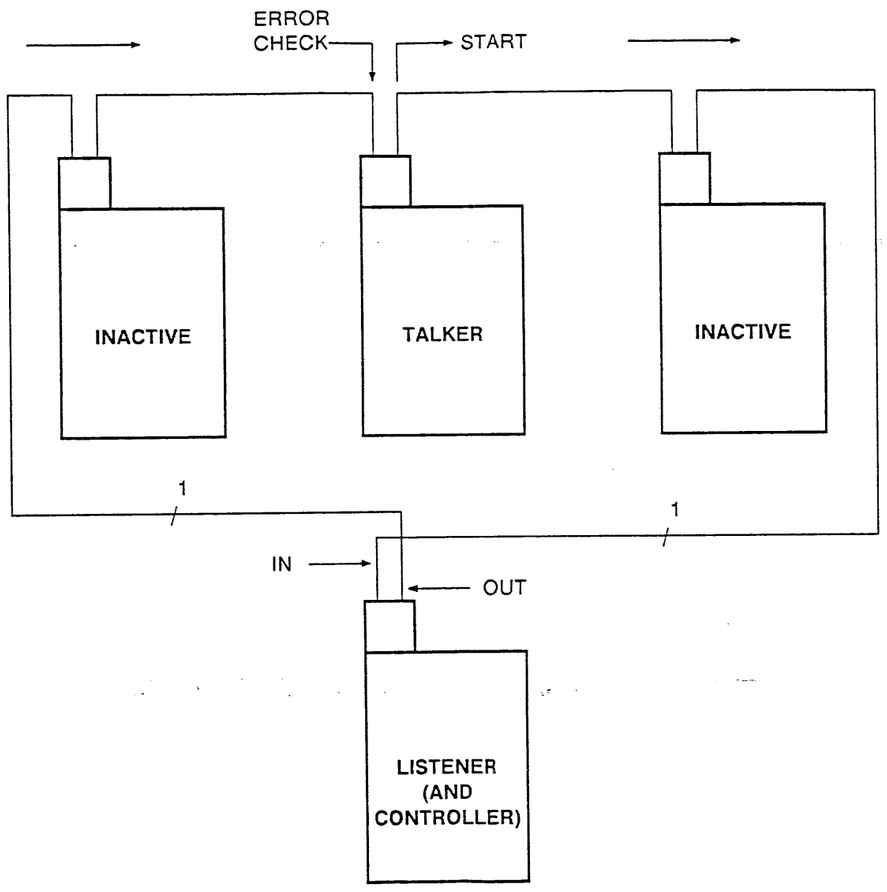
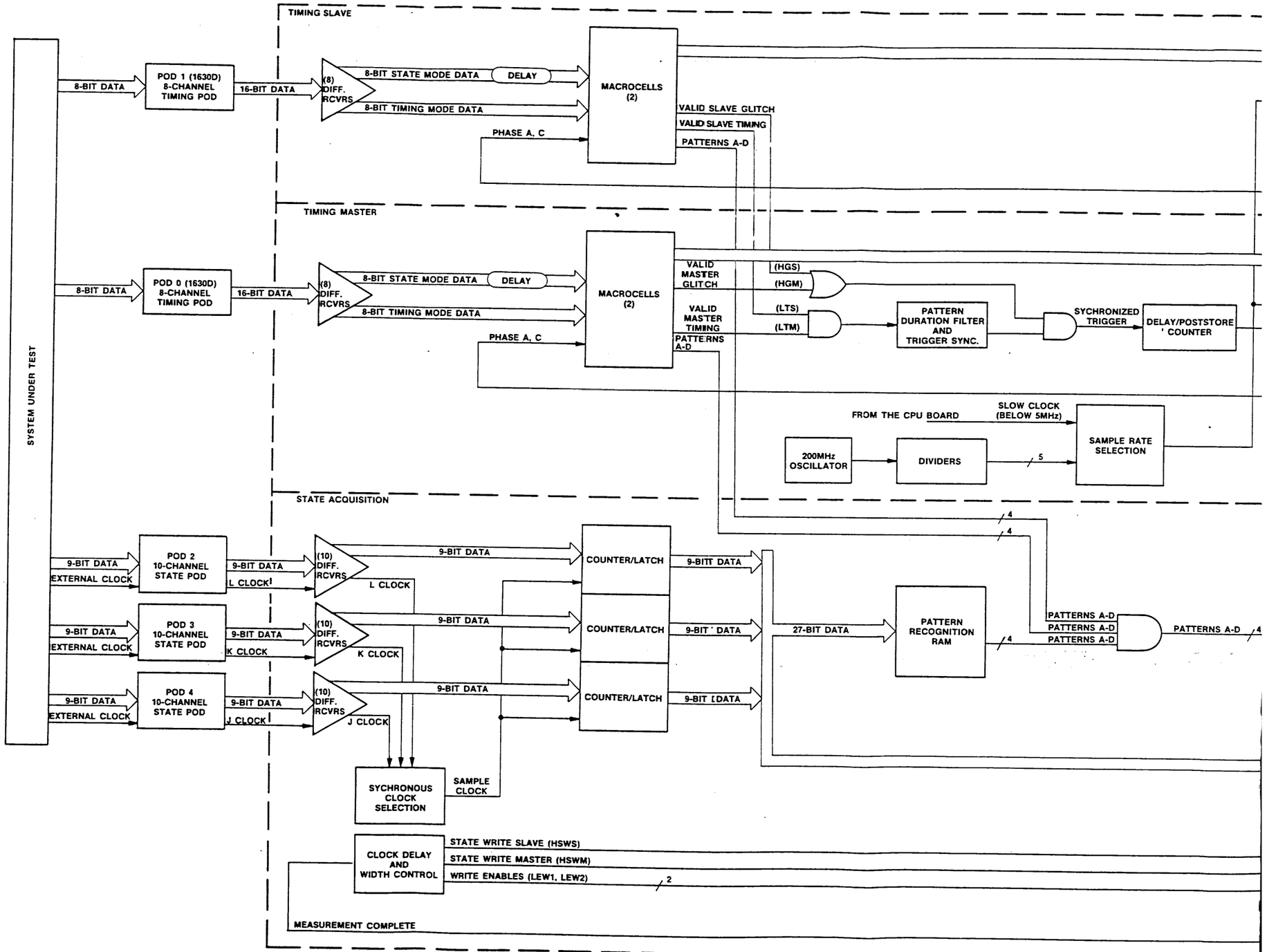


Figure 3-3. HP-IL System Configuration


TIMING SLAVE
SYSTEM UNDER TEST
8-BIT DATA
POD 1 (1630D) 8-CHANNEL TIMING POD
16-BIT DATA
(8) DIFF. RCVRS
8-BIT STATE MODE DATA
DELAY
8-BIT TIMING MODE DATA
MACROCELLS (2)
VALID SLAVE GLITCH
VALID SLAVE TIMING
PHASE A, C
PATTERNS A-D
TIMING MASTER
8-BIT DATA
POD 0 (1630D) 8-CHANNEL TIMING POD
16-BIT DATA
(8) DIFF. RCVRS
8-BIT STATE MODE DATA
DELAY
8-BIT TIMING MODE DATA
MACROCELLS (2)
VALID MASTER GLITCH
VALID MASTER TIMING
PATTERNS A-D
PHASE A, C
(HGS)
(HGM)
(LTS)
(LTM)
PATTERN DURATION FILTER AND TRIGGER SYNC.
SYCHRONIZED TRIGGER
DELAY/POSTSTORE ' COUNTER
FROM THE CPU BOARD
SLOW CLOCK (BELOW 5MHz)
200MHz OSCILLATOR
DIVIDERS
5
SAMPLE RATE SELECTION
STATE ACQUISITION
9-BIT DATA
EXTERNAL CLOCK
POD 2 10-CHANNEL STATE POD
9-BIT DATA
L CLOCK
(10) DIFF. RCVRS
L CLOCK
9-BIT DATA
COUNTER/LATCH
9-BITT DATA
POD 3 10-CHANNEL STATE POD
K CLOCK
K CLOCK
COUNTER/LATCH
9-BIT ' DATA
27-BIT DATA
PATTERN RECOGNITION RAM
PATTERNS A-D
PATTERNS A-D
PATTERNS A-D
PATTERNS A-D
POD 4 10-CHANNEL STATE POD
J CLOCK
J CLOCK
COUNTER/LATCH
9-BIT DATA
SYCHRONOUS CLOCK SELECTION
SAMPLE CLOCK
CLOCK DELAY AND WIDTH CONTROL
STATE WRITE SLAVE (HSWS)
STATE WRITE MASTER (HSWM)
WRITE ENABLES (LEW1, LEW2)
2
MEASUREMENT COMPLETE

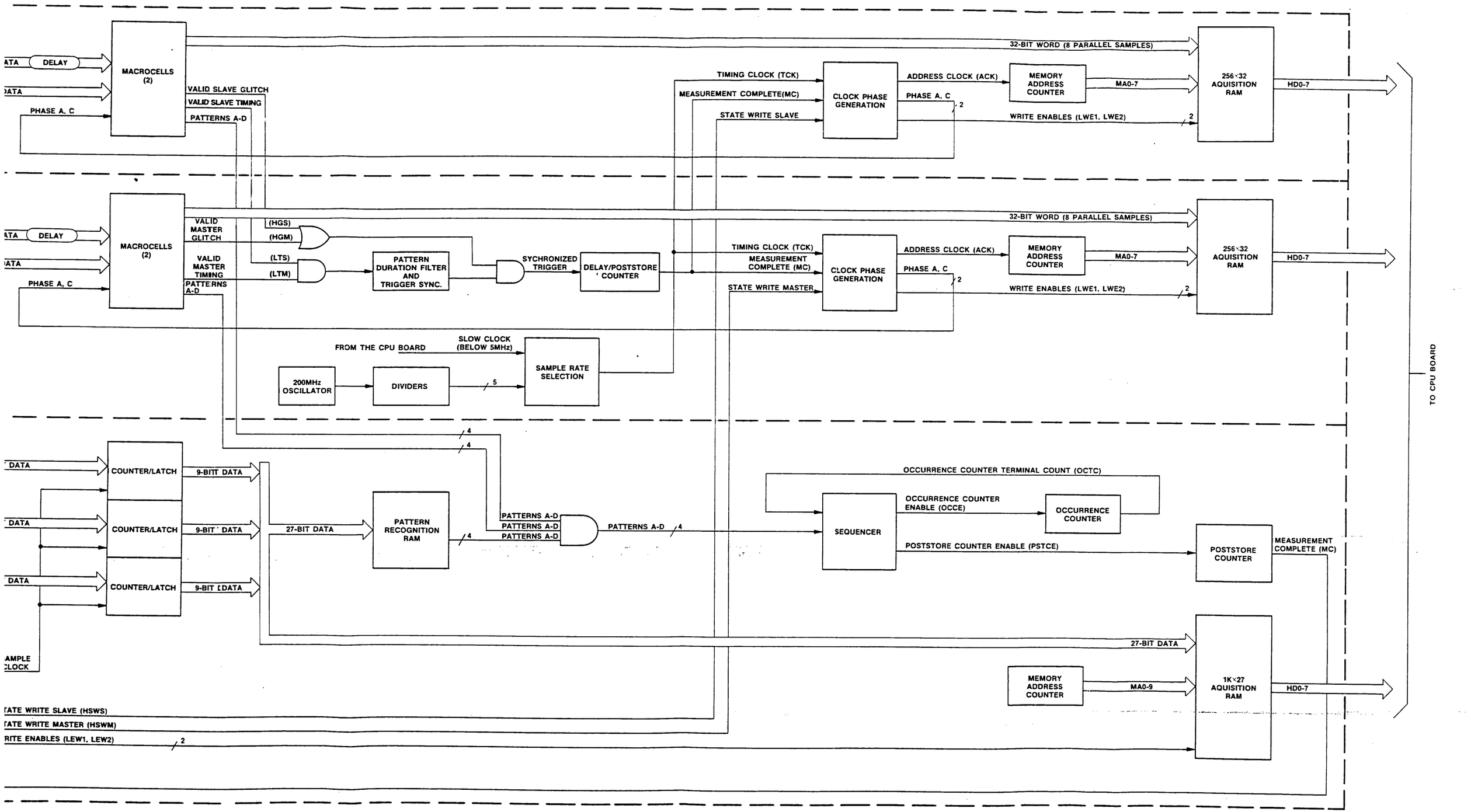


Figure 8D-1. State and Timing Acquisition System

SECTION IV
CONFIDENCE TESTS

4-1. INTRODUCTION

This section will acquaint the user with the HP 1630A/D/G and 1631A/D Self Tests (ST). ST is a series of tests, resident in ROM, that confirms correct operation of the mainframe hardware and firmware. The ST tests do not verify all of the critical specifications given in table 1-1 of Section I. These tests check the basic functions of the system.

Please note that the Self Test is a troubleshooting aid, but will not find 100% of instrument failures. Whenever servicing a 1630/31, the operational tests, adjustments, any necessary functional tests, and the ET 19776 tests must also be completed before full functionality and performance can be assured. The Operation Verification tests are covered in Appendix A. See the ET 19776 manual for the Performance Verification tests.

Note: The terms MPU or processor, and MMU will be used throughout this manual in reference to the Microprocessor Unit and the Memory Management Unit used on the CPU board.

4-2. EQUIPMENT REQUIRED

The equipment required for the self tests is listed in table 1-3, Recommended Test Equipment, Section I.

4-3. SELF TEST FUNCTION VERIFICATION

4-4. Initiating 1630/1631 Self Test (ST)

ST can be initiated by setting the rear panel Self Test switch, #6, into the "1" or open position and cycling power OFF/ON.

NOTE

The processor samples the setting of the system status switches ONLY during turn-on. Changing SW6 to "1" after turn-on will not initiate SELF TEST. Cycling the power OFF/ON will reset the switch status. After ST is executed, however, the ST switch may be set to a "0" allowing the System Specification menu to be displayed without cycling power.

After power is cycled OFF/ON and an initialization routine is executed, the ST routine will begin. The ST test sequence is as follows:

a. RAM test.

b. ROM test.

c. Acquisition test.

d. Analog Test.

e. HP-IB test.

4-5. Self Test RAM Test Procedure

PURPOSE:

The RAM test verifies the MPU's and MMU's ability to read and write from all 64K RAM locations on the CPU board.

CIRCUITRY TESTED:

RAM, MPU and MMU interaction, RAM refresh by the CRT controller, RAM strobe timing circuitry, and ROM selection and data transfer.

OPERATION:

a. Before the RAM test begins, an initialization routine is done for the CRT controller (CRTC). This initialization routine reads the rear panel switches, etc.

b. The processor configures the memory management unit (MMU) to map a 2K (800H) block of RAM.

c. The processor (MPU) writes a 01, 02, 03, ... 80, 00 hex pattern sequentially through each 2K block of RAM. The pattern used is derived by shifting-left the contents of the A accumulator.

d. After all 64K of RAM is mapped, the processor sequentially reads back the contents of RAM. The value stored is compared to the present value of the A accumulator.

e. If the value stored does not match the present value of the A accumulator, then an "Error in RAM" message is displayed.

f. If after all 64K of RAM is tested and no compare error exists, then a ROM and Acquisition test is performed.

ERROR MESSAGE INTERPRETATION:

If an "Error in RAM" message is displayed, Blue-stripe the CPU board.

4-6. Self Test ROM Test Procedure

PURPOSE:

The ROM test verifies that all of the firmware is good. The test also checks that the processor (MPU) and memory management unit (MMU) can address and retrieve data from ROM.

CIRCUITRY TESTED:

All ROMs, MPU and MMU interaction, ROM selection and data transfer, and RAM.

OPERATION:

a. Before the ROM test begins, the RAM test must have passed.

b. The processor configures the MMU to map an 8K block of ROM.

c. Information is read from ROM and a checksum routine is done for each ROM. The checksum for each ROM is compared to a stored checksum value of that ROM in ROM #7 (U4H).

d. If the checksums do not match, then a "Error in ROM #X Expected XX Was XX" message is displayed.

e. If all of the checksums match, then an Acquisition test is performed.

ERROR MESSAGE INTERPRETATION:

If an "Error in ROM #X(0-7) Expected XX Was XX" message is displayed, it is interpreted as follows:

Error in ROM #X(0-7) - X indicates the faulty ROM number given as:

U3K = ROM #0	U4K = ROM #4
U3J = ROM #1	U4J = ROM #5
U3I = ROM #2	U4I = ROM #6
U3H = ROM #3	U4H = ROM #7

Expected XX - indicates the stored checksum value in ROM #X for that ROM (given in hex).

Was XX - indicates the checksum tabulated for that ROM during the test (given in hex).

If after replacing the suspect ROM, the failure still exists, Blue-stripe the CPU board.

4-7. Self Test Acquisition Test Procedure

PURPOSE:

This test verifies the processor's ability to configure the system to take a state measurement. It also verifies that all pod channels can sample data between -9.9 and +9.9 volts.

CIRCUITRY TESTED:

This test checks the processor, system timing control, state and timing boards, and the pods.

OPERATION:

a. Both RAM and ROM tests must have passed before this test begins.

b. The processor configures the system for a Trace Specification of <don't care start-on any state, trace all states>.

c. System starts tracing with pods 4, 2, 0 thresholds set at +9.9 volts and pods 3 and 1 set at -9.9 volts. "0s" should be sampled on pods 4, 2, 0 and "1s" should be sampled on pods 3 and 1.

d. 512 states are clocked in and sampled at this threshold pattern.

e. A sample is taken for "measurement complete". It should be false.

f. The pod threshold voltages are reversed, making the sample pattern of step (c) reversed.

g. 511 states are clocked in and sampled at this threshold pattern.

h. A sample is taken for "measurement complete". It should be false.

i. The memory counter is sampled for words remaining; one should remain.

j. The last word is clocked in, making the "measurement complete" status true. The trace is then halted.

k. Any acquisition errors are summarized and the self test determines if a Timing Slave board is in the instrument. If a Timing Slave board is not in the system, errors are ignored for the Timing Slave channels.

l. If an error occurred, a "Acq Error XX . . . XX" message will be displayed in hex. The number of hex pairs in the message depends on the instrument model. See the error message information following.

m. If no errors occurred "Self Test Passed Reset Rear Panel Switch to xxxx x0xx to continue" message should be displayed. When the switch is reset the System Specification menu should be displayed.

ERROR MESSAGE INTERPRETATION

There are two forms of acquisition error message in the HP 163X family.

```
"Acq error XX XX XX XX XX XX XX XX XX XX"
```

This error message is present on the latest versions of the HP 163X family and can be generally thought of as covering instruments with disc-based mass storage capability. This message must be interpreted differently depending on whether the instrument is a 1630/31A/D or a 1630G. Table 4-1 covers specific interpretation of 1630/31A/D messages and table 4-2 covers 1630G messages.

```
"Acq error XX XX XX XX XX XX XX"
```

This message covers earlier versions of HP 1630A/D and all 1630A/D option 007. These instruments have firmware for using them with tape-based mass storage. Specific interpretation of error messages is covered in table 4-3.

The error message, a series of HEX digits must be converted to a binary equivalent before it can be fully interpreted. The following general example of a 1631D failure shows how this is done.

```
"Acq error 01 80 00 00 00 00 03 00 00 00"

  01       80       00       00       00       00       03       00       00       00
00000001 10000000 00000000 00000000 00000000 00000000 00000011 00000000 00000000 00000000
```

a. This example shows that incorrect Acquisition data was acquired.

b. Trace point was not found.

c. All channels passed except pod 0 (Timing Master) Channels 1 and 0.

d. All analog acquisition passed.

If failures occur in this test, try swapping LIKE pods to determine if the problem follows the pod. If the failure does follow the pod, that pod may need to be replaced.

Whenever an acquisition error occurs, always check that the pods are properly seated in their connectors and that none of the connector pins are bent. If all of the channels on any board fail, check that the board is properly seated in it's motherboard connector.

After completion of the self-test, continue with the operational tests (see chart on page A-2 for 1630/31A/D or page A-4 for 1630G).

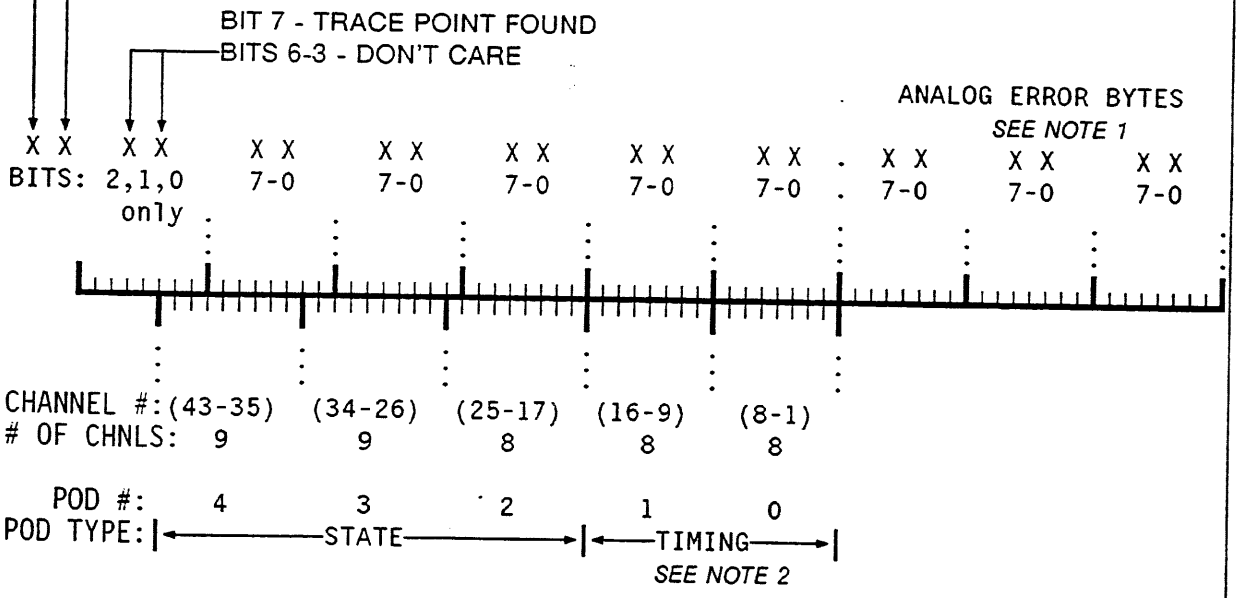
Table 4-1. 1630A/D, 1631A/D Error Mesage Interpretation.

This table covers interpretation of errors in 1630A/D and 1631A/D in the most recent versions, those with disc-based mass-storage capability.

For earlier 1630A/D, those with tape-based mass storage (also option 007), see table 4-3.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE 1: Analog errors are only relevant in the 1631A/D. For 1630A/D this section of the error code will show all bits passing. For analog errors see paragraph 4-8.

NOTE 2: In the case of timing errors, channels 8-1 actually represent the Timing Master and channels 16-9 the Timing Slave. The example above represents a 1630/31D. If the instrument is a 1630/31A, the test will show channels 16-9 as passing and channels 8-1 will represent POD 1.

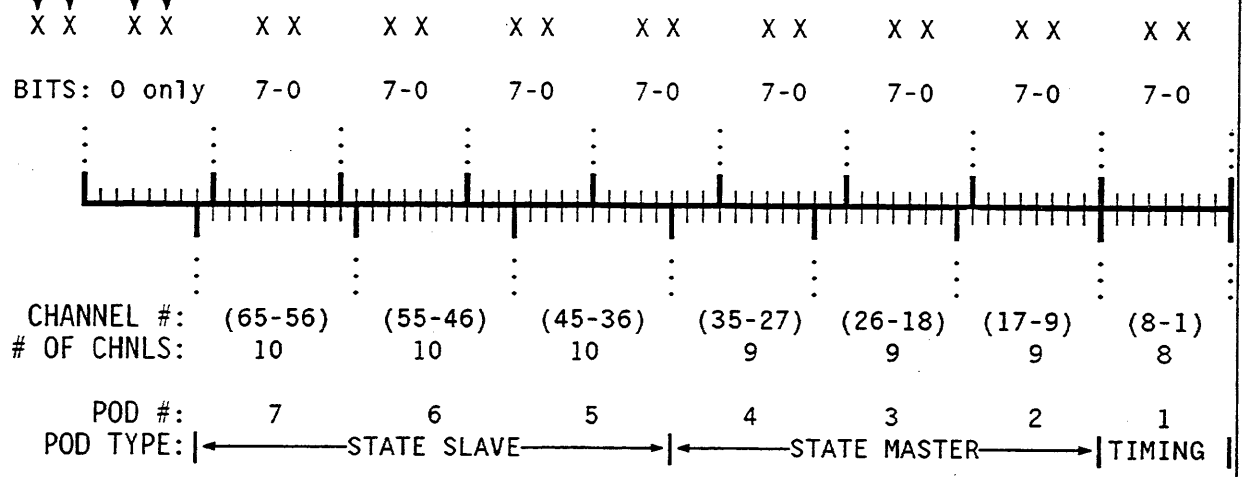
NOTE 3: Each pair of analog error bytes has 8 bits (4 bits per byte). Since the timing pods (pods 0 and 1) have 8 channels, the 8-bit pairs of error bytes interpret directly to the timing pods' 8 channels. However, the state pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. As in the diagram above, the one bit offset must be taken into account when interpreting acquisition errors.

Table 4-2. 1630G Error Mesage Interpretation.

This table covers error message interpretation in 1630G only.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE: Since the timing pod has 8 channels, the 8-bit pair of error bytes interpret directly to the timing pods' 8 channels. However, the state master pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. The State Slave pods (pods 5, 6, and 7) have 10 channels and the byte to channel interpretation is offset by two bits per pod. As in the diagram above, the bit offset must be taken into account when interpreting acquisition errors.

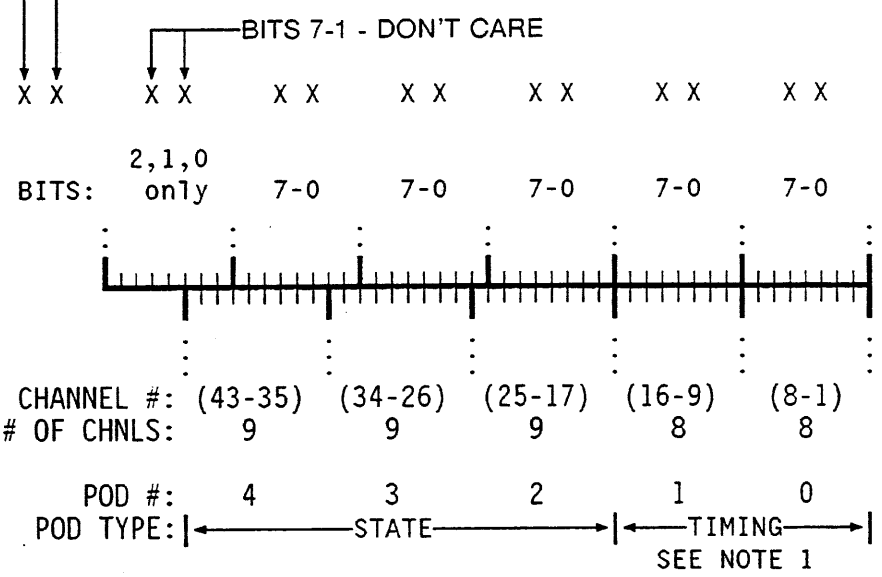
Table 4-3. Earlier 1630A/D Error Mesage Interpretation.

This table covers error message interpretation in 1630A/D of earlier vintage as well as recent 1630A/D with tape-based mass-storage (option 007).

For recent 1630A/D, those using disc-based mass-storage, see table 4-1.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE 1: In the case of timing errors, channels 8-1 actually represent the Timing Master and channels 16-9 the Timing Slave. The example above represents a 1630D. If the instrument is a 1630A, the test will show channels 16-9 as passing and channels 8-1 will represent POD 1.

NOTE 2: Since the timing pod has 8 channels, the 8-bit pair of error bytes interpret directly to the timing pods' 8 channels. However, the state pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. As in the diagram above, the bit offset must be taken into account when interpreting acquisition errors.

4-8. 1631A/D Analog Acquisition Self Test

PURPOSE:

This test verifies operation of the DAC, Trigger Threshold, and in general everything that is vital to calibration.

CIRCUITRY TESTED:

This test checks the DACs, Trigger Threshold, status and address lines of the CPU, Gain Hybrid, and input relay.

BYTE I OPERATION:

1. Test Channel 1

   a. Calibration Mode is selected.

   b. Maximum gain (full-scale vernier and X32 gain) on channel 1 is set and trigger on Channel 1.

   c. External offset is set to 0.

   d. Channel 1 offset is set to -2.048 volts.

   e. The trigger threshold status is read.

   f. Channel 1 offset is set to +2.048 volts.

   g. The trigger status is read again. If the status is not equal to the previous reading then an error is indicated.

2. Test Channel 2

   Same as channel 1

3. Test External Offset

   a. Channel 2 trigger is selected.

   b. External Offset is set to -2.5 volts.

   c. Trigger status is read.

   d. External Offset is set to +2.5 volts.

   e. Trigger status is read again. If it is the same as the previous reading an error is indicated.

4. Relay Switch test.

   a. Relay switch is turned to normal mode (calibration off).

   b. External offset is set to -2.5 volts.

   c. Trigger status is read.

   d. External offset is set to +2.5 volts and trigger status is read again. If the status is not the same as the previous reading an error is indicated.

BYTE II OPERATION:

Test Status Lines

   a. Calibration Mode, trigger immediate is selected.

   b. Delay Counter is set to 0FFF1H.

   c. Poststore Counter is set to 0.

   d. Memory Address Counter is set to 0FFH.

   e. Status is read. If Prestore is valid an error is indicated. (error = status byte).

BYTE III OPERATION:

Check the Counters

   a. Continuing the same conditions from Byte II above, four clocks are generated. Status is read. Only Prestore has to be set.

   b. Four more clocks are generated and status is read. LLSYNTRG (Latched Synchronous Trigger) should be low true. If not, error.

   c. Sixty (60) more clocks are generated and status is read. LLSYNTRG should be low true and LTPF (Tracepoint Found) low true. If not, error.

   d. Fifty-six (56) more clocks are generated and the status is read. The conditions at the end of step c should still be true. If not, error.

   e. Four (4) more clocks are generated and the status is read. Measurement should be complete. LMFUL (Memory Full) and LAMC (Analog Measurement Complete) should be low true.

1631A/D ANALOG TEST ERROR BYTE INTERPRETATION:

The analog acquisition error is a series of hex digits. The binary equivalent of these digits can be interpreted with the following table:

Error Bytes:	I	II	III
	XX	XX	XX
Bits:	(7-0)	(7-0)	(7-0)

Description:

Byte I:

BIT 7 6 5 4 3 2 1 0	
1 Ø Ø X X X X X	Channel 1 offset malfunction
Ø 1 Ø X X X X X	Channel 2 offset malfunction
Ø Ø 1 X X X X X	External offset malfunction
1 1 1 X X X X X	Trigger threshold malfunction
X X X 1 X X X X	Relay switch malfunction

Byte II:

BIT	VALUE	MALFUNCTION
7	Ø	Prestore Counter
6	1	Poststore Counter
5	1	MAC, Poststore, or Memory Full Flip-flop
4	1	Prestore or Poststore Counters
3	X	Don't care
2	1	Clock circuitry
1	X	Don't care
Ø	X	Don't care

Byte III:

BIT	VALUE	MALFUNCTION
7	1	Prestore Counter
6	1	Measurement Complete on Analog Board false when it should be true.
5	1	Memory did not wrap around when it should have.
4	1	Tracepoint was not found when it should have been.
3	1	Memory wrapped around when it shouldn't or Measurement complete on board is true when it should be false.
2	1	Trigger condition not received when it should have been.
1	X	Don't care
Ø	X	Don't care

If any analog errors occur during self-test, blue-stripe the analog board.

4-9. 1630G Internal Storage Test and Reset

When an error is found in internal storage the following will be displayed on the screen:

"Internal checksum error"

It is necessary then for the 1630G to reset internal storage. This will be done automatically by the 1630G and the message "WAIT Resetting internal storage" will be displayed. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed.

To manually reset internal storage, first put the instrument into the self-test mode, then toggle switch 1 (MSB) of the HP-IB address switch. The message "WAIT Resetting internal storage" will appear on-screen while the reset is taking place. When the reset has been completed successfully, the message "Internal storage reset successful" is displayed. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed on-screen.

The analyzer may be used without the internal storage and the rest of the performance of the analyzer is not affected.

SECTION V
ADJUSTMENTS

5-1. INTRODUCTION

This section contains adjustment procedures for the power supply, CPU board, display driver, Timing Master board (if applicable), State Master board and Analog board. Perform the adjustment procedure only after instrument repairs. The adjustments can be made separately.

Board removal procedures, necessary before installing boards into the service connector, can be found in Section VIII. An auxiliary fan must be used to cool boards being run in the service connector.

WARNING

Read the safety summary at the front of this manual before performing adjustment procedures.

CAUTION

The adjustments are performed with the top and side covers removed. Use care to avoid shorting or damaging internal parts of the instrument.

5-2. EQUIPMENT REQUIRED

A list of recommended test equipment is provided in Section I, table 1-3.

5-3. POWER SUPPLY ADJUSTMENT

a. Turn OFF the logic analyzer and remove power cord.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover. Remove cover.

c. Connect an external DVM to measure volts between GND and -5.2V on test connector TP2 (corner of board near CRT).

d. Plug in power cord and turn the logic analyzer ON.

e. Adjust trimpot R34 (labeled VOLT ADJ) until the measured value of -5.2V reads between -5.0 and -5.4 volts. Measure the +5.0V supply; it should be between +4.8 and +5.2 volts.

f. Adjustment complete. Replace covers.

5-4. CPU ADJUSTMENT

a. Referring to the CPU Board Removal procedure in Section VIII, remove the processor board (A3).

b. With power OFF, install the CPU board into the upright service connector J1.

c. Connect the cables from the keyboard and display driver.

d. Place the instrument's top cover over the exposed power supply to prevent tools from dropping onto the power supply, and to maintain proper air flow.

e. Connect a DVM between U100 pin 4 (negative lead) and U100 pin 6 (positive lead).

f. Turn ON the logic analyzer.

g. Adjust trimpot R37 (located at the bottom-right) until the DVM reads +5.00 volts +/-5 mV.

h. Adjustment complete. Replace board and covers.

5-5. DISPLAY SYSTEM ADJUSTMENTS

This adjustment procedure is in two parts; yoke and display driver. The Yoke Adjustment Procedure must be performed if any part of the Display System is replaced (CRT, display driver, or yoke) or if a display cannot be aligned on the CRT screen. If the Yoke Adjustment Procedure is performed then the Display Driver Adjustment Procedure must also be done; if not, then the latter may be done alone. It is good practice to discharge the CRT before beginning.

YOKE ADJUSTMENT PROCEDURE

a. Turn OFF the logic analyzer.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove cover.

c. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

d. Remove the two yoke connectors.

e. Insure that the yoke is firmly pressed against the flange of the CRT. If not, loosen the yoke neck screw that attaches the yoke to the CRT and slide the yoke against the CRT. Gently tighten the screw until firm.

f. While holding a flexible straight edge from the lower-left corner to the upper-right corner of the CRT (facing the CRT), make a mark about one inch long with a water soluble felt pen across the center of the CRT. See figure 5-1.

g. Repeat the above step for the upper-left corner and the lower-right corner forming an "X" in the center of the CRT. See figure 5-1.

h. Adjust BRIGHTNESS control pot to minimum (full counter-clockwise). See figure 5-2 for the display adjustment locations.

i. Turn ON the logic analyzer.

j. Adjust BRIGHTNESS control pot until a dot appears on the CRT.

k. The dot should appear within a .3 cm (1/8 inch) radius of the intersection of the two lines. If this does not occur, align the dot using the centering rings on the yoke. See figure 5-1.

l. Turn OFF the logic analyzer and clean the CRT screen with mild soap and water.

m. Reconnect the two yoke connectors from the display driver.

n. Perform the Display Driver Adjustment Procedure.

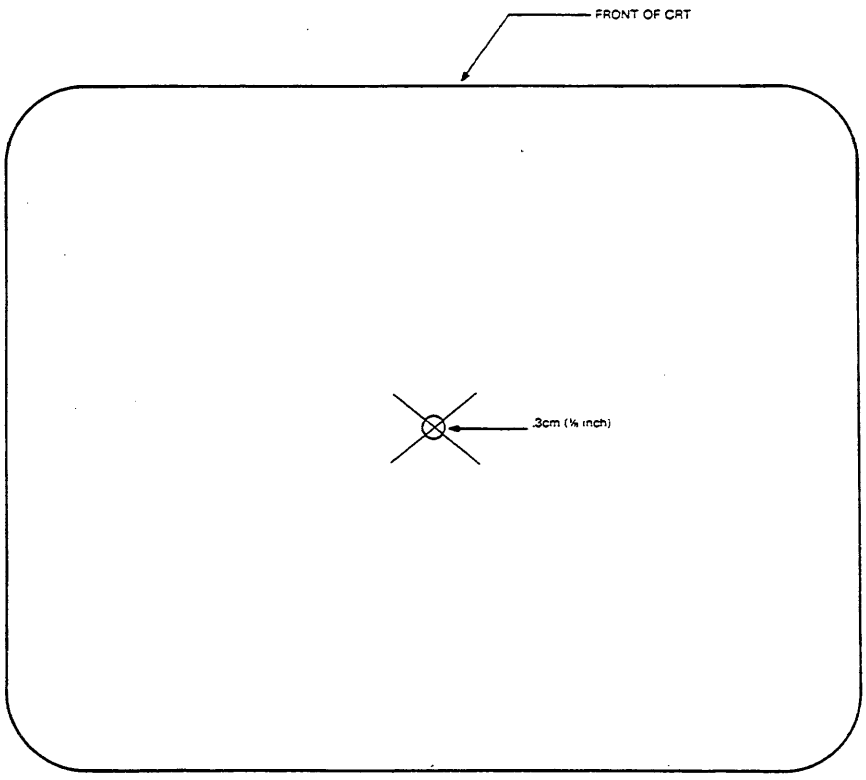


Figure 5-1. Yoke Centering Adjustment

DISPLAY DRIVER ADJUSTMENT PROCEDURE

a. Turn OFF the logic analyzer.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove cover.

c. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

d. Refer to the PROGRAM DISK LOADING PROCEDURE in Appendix A at the back of this manual.

e. Activate the Display Test Pattern as shown in figure 5-3 by pressing the < DISPLY > softkey on the Series 200 Controller.

f. Adjust the BRIGHTNESS control pot until the Display Test Pattern is visible. See figure 5-2 for the display adjustment locations.

g. Adjust the HEIGHT and VERT PHASE (position) until the Test Pattern meets the vertical measurements in figure 5-3.

NOTE

A non-metallic hex-type alignment tool is needed for adjustment of the HEIGHT coil. Use of a metal tool will result in a change in the setting when the tool is removed. Use of a blade-type tool could result in cracking of the adjustment slug.

h. Adjust HORIZ LINEARITY until the width of each square is the same.

i. Adjust HORIZ WIDTH until the Test pattern width is the same as the width shown in figure 5-3. Note that the pattern may no longer be centered within the edges of the CRT.

NOTE

The adjustments in steps (h) and (i) interact. Therefore reiteration of these two steps may be necessary for best results.

j. Now adjust the horizontal position by rotating the centering rings on the yoke. Adjust the rings for horizontal movement while minimizing the vertical movement of the pattern. Center the Test Pattern within the edges of the CRT.

k. Adjust VERT PHASE to vertically center the Test Pattern. This should only require minor adjustments.

l. The HOR HOLD adjustment has been pre-adjusted by the manufacturer and should not need to be changed.

m. The test pattern prompts you to press any key to call up the next display.

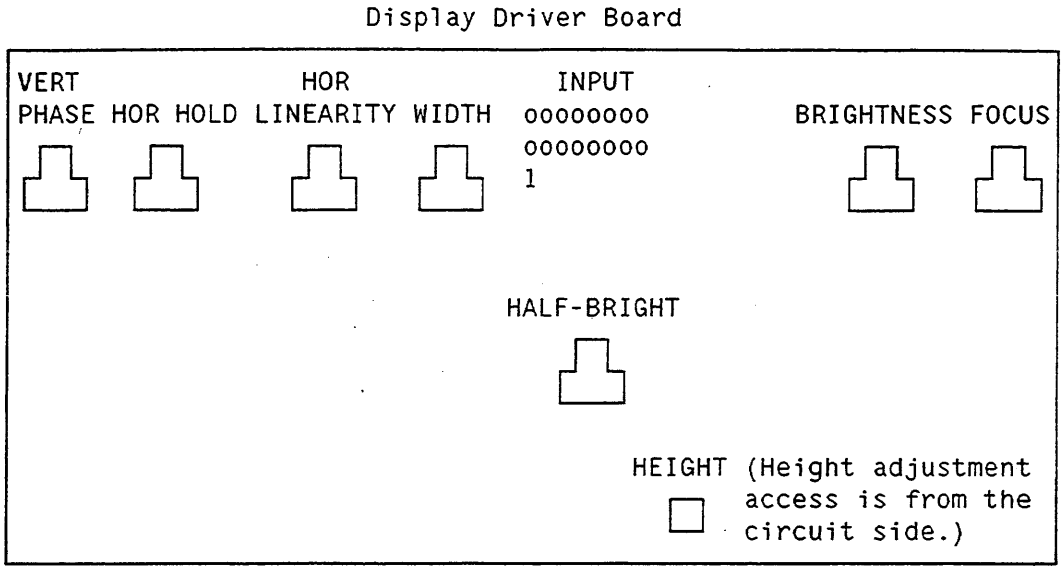


Figure 5-2. Display Adjustment Locations

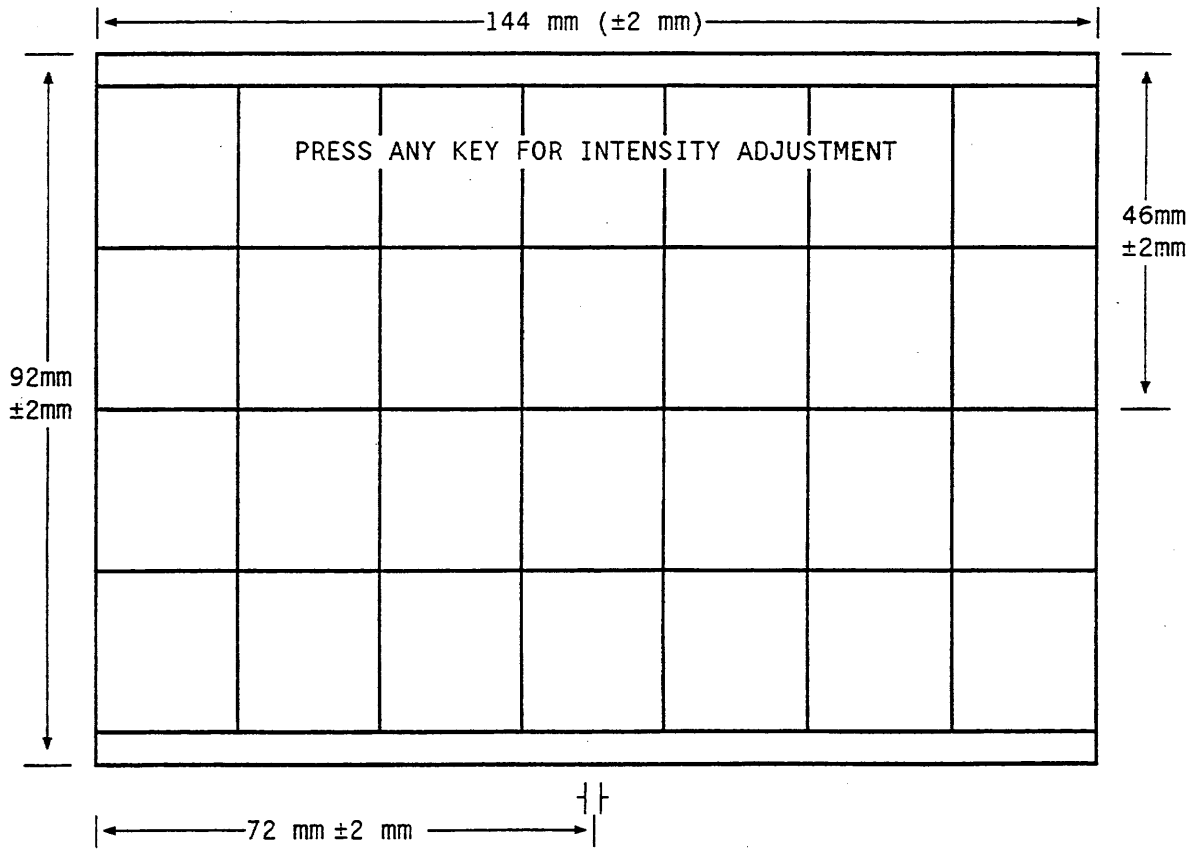


Figure 5-3. Display Size Test Pattern.

n. If a photometer is available, adjust the BRIGHTNESS control for a level of 39-41 foot Lamberts (133-140 CD/SQM) in the full-bright area of the display. Then, using the HALF-BRIGHT control, adjust the level of the half-bright area of the display to 19-21 foot Lamberts (65-72 CD/SQM).

NOTE

If you have an older instrument that does not have a HALF-BRIGHT adjustment (see figure 5-2) use the BRIGHTNESS control to adjust the brightness of the half-bright area of the display (see figure 5-4) for 19-21 foot lamberts (65-72 CD/SQM).

o. If a photometer is not available, adjust the BRIGHTNESS and FULL-BRIGHT controls for comfortable levels with good contrast between them.

p. Adjust FOCUS control to achieve the best display in the "FOCUS AREA" of the test pattern.

q. Verify that the "BLINKING CURSOR" area contains a blinking rectangular cursor, flashing between half-bright and full-bright several times per second. If the half-bright and full-bright areas of the display show the two different video levels, but the cursor does not blink, the CPU board is defective. If there are not two different video levels, the display board is defective. Refer to the CPU, Keyboard and Display Service Group 8B for troubleshooting information.

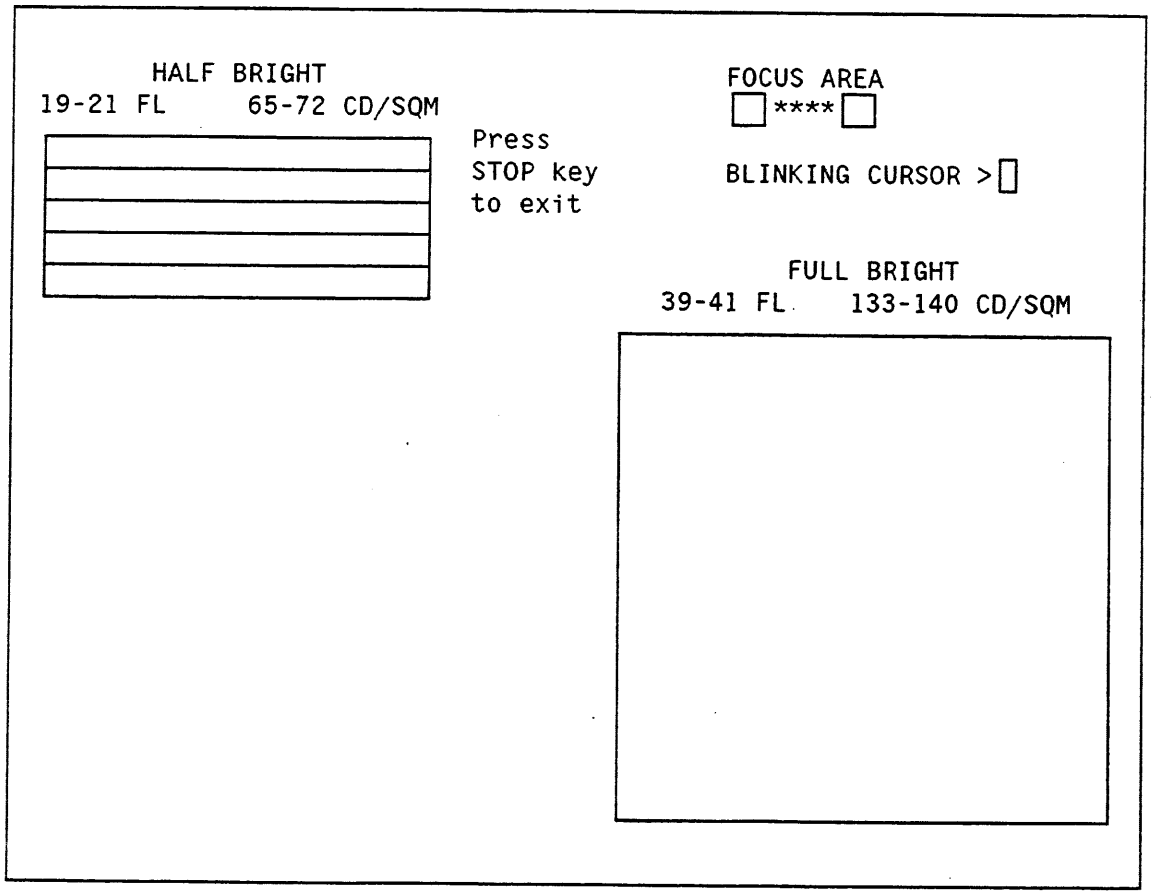


Figure 5-4. Display Brightness Test Pattern

5-6. TIMING MASTER ADJUSTMENT (200 MHz OSCILLATOR)

The Timing Master board may have an adjustment if the logic analyzer is an early model. If the Timing Master board part number is 01630-66506 or 01630-66510, the 200MHz oscillator uses discrete parts and may need adjustment. More recent boards, like the 01630-66524, use a "hybrid" oscillator which needs no adjustment.

NOTE

A portable fan must be used to maintain airflow across the macrocells.

a. Referring to the Acquisition Board Removal procedure in Section VIII, remove the Timing Master board A5.

NOTE

Service Note 1630A/D-2 addresses a change in the variable capacitor C26. See this Service Note to verify that the board has been properly re-worked.

b. With the power OFF, install the Timing Master board into the upright service connector J1. A probe doesn't need to be connected.

c. Connect Channel 1 of the oscilloscope to TP1 on the Timing Master board (located at the left-middle of the board). Set up the scope as follows:

Set Volts/div to .01 V/div
Set Time Base to 1 ns/div

d. Turn ON the logic analyzer and check for the presence of a 200 MHz signal at TP1.

e. If the 200 MHz signal doesn't exist, adjust trimcap C26 until a 200 MHz signal appears.

f. Continue adjusting trimcap C26 until the 200 MHz oscillation shows **MAXIMUM AMPLITUDE.**

g. Discontinue the oscillations by touching a screwdriver to the collector of the high-frequency transistor Q1. Remove the screwdriver and verify that the oscillator locks again to 200 MHz.

h. If the oscillations do not re-occur after being discontinued, adjust C26 until the oscillations begin again. Leave C26 at this setting and repeat step (g).

i. Adjustment complete. Replace board and covers.

5-7. STATE MASTER BOARD ADJUSTMENT

a. Referring to the Acquisition Board Removal procedure in Section VIII, remove the State Master board (A4).

b. With the power OFF, install the State Master board in the upright service connector J1.

c. DO NOT connect any state probes to the board. The Timing Master board must be installed.

d. Refer to the PROGRAM DISK LOADING PROCEDURE in Appendix A of this manual. Press the < Strobe > softkey on the 98XX controller.

e. The two scope probes required to perform the delay and width adjustments must be calibrated at the beginning of each calibration session to compensate for timing errors caused by different electrical lengths. This procedure will vary depending on the oscilloscope being used. Do this calibration before proceeding further.

   In many high frequency oscilloscopes this can be done by connecting both input probes to the same high frequency pulse and adjusting the scope to equalize the delay. If there is no delay equalization adjustment, note the difference in delay and take that into account during your measurements.

f. Connect Channel 1 of the oscilloscope to TP1 on the State Master board. Connect Channel 2 to TP2. Trigger the oscilloscope on the Channel 1 signal. The period of the signals is 5.5μs. By setting the oscilloscope controls to 0.5 V/div., 5.0 ns/div., and displaying both channels you should get approximately the display in figure 5-5. The adjustments to be made are shown on the figure. The adjustment accuracy is ±500 ps.

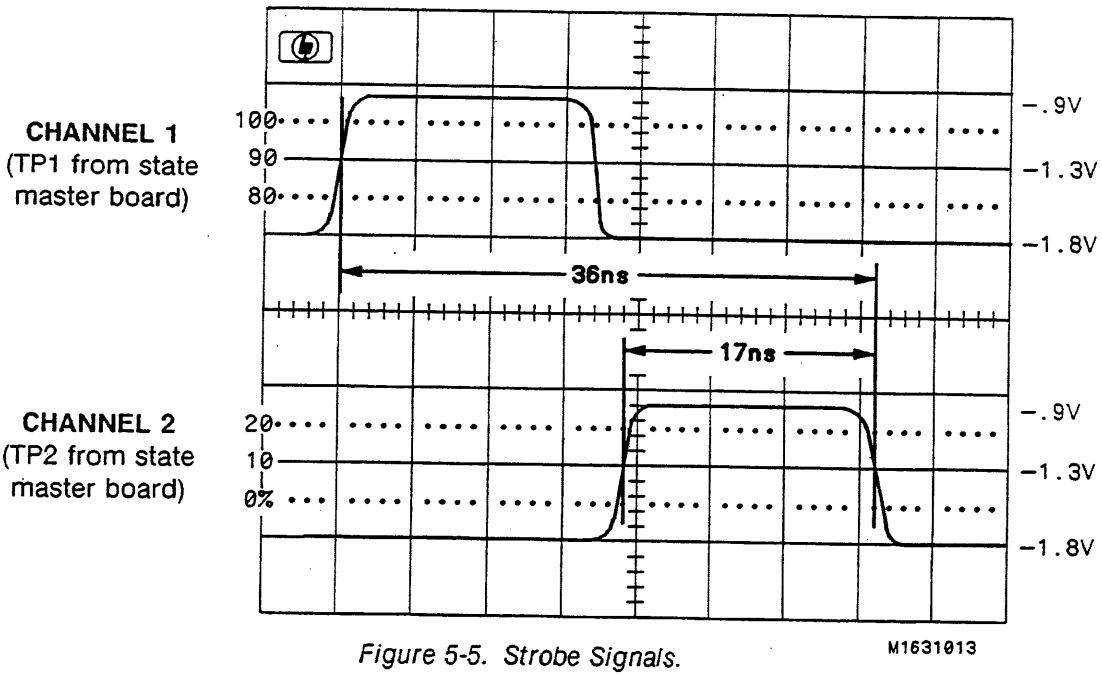


Figure 5-5. Strobe Signals.

The signals are ECL level waveforms. It is necessary to measure the timing of the signals at the -1.3V threshold level along the edges. To do this more easily, set a horizontal reference line of the oscilloscope to -1.3V by grounding both inputs of the scope, then setting the

baselines at the equivalent of 1.3V above the horizontal reference line. Now all timing measurements can be made along the horizontal reference.

NOTE

Different models of oscilloscope use different measurement techniques. To get the required measurement accuracy, use the measurement techniques appropriate to the model of oscilloscope you are using.

g. Adjust R4 to vary the pulse width of the signal at TP2. The adjustment is complete when the pulse width at TP2 is 17 ns ±500 ps at -1.3V.

h. Adjust R5 to vary the delay between the pulses at TP1 and TP2. The adjustment is complete when the delay between -1.3V on the rising edge at TP1 and -1.3V on the falling edge at TP2 is 36 ns ±500 ps.

5-8. STATE SLAVE BOARD ADJUSTMENT

a. Remove the State Slave Board. Removal procedures are in Section VIII.

b. With power OFF, install the State Slave board into the upright Service connector J1.

c. Place the intrument's top cover over the exposed power supply to prevent tools from dropping onto the power supply, and to maintain proper air flow.

d. Connect a DVM to TP1 and TPGND on the State Slave board under test.

e. Turn ON the 1630G.

f. Adjust trimpot R4 until the voltage at TP1 reads +5.00 volts +/-5 mV.

g. Adjustment complete. Replace board and covers.

5-9. ANALOG BOARD ADJUSTMENT

The Analog board <SKEW> adjustment requires an HP 8165A Programmable Signal Source to be installed on the HP-IB at address 716.

5-10. DAC Zero Adjustment

a. Refer to Appendix A for the PROGRAM DISK LOADING PROCEDURE and insert the Program Disk, then load the <ADJ1631> program.

b. The CRT screen on the 9826 or 9836 will direct the user with the proper procedure.

5-11. SKEW Adjustment

a. Refer to Appendix A for the PROGRAM DISK LOADING PROCEDURE and insert the Program Disk, then load the <SKEW> program.

b. The CRT screen on the 9826 or 9836 will direct the user with the proper procedure.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for ordering parts. Table 6-1 lists the abbreviations used in the parts list and throughout this manual. Figure 6-1 shows the locations of the mainframe mechanical parts (MP). Table 6-2 lists all replaceable parts for the 1631A/D. Table 6-3 contains the names and addresses that correspond to the manufacturers' code numbers.

6-2. ABBREVIATIONS

Table 6-1 lists abbreviations used in the parts list, the schematics, and elsewhere in this manual. In some cases two forms of the abbreviation are used, one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in the schematics and other parts of the manual, other abbreviation forms may be used with both lowercase and uppercase letters.

6-3. PARTS LIST

Table 6-2 is a list of replaceable parts and is organized as follows:

a. Mainframe parts are listed first, by reference designator.

b. Following that, individual assemblies are listed, again in reference designator order, with the components of each assembly listed in reference designator order.

c. If an assembly has more than one part number because it has been changed, all part numbers for that assembly are listed within the assembly group, in part number order. Individual part information distinguishing an assembly part number is given with it, in reference designator order.

The information given for each part consists of the following:

a. Hewlett-Packard part number and the check digit (for HP internal use).

b. Total quantity (Qty) on each assembly.

c. Description of the part.

d. A typical manufacturer of a given part in a five digit code. Refer to table 6-3 for a code to manufacturer breakdown.

e. The manufacturer's number for the part.

The total quantity for each part is given only once, at the first appearance of the part number in the list.

6-4. ORDERING INFORMATION

To order a part listed in the replaceable parts list, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the replaceable parts table, include the instrument serial number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-5. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

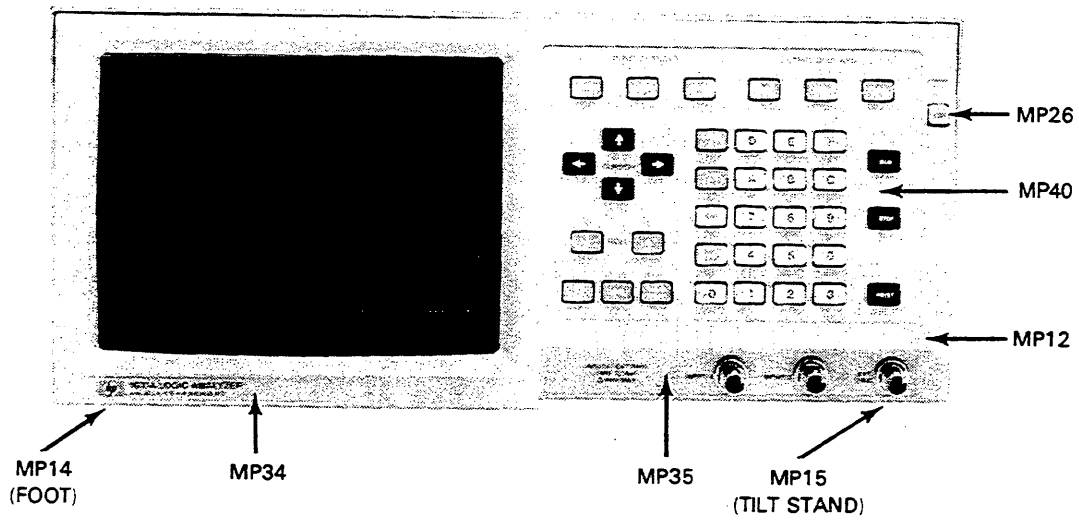
Table 6-1. Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	=assembly
B	=fan;motor
BT	=battery
C	=capacitor
CR	=diode;diode thyristor; varactor
DL	=delay line
DS	=annunciator;lamp;LED
E	=misc. electrical part
F	=fuse
FL	=filter
H	=hardware
J	=electrical connector (stationary portion);jack
L	=coil;inductor
MP	=misc. mechanical part
P	=electrical connector (moveable portion);plug
Q	=transistor;SCR; triode thyristor
R	=resistor
RT	=thermistor
S	=switch;jumper
T	=transformer
TB	=terminal board
TP	=test point
U	=integrated circuit; microcircuit
V	=electron tube; glow lamp
VR	=voltage regulator; breakdown diode
W	=cable
X	=socket
Y	=crystal unit(piezo-electric or quartz)

ABBREVIATIONS

A	=amperes
A/D	=analog-to-digital
AC	=alternating current
ADJ	=adjust(ment)
AL	=aluminum
AMPL	=amplifier
ANLG	=analog
ANSI	=American National Standards Institute
ASSY	=assembly
ASTIG	=astigmatism
ASYNCHRO	=asynchronous
ATTEN	=attenuator
AWG	=American wire gauge
BAL	=balance
BCD	=binary-code decimal
BD	=board
BFR	=buffer
BIN	=binary
BRDG	=bridge
BSHG	=bushing
BW	=bandwidth
C	=ceramic;cermet (resistor)
CAL	=calibrate;calibration
CC	=carbon composition
CCW	=counterclockwise
CER	=ceramic
CFM	=cubic feet/minute
CH	=choke
CHAM	=chamfered
CHAN	=channel
CHAR	=character
CM	=centimeter
CMOS	=complementary metal-oxide-semiconductor
CMR	=common mode rejection
CNDCT	=conductor
CNTR	=counter
CON	=connector
CONT	=contact
CRT	=cathode-ray tube
CW	=clockwise
D	=diameter
D/A	=digital-to-analog
DAC	=digital-to-analog converter
DARL	=darlington
DAT	=data
DBL	=double
DBM	=decibel referenced to 1mW
DC	=direct current
DCDR	=decoder
DEG	=degree
DEMUX	=demultiplexer
DET	=detector
DIA	=diameter
DIP	=dual in-line package
DIV	=division
DMA	=direct memory access
DPDT	=double-pole, double-throw
DRC	=DAC refresh controller
DRVR	=driver
DWL	=dowel
ECL	=emitter coupled logic
ELAS	=elastomeric
EXT	=external
F	=farads;metal film (resistor)
FC	=carbon film/ composition
FD	=feed
FEM	=female
FF	=flip-flop
FL	=flat
FM	=from;from
FR	=front
FT	=gain bandwidth product
FW	=full wave
FXD	=fixed
GEN	=generator
GND	=ground(ed)
GP	=general purpose
GRAT	=graticule
GRV	=groove
H	=henries;high
HD	=hardware
HDND	=hardened
HG	=mercury
HGT	=height
HLCL	=helical
HORIZ	=horizontal
HP	=Hewlett-Packard
HP-IB	=Hewlett-Packard Interface Bus
HR	=hour(s)
HV	=high voltage
HZ	=Hertz
I/O	=input/output
IC	=integrated circuit
ID	=inside diameter
IN	=inch
INCL	=include(s)
INCAND	=incandescent
INP	=input
INTEN	=intensity
INTL	=internal
INV	=inverter
JFET	=junction field-effect transistor
JKT	=jacket
K	=kilo(10^3)
L	=low
LB	=pound
LCH	=latch
LCL	=local
LED	=light-emitting diode
LG	=long
LI	=lithium
LK	=lock
LKWR	=lockwasher
LS	=low power Schottky
LV	=low voltage
M	=mega(10^6);megohms; meter(distance)
MACH	=machine
MAX	=maximum
MFR	=manufacturer
MICPROC	=microprocessor
MINTR	=miniature
MISC	=miscellaneous
MLD	=molded
MM	=millimeter
MO	=metal oxide
MTG	=mounting
MTLC	=metallic
MUX	=multiplexer
MW	=milliwatt
N	=nano(10^{-9})
NC	=no connection
NMOS	=n-channel metal-oxide-semiconductor
NPN	=negative-positive-negative
NPRN	=neoprene
NRFR	=not recommended for field replacement
NSR	=not separately replaceable
NUM	=numeric
OBD	=order by description
OCTL	=octal
OD	=outside diameter
OP AMP	=operational amplifier
OSC	=oscillator
P	=plastic
P/O	=part of
PC	=printed circuit
PCB	=printed circuit board
PD	=power dissipation
PF	=picofards
PI	=plug in
PL	=plate(d)
PLA	=programmable logic array
PLST	=plastic
PNP	=positive-negative-positive
POLYE	=polyester
POS	=positive;position
POT	=potentiometer
POZI	=pozidrive
PP	=peak-to-peak
PPM	=parts per million
PRCN	=precision
PREAMP	=preamplifier
PRGMBL	=programmable
PRL	=parallel
PROG	=programmable
PSTN	=position
PT	=point
PW	=potted wirewound
PWR	=power
R-S	=reset-set
RAM	=random-access memory
RECT	=rectifier
RET	=retainer
RF	=radio frequency
RGLTR	=regulator
RGTR	=register
RK	=rack
RMS	=root-mean-square
RND	=round
ROM	=read-only memory
RPG	=rotary pulse generator
RX	=receiver
S	=Schottky-clamped; seconds(time)
SCR	=screw;silicon controlled rectifier
SEC	=second(time);secondary
SEG	=segment
SEL	=selector
SGL	=single
SHF	=shift
SI	=silicon
SIP	=single in-line package
SKT	=skirt
SL	=slide
SLDR	=solder
SLT	=slot(ted)
SOLD	=solenoid
SPCL	=special
SQ	=square
SREG	=shift register
SRQ	=service request
STAT	=static
STD	=standard
SYNCHRO	=synchronous
TA	=tantalum
TBAX	=tubeaxial
TC	=temperature coefficient
TD	=time delay
THD	=thread(ed)
THK	=thick
THRU	=through
TP	=test point
TPG	=tapping
TPL	=triple
TRANS	=transformer
TRIG	=trigger(ed)
TRMR	=trimmmer
TRN	=turn(s)
TTL	=transistor-transistor
TX	=transmitter
U	=micro(10^{-6})
UL	=Underwriters Laboratory
UNREG	=unregulated
VA	=voltampere
VAC	=volt.ac
VAR	=variable
VCO	=voltage-controlled oscillator
VDC	=volt.dc
VERT	=vertical
VF	=voltage.filtered
VS	=versus
W	=watts
W/	=with
W/O	=without
WW	=wirewound
XSTR	=transistor
ZNR	=zener
°C	=degree Celsius (Centigrade)
°F	=degree Fahrenheit
°K	=degree Kelvin



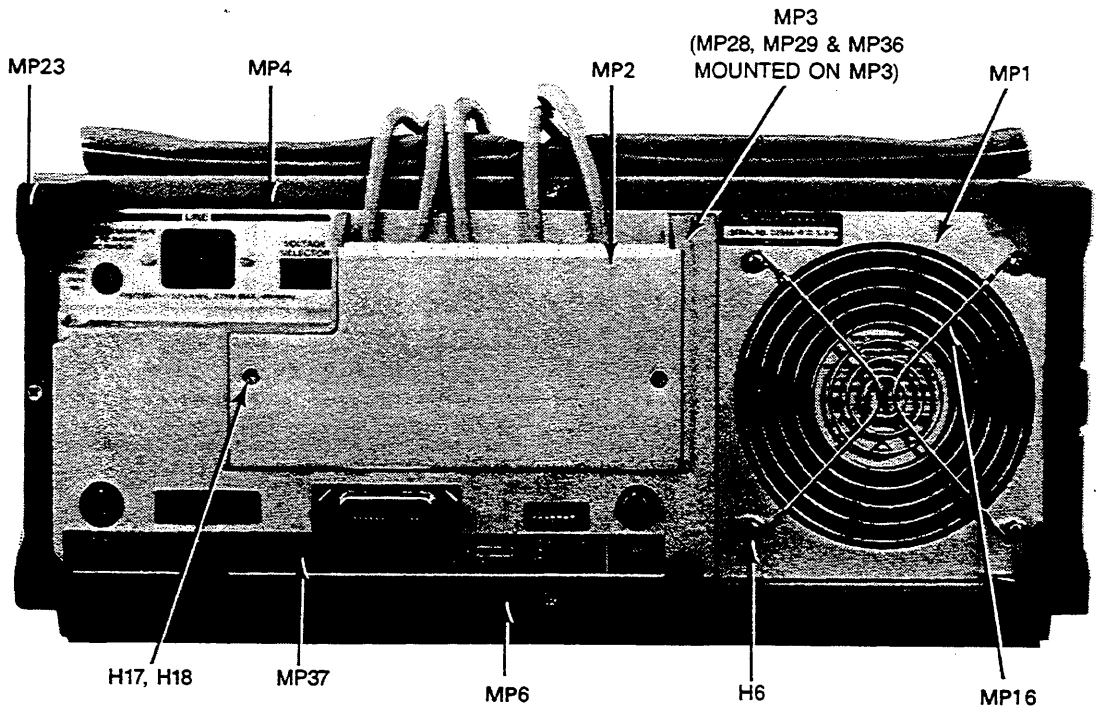
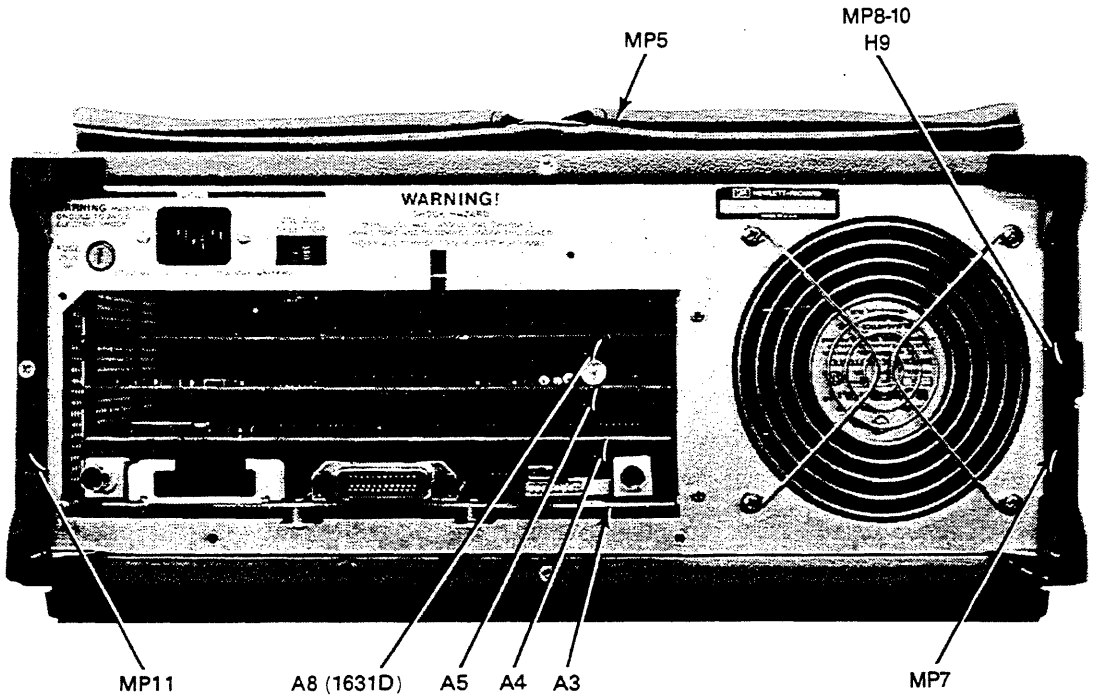


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 1 of 4)



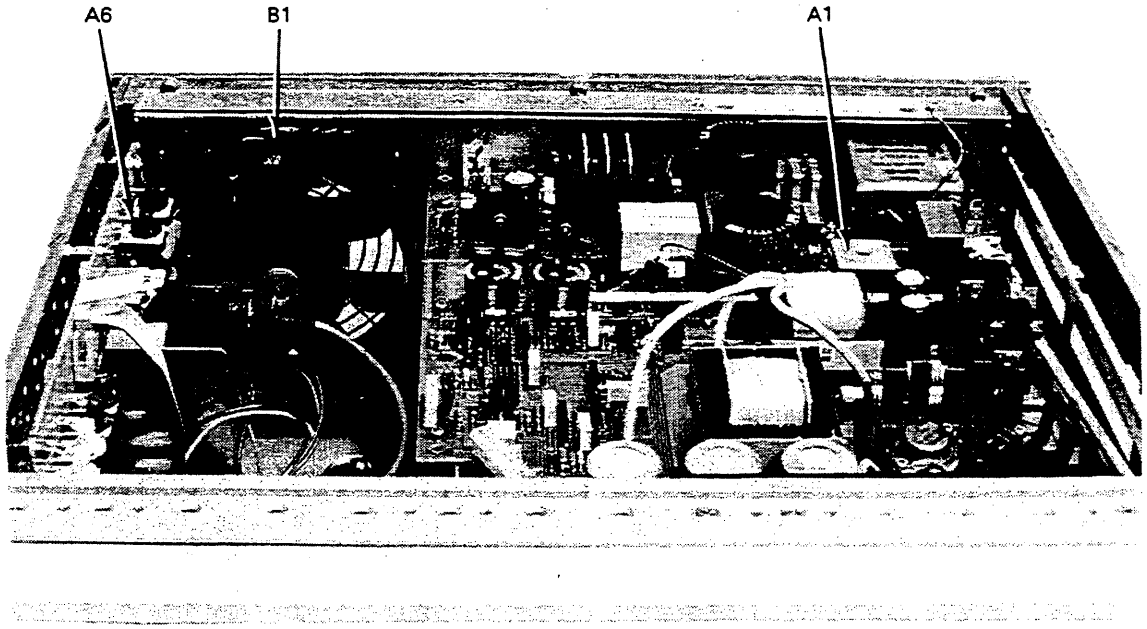
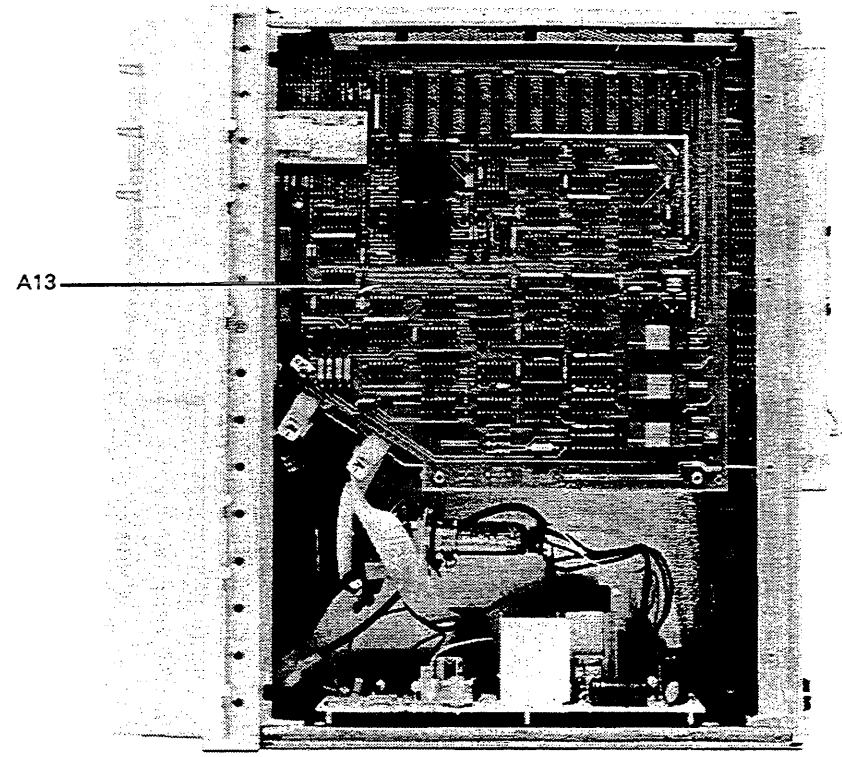


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 2 of 4)



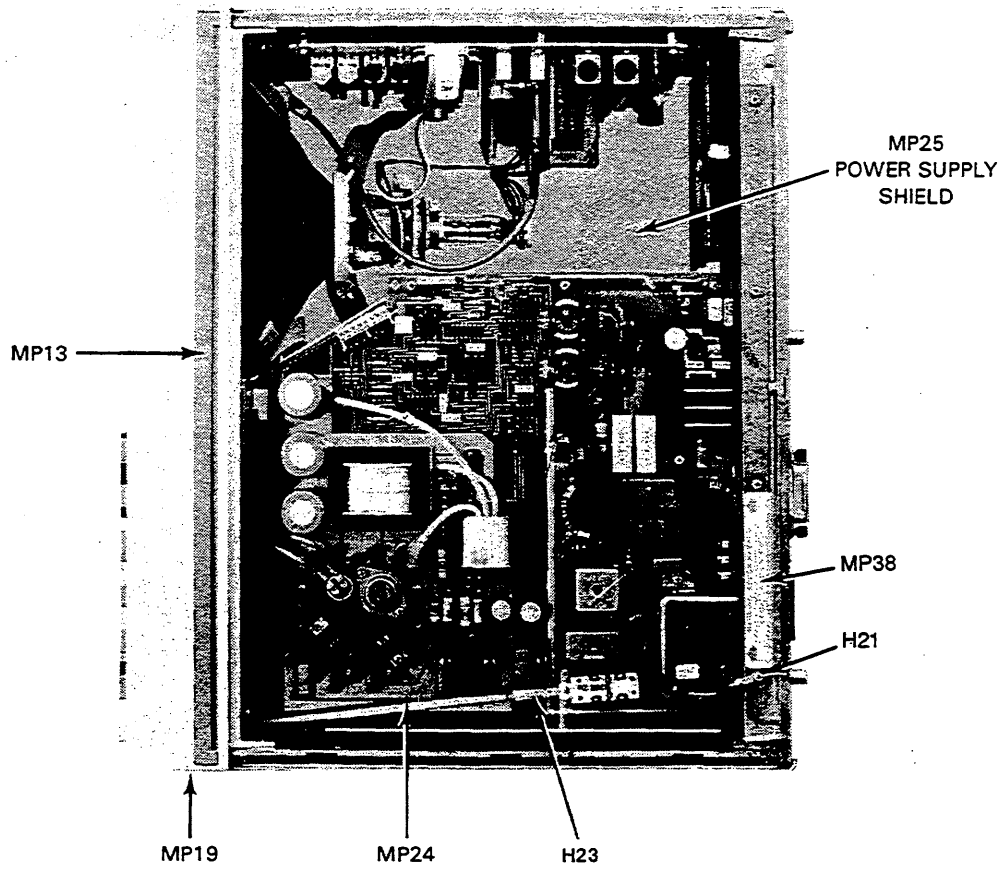


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 3 of 4)

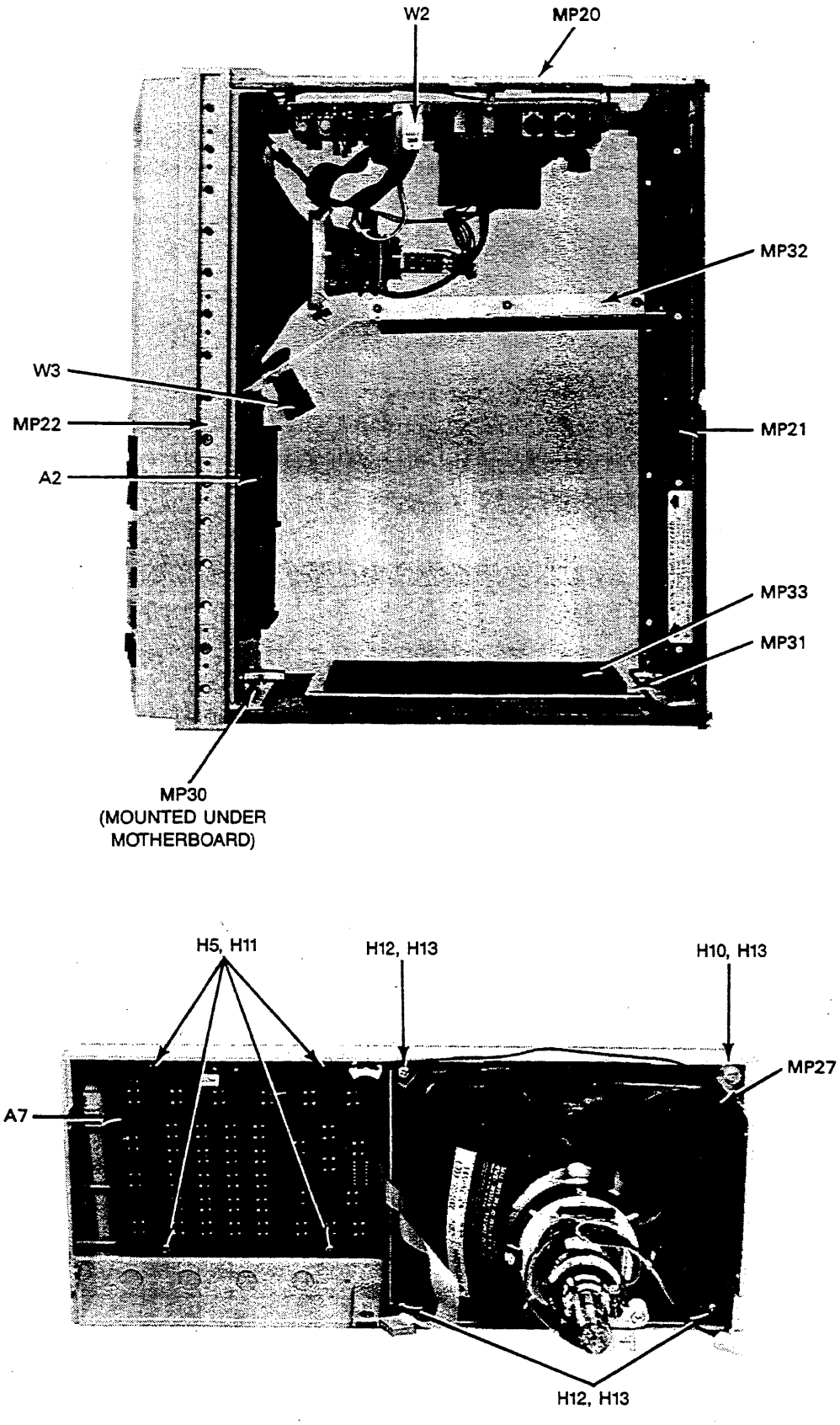


Figure 6-1. Mainframe Mechanical Parts Locations (sheet 4 of 4)

Table 6-2. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	1630A/D/G			PARTS AND HARDWARE FOR NON-METRIC MAINFRAMES WITH SERIAL PREFIXES BEFORE 2511A (1630A/D) 2510A (1630G) 2509A (1631A) 2510A (1631D)		
H7	2360-0195	0	8	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H8	2510-0192	6	16	SCREW-MACH 8-32 .25-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H9	2680-0172	1	2	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H19	0570-1171	7	3	SCREW-COVER MOUNTING 6-32	28480	0570-1171
H20	0510-0043	4	2	RETAINING RING-TOP, BOTTOM COVER MTG	28480	0510-0043
MP4	01630-04104	3	1	TOP COVER (Obsolete, see Section 7)	28480	01630-04104
MP6	5060-9845	2	1	BOTTOM COVER	28480	5060-9845
MP9	5040-7219	8	1	CAP-STRAP HANDLE (FRONT)	28480	5040-7219
MP10	5040-7220	1	1	CAP-STRAP HANDLE (REAR)	28480	5040-7220
MP11	5060-9915	7	1	COVER-SIDE PERFORATED	28480	5060-9915
MP20	5020-8835	4	4	STRUT-CORNER	28480	5020-8835
MP21	5020-8806	9	1	FRAME-REAR	28480	5020-8806
MP22	5020-8805	8	1	FRAME-FRONT	28480	5020-8805
	1630A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2242A & 2311A (1630A) 2234A & 2311A (1630D) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
A3	01630-66515	0	1	CPU BOARD	28480	01630-66515
B1	3160-0252	7	1	FAN 128V 50/60-HZ	28480	3160-0252
MP1	01630-00201	3	1	PANEL-REAR	28480	01630-00201
MP2	01630-04102	1	1	COVER PROBE CONNECTOR	28480	01630-04102
MP3	01630-44101	4	1	COVER CARD CAGE	28480	01630-44101
MP4	01630-04101	0	1	TOP COVER	28480	01630-04101
MP5	1540-0807	2	1	POUCH (MP2-MP5 are obsolete, see Section 7)	28480	1540-0807
W5	01630-61603	7	1	CABLE-FAN	28480	01630-61603
	1630A/D/G			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2412A (1630A/D) 2415A (1630G) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
A3	01630-66515	0	1	CPU BOARD (1630A/D)	28480	01630-66515
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1630A/D/G			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2428A (1630A) 2424A (1630D) 2425A (1630G) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
A3	01630-66515	0	1	CPU BOARD (1630A/D)	28480	01630-66515
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2451A & 2505A (1631A) 2446A & 2503A (1631D) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	1630A/D 1630G			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX: 2511A (1630A/D) 2510A (1630G) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2509A (1631A) 2510A (1631D) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1630A/D/G 1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2515A (1630A) 2514A (1630D) 2525A (1631A) 2518A (1631D) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1631A			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX: 2540A (1631A) ARE THE SAME AS THE CURRENT LIST WITH THE FOLLOWING EXCEPTIONS		
B1	3160-0428	9	1	FAN 120/240V 50/60-HZ	28480	3160-0428
	1630A/D/G 1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2605A (1630A) 2602A (1630D) 2602A (1630G) 2605A (1631A) 2551A (1631D) ARE THE SAME AS THE CURRENT LIST		
	1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIX: 2645A (1631A) 2641A (1631D) ARE THE SAME AS THE CURRENT LIST		
	1630A/D/G 1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2715A (1630A) 2720A (1630D) 2602A (1630G) 2714A (1631A) 2713A (1631D) ARE THE SAME AS THE CURRENT LIST		

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				CURRENT PARTS LIST, 1630A/D/G, 1631A/D (* DENOTES METRIC FRAME PARTS-SEE BEGINNING OF PARTS LIST)		
	1630A/D/G 1631A/D			MAINFRAME ASSEMBLIES/PARTS FOR SERIAL PREFIXES: 2812A (1630A) 2812A (1630D) 2812A (1630G) 2811A (1631A) 2811A (1631D)		
A1	01630-66534	3	1	POWER SUPPLY BOARD (see Section 7 AND/OR APPROPRIATE SERVICE NOTE)	28480	01630-66534
A2	01630-66501	4	1	MOTHER BOARD	28480	01630-66501
A3	01630-66535	4	1	CPU BOARD (1630A/D, 1631A/D)	28480	01630-66535
A3	01630-66526	3	1	CPU BOARD (1630G)	28480	01630-66528
A3	01630-66515	0	1	CPU BOARD (1630A/D OPTION 007)	28480	01630-66515
A4	01630-66518	3	1	STATE MASTER BOARD	28480	01630-66518
A5	01630-66524	1	1	TIMING MASTER BOARD	28480	01630-66524
A6	0950-1692	3	1	DISPLAY BOARD ASSEMBLY	28480	0950-1692
A7	01630-66530	9	1	KEYBOARD (INCLUDES CABLE)	28480	01630-66530
A8	01630-66508	1	1	TIMING SLAVE BOARD (1630/31D)	28480	01630-66508
A9	10271A	6	3	STATE MASTER PROBE	28480	10271A
A10	10272A	7	AR	TIMING PROBE(1630/31A/30G-1, 1630/31D-2)	28480	10272A
A11	01630-66517	2	1	STATE SLAVE BOARD (1630G)	28480	01630-66517
A12	10273A	8	3	STATE SLAVE PROBE (1630G)	28480	10273A
A13	01631-66501	5	1	ANALOG ACQUISITION BOARD (1631A/D)	28480	01631-66501
A14	10435A	4	2	PROBE 10:1 DIVIDER (1631A/D)	28480	10435A
B1	3160-0521	3	1	FAN 12VDC	28480	3160-0521
E1	1250-1454	2	1	CONNECTOR/ADAPTER BNC TO PROBE (1631A/D)	28480	1250-1454
H1	0515-0430	3	25	SCREW-MACH M3 6MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
H2	0515-0943	3	13	SCREW-MACH M4 12MM-LG FLAT-HD TORX	00000	ORDER BY DESCRIPTION
H3	0515-0374	4	11	SCREW-MACH M3 10MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
H4	0515-0641	8	2	SCREW-TPG M4 10MM-LG TAPPING	00000	ORDER BY DESCRIPTION
H5	0624-0520	2	4	SCREW-TPG 6-19 .5IN-LG PAN-HD (KBRD MTG)	00000	ORDER BY DESCRIPTION
H6	0624-0644	2	4	SCREW-TPG 8-32 .75IN-LG PAN-HD (FAN MTG)	00000	ORDER BY DESCRIPTION
H7	0515-1402*	1	4	SCREW-MACH M3.5 8MM-LG PAH-HD TORX	00000	ORDER BY DESCRIPTION
H8	0515-1403*	2	16	SCREW-MACH M4 6MM-LG FLAT-HD TORX	00000	ORDER BY DESCRIPTION
H9	0515-1384*	8	2	SCREW-MACH M5 10MM-LG FLAT-HD TORX	00000	ORDER BY DESCRIPTION
H10	3050-0002	2	1	WASHER-FL MTLC NO. 10 .203-IN-ID	28480	3050-0002
H11	3050-0003	3	4	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H12	3050-0006	6	3	WASHER-SHLDR NO. 10 .5-IN-OD	28480	3050-0006
H13	0624-0598	5	4	SCREW-TPG 8-16 .625IN-LG PAN-HD (CRT MTG)	00000	ORDER BY DESCRIPTION
H14	2420-0001	5	4	FASTENING NUT-HEX (FAN-OLDER INST.)	28480	2420-0001
H15	0590-1611	2	3	NUT-KNURLED 1/2-28 (1631A/D)	28480	0590-1611
H16	3050-1016	0	3	WASHER-FLAT .5ID .625OD (1631A/D)	28480	3050-1016
H17	0570-1171	7	2	SCREW-PROBE CONNECTOR COVER 6-32	28480	0570-1171
H18	0510-0043	4	2	RETAINING RING-PROBE CONNECTOR COVER	28480	0510-0043
H19	0515-1245*	0	3	SCREW-COVER MOUNTING M3.5 12MM-LG	28480	0515-1245
H20	0510-1253*	0	3	RETAINING RING-COVER MOUNTING SCREW	28480	0510-1253
H21	0515-0433	6	1	SCREW-MACH M4 8MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
H22	0515-0380	2	6	SCREW-MACH M4 10MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
H23	01830-23201	3	1	COUPLER - SWITCH EXTENTION	28480	01830-23201
L1	9140-0720	8	1	DEFLECTION YOKE	28480	9140-0720
MP1	01630-00203	5	1	PANEL-REAR	28480	01630-00203
MP2	01630-64103	8	1	COVER PROBE CONNECTOR	28480	01630-64103
MP3	01630-44102	5	1	COVER CARD CAGE	28480	01630-44102
MP4	01630-04105*	4	1	TOP COVER	28480	01630-04105
MP5	01630-84501	2	1	POUCH	28480	01630-84501
MP6	5061-9445*	0	1	BOTTOM COVER	28480	5061-9445
MP7	5060-9882	7	1	COVER-SIDE	28480	5060-9882
MP8	5060-9802	1	1	STRAP HANDLE 12 INCH	28480	5060-9802
MP9	5041-6819*	4	1	CAP-STRAP HANDLE (FRONT)	28480	5041-6819
MP10	5041-6820*	7	1	CAP-STRAP HANDLE (REAR)	28480	5041-6820
MP11	5061-9515*	5	1	COVER-SIDE PERFORATED	28480	5061-9515
MP12	7101-0694	1	1	BEZEL-FRONT	28480	7101-0694
MP13	5040-7202	9	1	TRIM STRIP-TOP	28480	5040-7202
MP14	5040-7201	8	4	FEET	28480	5040-7201
MP15	1460-1345	5	2	TILT STAND	28480	1460-1345

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP16	3160-0092	3	1	FAN GUARD	28480	3160-0092
MP17				NOT USED		
MP18				NOT USED		
MP19	5001-0440	1	2	TRIM STRIP-SIDE	28480	5001-0440
MP20	5021-5835*	0	4	STRUT-CORNER	28480	5021-5835
MP21	5021-5806*	5	1	FRAME-REAR	28480	5021-5806
MP22	5021-5805*	4	1	FRAME-FRONT	28480	5021-5805
MP23	5040-7221	2	4	STANDOFF-REAR PANEL (REAR FOOT)	28480	5040-7221
MP24	5041-3170	4	1	SWITCH SHAFT	28480	5041-3170
MP25	01630-00601	7	1	SHIELD-POWER SUPPLY-PLASTIC	28480	01630-00601
MP26	5041-2799	1	1	KEYCAP-LINE	28480	5041-2799
MP27	0360-2109	8	1	GROUND LUG	28480	0360-2109
MP28	8160-0486	4	8	RFI STRIP-FINGERS BE-CU ZINC PLATED	28480	8160-0486
MP29	0403-0179	0	3	BUMPER FOOT-ADHESIVE MOUNTING	28480	0403-0179
MP30	54201-01201	7	1	BRACKET-MOTHER BOARD	28480	54201-01201
MP31	01630-01202	6	1	BRACKET CARD GUIDE	28480	01630-01202
MP32	01630-01203	7	1	BRACKET CENTER GUIDE	28480	01630-01203
MP33	0403-0512	5	10	PC CARD GUIDE	28480	0403-0512
MP34	7121-3936	2	1	LABEL-IDENTIFICATION (1630A)	28480	7121-3936
MP34	7121-3934	0	1	LABEL-IDENTIFICATION (1630D)	28480	7121-3934
MP34	01630-94306	5	1	LABEL-IDENTIFICATION (1630G)	28480	01630-94306
MP34	01631-94302	3	1	LABEL-IDENTIFICATION (1631A)	28480	01631-94302
MP34	01631-94301	2	1	LABEL-IDENTIFICATION (1631D)	28480	01631-94301
MP35	7121-3935	1	1	LABEL-BLANK (1630A/D/G)	28480	7121-3935
MP35	54200-94301	2	1	LABEL-ANALOG INPUT (1631A/D)	28480	54200-94301
MP36	01630-94305	5	1	LABEL-PROBE CONNECTOR LOCATIONS	28480	01630-94305
MP37	7121-3658	5	1	LABEL HP-IB HP-IL ETC.	28480	7121-3658
MP38	7121-3659	6	1	LABEL-POWER SUPPLY WARNING	28480	7121-3659
MP39	7121-4002	5	1	LABEL-CRT CAUTION	28480	7121-4002
MP40	7121-4026	3	1	LABEL-KEYBOARD	28480	7121-4026
V1	2090-0066	1	1	TUBE-CRT	28480	2090-0066
W1	8120-1521	6	1	POWER CORD 115V USA/CANADA	28480	8120-1521
W1	8120-1703	6	1	POWER CORD OPTION 900 UNITED KINGDOM	28480	8120-1703
W1	8120-0696	4	1	POWER CORD OPTION 901 AUST/NEW ZEALAND	28480	8120-0696
W1	8120-1692	2	1	POWER CORD OPTION 902 EUROPEAN CONTINENT	28480	8120-1692
W1	8120-2296	4	1	POWER CORD OPTION 906 SWITZERLAND	28480	8120-2296
W1	8120-2957	4	1	POWER CORD OPTION 912 DENMARK	28480	8120-2957
W1	8120-4600	8	1	POWER CORD OPTION 917 SOUTH AFRICA	28480	8120-4600
W1	8120-4754	3	1	POWER CORD OPTION 918 JAPAN	28480	8120-4754
W2	8120-3785	8	1	CABLE DISPLAY-16	28480	8120-3785
W3	8120-3784	7	1	CABLE KEYBD-14 (FOR KEYBD WITHOUT CABLE)	28480	8120-3784
W4	82167-60002	6	1	CABLE HP-IL INTERFACE	28480	82167-60002

(* DENOTES METRIC FRAME PARTS-SEE BEGINNING OF PARTS LIST)

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01630-66502	5	1	POWER SUPPLY ASSEMBLY SAME AS 01630-66529 WITH THE FOLLOWING EXCEPTIONS: DELETE R43, TP3	28480	01630-66502
A1E1				SEE SECTION 7 OR SERVICE NOTES		
A1E2				SEE SECTION 7 OR SERVICE NOTES		
A1MP8	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1P2	1251-7826	6	2	CONNECTOR-MALE	28480	1251-7826
A1R37	0757-0459	8	2	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1RT1				SEE SECTION 7 OR SERVICE NOTES		
A1RT2				SEE SECTION 7 OR SERVICE NOTES		
A1	01630-66514	9	1	POWER SUPPLY ASSEMBLY SAME AS 01630-66529 WITH THE FOLLOWING EXCEPTIONS: DELETE R43	28480	01630-66514
A1E1				SEE SECTION 7 OR SERVICE NOTES		
A1E2				SEE SECTION 7 OR SERVICE NOTES		
A1MP8	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1P2	1251-7826	6	2	CONNECTOR-MALE	28480	1251-7826
A1R37	0757-0459	8	2	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1RT1				SEE SECTION 7 OR SERVICE NOTES		
A1RT2				SEE SECTION 7 OR SERVICE NOTES		
A1	01630-66525	2	1	POWER SUPPLY ASSEMBLY SAME AS 01630-66529 WITH THE FOLLOWING EXCEPTIONS: DELETE R43	28480	01630-66525
A1P2	1251-7826	6	2	CONNECTOR-MALE	28480	1251-7826
A1R37	0757-0459	8	2	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
				The parts list for 01630-66534 and later boards is located in a separate list that follows this one.		
A1	01630-66529	6	1	POWER SUPPLY ASSEMBLY	28480	01630-66529
A1C1	0180-0291	3	14	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C2	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C3	0180-2946	9	3	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1C4	0160-5473	1	10	CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C5	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C6	0160-5347	8	3	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C7	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C8	0140-0180	5	7	CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C9	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C10	0180-3224	8	2	CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C11	0180-3224	8		CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C12	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1C13	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
A1C14	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C15	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C16	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C17	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C18	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C19	0140-0199	6	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A1C20	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C21	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C22	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C23	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C24	0160-0164	7	3	CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C25	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C26	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C27	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C28	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C29	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C30	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C31	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C32	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C33	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C34	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 3000VDC MICA	72136	DM19F202G0300WV1CR
A1C35	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C36	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C37	0160-2202	8	1	CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A1C38	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C39	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C40	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C41	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C42	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C43	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C44	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C45	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C46	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C47	0180-3046	2	3	CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C48	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C49	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1CR1	1906-0006	9	1	DIODE-FW BRDG 400V 1A	18546	VE48
A1CR2	1901-0719	1	2	DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A1CR3	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A1CR4	1906-0224	3	1	DIODE-FW BRDG 600V 25A	04713	MDA2506
A1CR5	1901-0028	5	1	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1CR6	1901-0050	3	10	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR10	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A1CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR15	1906-0079	6	1	DIODE-FW BRDG 100V 10A	18546	VJ148X
A1CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR18	1906-0239	0	1	DIODE-CT-RECT 45V 30A	01281	SD-241
A1CR19	1906-0263	0	1	RFCT VSK 12	28480	1906-0263
A1CR20	1906-0262	9	1	RECT USE 2402	28480	1906-0262
A1DS1	1990-0652	8	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
A1E1				NOT ASSIGNED		
A1E2				NOT ASSIGNED		
A1E3	2110-0642	3	1	FUSEHOLDER	28480	2110-0642
A1E4	2110-0565	9	1	FUSEHOLDER CAP	28480	2110-0565
A1E5	0340-0884	0	1	INSULATOR XISTOR THERMAL CONDUCTIVE TO3	28480	0340-0884
A1E6	0340-0949	8	8	INSULATOR XISTOR THERMAL CONDUCTIVE	28480	0340-0949
A1F1	2110-0056	3	1	FUSE 6A 250V NTD 1.25X.25 UL IEC	75915	312006
A1FL1	9135-0175	6	1	FILTER-LINE	28480	9135-0175
A1H1	01830-23201	3	1	COUPLER-SW EXTN	28480	01830-23201
A1H2	0403-0285	9	1	BUMPER FOOT-ADHESIVE MOUNTING	28480	0403-0285
A1H3	0515-0372	2	12	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A1H4	0515-1025	4	1	SCREW-MACH M3 X 0.5 26MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A1H5				NOT ASSIGNED		
A1H6	2190-0005	0	12	WASHER-LK EXT T NO. 4 .116-IN-ID	28480	2190-0005
A1H7	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A1H8	3050-0003	3	1	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
A1L1	9140-0624	1	1	INDUCTOR 270UH 10% .725DX.818LG	28480	9140-0624
A1L2	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192
A1MP1	1205-0490	9	3	HEAT SINK 6022BS	28480	1205-0490
A1MP2				NOT ASSIGNED		
A1MP3	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1MP4	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP5	1600-1330	6	1	STIFFENER-PCB	28480	1600-1330
A1MP6	1205-0489	6	3	HEAT SINK 6021BS	28480	1205-0489
A1MP7	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP8	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP9	1205-0486	3	1	HEAT SINK	28480	1205-0486
A1Q1	1854-0827	1	2	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1Q2	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1P1	1251-7986	9	1	CONNECTOR-50 CONTACT (MALE)	28480	1251-7986
A1P2	1252-0161	0	1	CONNECTOR 2-PIN MALE POST TYPE	28480	1252-0161
A1R1	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R2	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R3	0698-3615	8	1	RESISTOR 47 5% 2W MO TC=0+-200	27167	FP42-2-TOO-47R0-J
A1R4	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R5	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R6	0757-0059	4	1	RESISTOR 1M 1% .5W F TC=0+-100	28480	0757-0059
A1R7	0757-0409	8	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R8	0757-0415	6	2	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R9	0757-0409	8		RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R10	0757-0415	6		RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R11	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R14	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R15	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R16	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1R17	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R19 *	0698-8959	3	1	RESISTOR 619K 1% .125W F TC=0+-100	28480	0698-8959
A1R19 *	0757-0461	2	1	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-6812-F
*				See Section 7		
A1R20	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R21	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2741-F
A1R22	0757-0441	8	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-TO-8251-F
A1R23	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R24	0757-0795	5	1	RESISTOR 75 1% .5W F TC=0+-100	19701	MF-1/2-TO-75R0-F
A1R25	0698-3603	4	3	RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R26	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R27	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R29	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-9091-F
A1R30	0757-0468	9	2	RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1303-F
A1R31	0757-0450	9	1	RESISTOR 22.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2212-F
A1R32	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R34	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R35	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A1R36	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A1R37	0698-3160	8	1	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3162-F
A1R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R39	0757-0459	8	1	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1R40	0757-0468	9		RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1303-F
A1R41	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R42	0757-0479	2	1	RESISTOR 392K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-3923-F
A1R43	0811-1672	5	1	RESISTOR 3.3 5% 2W PW TC=0+-400	75042	BWH2-3R3-J
A1R50	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1RP1	1810-0488	8	3	NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP2	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP3	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RT1				NOT ASSIGNED		
A1RT2				NOT ASSIGNED		
A1RT3	0837-0263	2	1	THERMISTOR DISC 5-OHM	28480	0837-0263
A1RV1	0837-0120	0	1	VARISTOR-130VAC	28480	0837-0120
A1RV2	0837-0261	0	1	VARISTOR-220VAC	28480	0837-0261
A1SW1	3101-2582	6	1	SWITCH-SLIDE	28480	3101-2582
A1SW2	3101-2150	4	1	SWITCH-PB DPDT ALTNG 5A 250VAC	28480	3101-2150
A1SW3	3103-0091	2	1	SWITCH-THRM FXD +110C 6A OPN-ON-RISE	28480	3103-0091
A1T1	9100-4271	8	1	TRANSFORMER-CONT	28480	9100-4271
A1T2	9100-4265	0	2	TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T3	9100-4265	0		TRANSFORMER-BASE DRIVE	28480	9100-4265

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1T4	9100-4163	7	1	TRANSFORMER	28480	9100-4163
A1T5	9100-4266	1	1	TRANSFORMER-POWER	28480	9100-4266
A1T6	9100-4267	2	1	CHOKE-COUPLED	28480	9100-4267
A1TP1	1251-3618	6	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-3618
A1TP2	1251-3900	9	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3900
A1TP3	1251-7826	6	1	CONNECTOR-MALE	28480	1251-7826
A1U1	1826-0718	0	1	IC-MC1404	28480	1826-0718
A1U2	1820-2111	9	1	IC DRVR TTL INV	01295	SN75468N
A1U3	1826-0468	7	2	IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U4	1826-0468	7		IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U5	1826-1501	1	1	IC-TL594	28480	1826-1501
A1U6	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MLM324P
A1VR1	1826-0147	9	2	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR2	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
A1VR3	1826-0147	9		IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR4	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				The parts list for 01630-66529 and earlier power supply boards is located in a separate list that immediately precedes this one.		
A1	01630-66534	3	1	POWER SUPPLY ASSEMBLY	28480	01630-66534
A1C1	0180-3771	0	14	CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C2	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C3	0180-2946	9	3	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1C4	0160-4832	4	10	CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C5	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C6	0160-5347	8	3	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C7	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C8	0160-6333	4	4	CAPACITOR-FXD 2200PF +-5% 1KVDC POLYP	28480	0160-6333
A1C9	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C10	0180-3224	8	2	CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C11	0180-3224	8		CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C12	0160-4048	4	1	CAPACITOR-FXD 0.022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1C13	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
A1C14	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C15	0160-6333	4		CAPACITOR-FXD 2200PF +-5% 1KVDC POLYP	28480	0160-6333
A1C16	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C17	0160-6333	4		CAPACITOR-FXD 2200PF +-5% 1KVDC POLYP	28480	0160-6333
A1C18	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C19	0160-4814	2	2	CAPACITOR-FXD 150PF +-5% 100VDC CER	56289	592CCOG151J100B
A1C20	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C21	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C22	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C23	0160-6333	4		CAPACITOR-FXD 2200PF +-5% 1KVDC POLYP	28480	0160-6333
A1C24	0160-0164	7	3	CAPACITOR-FXD 0.039F +-10% 200VDC POLYE	28480	0160-0164
A1C25	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C26	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C27	0160-0164	7		CAPACITOR-FXD 0.039F +-10% 200VDC POLYE	28480	0160-0164
A1C28	0160-0164	7		CAPACITOR-FXD 0.039F +-10% 200VDC POLYE	28480	0160-0164
A1C29	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C30	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C31	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C32	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C33	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C34	0160-3715	0	1	CAPACITOR-FXD 0.015UF +-10% 250VDC	28480	0160-3715
A1C35	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C36	0160-5471	9	4	CAPACITOR-FXD 0.1UF +-5% 50VDC MET POLYE	28480	0160-5471
A1C37	0160-4814	2		CAPACITOR-FXD 150PF +-5% 100VDC CER	56289	592CCOG151J100B
A1C38	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C39	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C40	0160-4830	2	1	CAPACITOR-FXD 2200PF +-10% 100VDC CER	56289	592CX7R222K100B
A1C41	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C42	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C43	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C44	0160-4832	4		CAPACITOR-FXD 0.01UF +-10% 100VDC CER	56289	592CX7R103K100C
A1C45	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C46	0180-3771	0		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	299D105X9035AB1
A1C47	0180-2890	2	3	CAPACITOR-FXD 7500UF +75-10% 6.3VDC AL	00853	300JJ752U6R3C
A1C48	0180-2890	2		CAPACITOR-FXD 7500UF +75-10% 6.3VDC AL	00853	300JJ752U6R3C
A1C49	0180-2890	2		CAPACITOR-FXD 7500UF +75-10% 6.3VDC AL	00853	300JJ752U6R3C
A1C50	0160-5468	4	6	CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468
A1C51	0160-5468	4		CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468
A1C52	0160-5468	4		CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468
A1C53	0160-5468	4		CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468
A1C54	0160-5468	4		CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468
A1C55	0160-5468	4		CAPACITOR-FXD 0.47UF +-10% 50VDC	28480	0160-5468

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C56	0160-5579	8	1	CAPACITOR-FXD 0.047UF +-5% 63VDC	28480	0160-5579
A1C57	0160-5471	9		CAPACITOR-FXD 0.1UF +-5% 50VDC MET POLYE	28480	0160-5471
A1C58	0160-5471	9		CAPACITOR-FXD 0.1UF +-5% 50VDC MET POLYE	28480	0160-5471
A1C59	0160-5471	9		CAPACITOR-FXD 0.1UF +-5% 50VDC MET POLYE	28480	0160-5471
A1C60	0160-5098	6	1	CAPACITOR-FXD 0.22UF +-10% 50VDC CER	56289	592CX7R224K050E
A1CR1	1906-0006	9	1	DIODE-FW BRDG 400V 1A	18546	VE48
A1CR2	1901-1087	8	2	DIODE-PWR RECT 600V 3A 200NS	04713	MR856
A1CR3	1901-1087	8		DIODE-PWR RECT 600V 3A 200NS	04713	MR856
A1CR4	1906-0224	3	1	DIODE-FW BRDG 600V 25A	04713	MDA2506
A1CR5	1901-0731	7	7	DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR6	1901-0050	3	11	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR10	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A1CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR15	1906-0079	6	1	DIODE-FW BRDG 100V 10A	18546	VJ148X
A1CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR18	1906-0239	0	1	DIODE-CT-RECT 45V 30A	01281	SD-241
A1CR19	1906-0263	0	1	RFCT VSK 12	28480	1906-0263
A1CR20	1906-0262	9	1	RECT USE 2402	28480	1906-0262
A1CR21	1901-1081	2	2	DIODE-PWR RECT 100V 3A	04713	MR501
A1CR22	1901-1081	2		DIODE-PWR RECT 100V 3A	04713	MR501
A1CR23	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR24	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR25	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR26	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR27	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR28	1901-0731	7		DIODE-PWR RECT 400V 1A	71468	1N4004G
A1CR29	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1DS1	1990-0652	8	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
A1E1	0340-1172	1	4	BUSHING-INSULATING NYLON	28480	0340-1172
A1E2				NOT ASSIGNED		
A1E3	2110-0642	3	1	FUSEHOLDER	28480	2110-0642
A1E4	2110-0565	9	1	FUSEHOLDER CAP	28480	2110-0565
A1E5	0340-0884	0	1	INSULATOR XISTOR THERMAL CONDUCTIVE TO3	28480	0340-0884
A1E6	0340-0949	8	2	INSULATOR XISTOR THERMAL CONDUCTIVE	28480	0340-0949
A1F1	2110-0056	3	1	FUSE 6A 250V NTD 1.25X.25 UL IEC	75915	312006
A1FL1	9135-0175	6	1	FILTER-LINE	28480	9135-0175
A1H1	01830-23201	3	1	COUPLER-SWITCH EXTENSION	28480	01830-23201
A1H2	0515-1410	1	1	SCREW-MACH M3 20MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H3	0515-0372	2	8	SCREW-MACH M3 8MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A1H4	0515-1025	4	1	SCREW-MACH M3 26MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A1H5	0515-0374	4	5	SCREW-MACH M3 10MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A1H6	0400-0311	6	2	GROMMET-MOUNTING NYLON	28480	0400-0311
A1H7	3050-1071	7	8	WASHER-RECTANGULAR 10MM X 5.5MM	28480	3050-1071
A1L1	9140-0624	1	1	INDUCTOR 270UH 10% .725DX.818LG	28480	9140-0624
A1L2	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192
A1MP1	1205-0490	9	1	HEAT SINK 6022BS	28480	1205-0490
A1MP2	1205-0645	6	1	HEAT SINK	28480	1205-0645
A1MP3	1205-0489	6	4	HEAT SINK 6021BS	28480	1205-0489
A1MP4	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP5	1600-1330	6	1	STIFFENER-PCB	28480	1600-1330
A1MP6	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP7	1205-0663	8	1	HEAT SINK TO220	28480	1205-0663
A1MP8	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP9	1205-0486	3	1	HEAT SINK	28480	1205-0486

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1Q1	1854-0827	1	2	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1Q2	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1Q3	1853-0036	2	1	TRANSISTOR PNP SI PD=310MW FT=250MHZ	27014	2N3906
A1P1	1251-7986	9	1	CONNECTOR-50 CONTACT (MALE)	28480	1251-7986
A1P2	1252-0161	0	1	CONNECTOR 2-PIN MALE POST TYPE	28480	1252-0161
A1R1	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R2	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R3	0698-3615	8	1	RESISTOR 47 5% 2W MO TC=0+-200	27167	FP42-2-TOO-47R0-J
A1R4	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R5	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R6	0757-0059	4	1	RESISTOR 1M 1% .5W F TC=0+-100	28480	0757-0059
A1R7	0757-0409	8	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R8	0757-0415	6	2	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R9	0757-0409	8		RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R10	0757-0415	6		RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R11	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R14	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R15	0757-0316	6	1	RESISTOR 42.2 1% .125W F TC=0+-100	24546	C4-1/8-TO-42R2-F
A1R16	0757-0462	3	2	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1R17	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R19	0757-0461	2	1	RESISTOR 68.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-6812-F
A1R20	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R21	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2741-F
A1R22	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2612-F
A1R23	0757-0440	7	4	RESISTOR 7500 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R24	0757-0795	5	1	RESISTOR 75 1% .5W F TC=0+-100	19701	MF-1/2-TO-75R0-F
A1R25	0698-3603	4	3	RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R26	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R27	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J
A1R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R29	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-9091-F
A1R30	0698-4502	4	1	RESISTOR 64.9K 1% .125W F TC=0+-100	24546	C4-1/8-TO-6492-F
A1R31	0757-0450	9	1	RESISTOR 22.1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2212-F
A1R32	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R34	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R35	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A1R36	0757-0283	6	2	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A1R37	0698-3450	9	1	RESISTOR 42.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4222-F
A1R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R39	0757-0459	8	1	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5622-F
A1R40	0757-0468	9	1	RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1303-F
A1R41	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R42	0757-0479	2	1	RESISTOR 392K 1% .125W F TC=0+-100	19701	MF4C1/8-TO-3923-F
A1R43	0811-1672	5	1	RESISTOR 3.3 5% 2W PW TC=0+-400	75042	BWH2-3R3-J
A1R44	0757-0440	7		RESISTOR 7500 1% .125W F TC=0+-100	24546	C4-1/8-TO-7501-F
A1R45	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R46	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A1R47	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A1R48	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R49	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R50	0757-0462	3		RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1RP1	1810-0488	8	4	NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP2	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP3	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP4	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RT1	0837-0263	2	2	THERMISTOR DISC 5-OHM	28480	0837-0263
A1RT2	0837-0263	2		THERMISTOR DISC 5-OHM	28480	0837-0263
A1RT3	0837-0260	9	1	THERMISTOR-SWITCHING 100 OHMS	50157	OTP100.11
A1RV1	0837-0261	0	1	VARISTOR-220VAC	28480	0837-0261

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1SW1	3101-2582	6	1	SWITCH-SLIDE	28480	3101-2582
A1SW2	3101-2150	4	1	SWITCH-PB DPDT ALTNG 5A 250VAC	28480	3101-2150
A1T1	9100-4271	8	1	TRANSFORMER-CONT	28480	9100-4271
A1T2	9100-4265	0	2	TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T3	9100-4265	0		TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T4	9100-4629	0	1	TRANSFORMER	01961	PE 63586
A1T5	9100-4266	1	1	TRANSFORMER-POWER	28480	9100-4266
A1T6	9100-4267	2	1	CHOKE-COUPLED	28480	9100-4267
A1TP1	1251-3618	6	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-3618
A1TP2	1251-3900	9	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3900
A1TP3	1251-7826	6	1	CONNECTOR-MALE	28480	1251-7826
A1U1	1826-0718	0	1	IC-MC1404	28480	1826-0718
A1U2	1820-2111	9	1	IC DRVR TTL INV	01295	SN75468N
A1U3	1826-0468	7	2	IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U4	1826-0468	7		IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U5	1826-1501	1	1	IC-TL594	28480	1826-1501
A1U6	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MLM324P
A1U7	1826-0412	1	1	IC COMPARATOR DUAL 8-PIN-DIP	27014	LM393N
A1V1	1970-0050	8	2	TUBE-ELECTRON SURGE VOLTAGE PROTECTOR	25088	B1-A230-Y8
A1V2	1970-0050	8		TUBE-ELECTRON SURGE VOLTAGE PROTECTOR	25088	B1-A230-Y8
A1VR1	1826-0147	9	2	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR2	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
A1VR3	1826-0147	9		IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR4	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2	01630-66501	4	1	MOTHERBOARD ASSEMBLY	28480	01630-66501
A2C1	0160-6500	7	3	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A2C2	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A2C3	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A2J1	1251-7867	5	1	CONNECTOR-100 CONTACT (MALE)	28480	1251-7867
A2J2	1251-7300	1	2	CONNECTOR-50 CONTACT (MALE)	28480	1251-7300
A2J3	1251-8733	6	4	CONNECTOR-100 CONTACT (MALE)	28480	1251-8733
A2J4	1251-8733	6		CONNECTOR-100 CONTACT (MALE)	28480	1251-8733
A2J5	1251-8733	6		CONNECTOR-100 CONTACT (MALE)	28480	1251-8733
A2J6	1251-8733	6		CONNECTOR-100 CONTACT (MALE)	28480	1251-8733
A2J7	1251-7300	1		CONNECTOR-50 CONTACT (MALE)	28480	1251-7300
A2RP1	1810-0619	7	4	RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP2	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP3	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619
A2RP4	1810-0619	7		RESISTIVE NETWORK-171/241	28480	1810-0619

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
				EARLY CPU BOARDS HAVE PARTS OF THE HP-IL CIRCUITRY MOUNTED ON A SMALL PC BOARD. THESE PARTS ARE ON LATER VERSIONS OF THE CPU BOARD		
A3A1	01630-66513	8	1	ESD ASSEMBLY	28480	01630-66513
A3A1C1	0160-5246	6	1	CAPACITOR-FXD .1UF 50VDC	28480	0160-5246
A3A1CR1	1901-0050	3	4	DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3A1R1	0683-4705	8	1	RESISTOR-FXD 47 OHM .25W CC	28480	0683-4705
A3U20	1LR4-0002	2	1	IC HP-IL	28480	1LR4-0002
A3A1XU1	1200-0567	1	1	SOCKET-IC 28-PIN	28480	1200-0567
A3	01630-66503	6	1	CPU ASSY - SAME AS 01630-66522	28480	01630-66503
A3	01630-66512	7	1	CPU ASSY - SAME AS 01630-66522 EXCEPT: CHANGE A3XU6I QTY TO 1	28480	01630-66512
A3	01630-66515	0	1	CPU ASSY - SAME AS 01630-66535 EXCEPT:	28480	01630-66515
A3U3H	01630-80011	1	1	PROM 3 D2764-3	28480	01630-80011
A3U3I	01630-80010	0	1	PROM 2 D2764-3	28480	01630-80010
A3U3J	01630-80009	7	1	PROM 1 D2764-3	28480	01630-80009
A3U3K	01630-80008	6	1	PROM 0 D2764-3	28480	01630-80008
A3U4H	01630-80015	5	1	PROM 7 D2764-3	28480	01630-80015
A3U4I	01630-80014	4	1	PROM 6 D2764-3	28480	01630-80014
A3U4J	01630-80013	3	1	PROM 5 D2764-3	28480	01630-80013
A3U4K	01630-80012	2	1	PROM 4 D2764-3	28480	01630-80012
A3	01630-66519	7	1	CPU ASSY - SAME AS 01630-66522 EXCEPT:	28480	01630-66519
A3U3H	01630-80041	7	1	PROM 3 27128-3	28480	01630-80041
A3U3I	01630-80040	6	1	PROM 2 27128-3	28480	01630-80040
A3U3J	01630-80025	7	1	PROM 1 27128-3	28480	01630-80025
A3U3K	01630-80024	6	1	PROM 0 27128-3	28480	01630-80024
A3U4H	01630-80042	8	1	PROM 7 27128-3	28480	01630-80042
A3U4I	01630-80030	4	1	PROM 6 27128-3	28480	01630-80030
A3U4J	01630-80029	1	1	PROM 5 27128-3	28480	01630-80029
A3U4K	01630-80028	0	1	PROM 4 27128-3	28480	01630-80028
A3	01630-66522	9	1	CPU ASSY - SAME AS 01630-66535 EXCEPT:	28480	01630-66522
				DELETE:		
C64						
CR5-8						
J7						
R38						
U20,U3P-Q						
				ADD:		
A3A1	01630-66513	8	1	BOARD-ESD	28480	01630-66513
				CHANGE:		
A3J1	1250-1774	9	2	CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM	28480	1250-1774
A3J4	1250-1774	9		CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM	28480	1250-1774
A3U3H	01630-80011	1	1	PROM 3 D2764-3	28480	01630-80011
A3U3I	01630-80010	0	1	PROM 2 D2764-3	28480	01630-80010
A3U3J	01630-80009	7	1	PROM 1 D2764-3	28480	01630-80009
A3U3K	01630-80008	6	1	PROM 0 D2764-3	28480	01630-80008
A3U4H	01630-80015	5	1	PROM 7 D2764-3	28480	01630-80015
A3U4I	01630-80014	4	1	PROM 6 D2764-3	28480	01630-80014
A3U4J	01630-80013	3	1	PROM 5 D2764-3	28480	01630-80013
A3U4K	01630-80012	2	1	PROM 4 D2764-3	28480	01630-80012

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3	01630-66526	3	1	CPU ASSY - SAME AS 01630-66535 EXCEPT:	28480	01630-66526
A3U3H	01630-80041	7	1	PROM 3 27128-3	28480	01630-80041
A3U3I	01630-80040	6	1	PROM 2 27128-3	28480	01630-80040
A3U3J	01630-80025	7	1	PROM 1 27128-3	28480	01630-80025
A3U3K	01630-80024	6	1	PROM 0 27128-3	28480	01630-80024
A3U4H	01630-80042	8	1	PROM 7 27128-3	28480	01630-80042
A3U4I	01630-80030	4	1	PROM 6 27128-3	28480	01630-80030
A3U4J	01630-80029	1	1	PROM 5 27128-3	28480	01630-80029
A3U4K	01630-80028	0	1	PROM 4 27128-3	28480	01630-80028
A3	01630-66528	5	1	CPU ASSEMBLY - SAME AS 01630-66535 See Section 7, Instrument History	28480	01630-66528
A3	01630-66533	2	1	CPU ASSEMBLY - SAME AS 01630-66535 See Section 7, Instrument History	28480	01630-66533
A3	01630-66535	4	1	CPU ASSEMBLY	28480	01630-66535
A3C1	0160-5311	6	2	CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-5311
A3C2	0160-5311	6		CAPACITOR-FXD 330PF +-5% 100VDC CER	28480	0160-5311
A3C3	0160-6500	7	40	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C4	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C5	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C6	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C7	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C8	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C9	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C10	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C11	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C12	0160-5474	2	6	CAPACITOR-FXD .1UF +-5% 100VDC MET POLY	28480	0160-5474
A3C13	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C14	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C15	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C16	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C17	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C18	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C19	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C20	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C21	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C22	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C23	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C24	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C25	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C26	0160-3508	9	7	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C27	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C28	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C29	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C30	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C31	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C32	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C33	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C34	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C35 *	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER See Section 7, Instrument History	28480	0160-3508
A3C35 *	0160-5471	9	6	CAPACITOR-FXD .1UF +-5% 50VDC MET POLY See Section 7, Instrument History	28480	0160-5471

See Introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3C36	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C37	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C38	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C39	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C40	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C41	0160-5474	2		CAPACITOR-FXD .1UF 100VDC	28480	0160-5474
A3C42	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C43	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C44	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C45	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C46	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C47	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C48	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C49	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C50	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C51	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C52	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C53	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A3C54	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C55	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A3C56				NOT USED		
A3C57	0180-0229	7	3	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C58	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C59	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A3C60	0180-0374	3	1	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A3C61	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A3C62	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A3C63	0160-4835	7	1	CAPACITOR-FXD .1UF 50VDC	28480	0160-4835
A3C64	0160-5246	6	1	CAPACITOR-FXD .1UF 50VDC	28480	0160-5246
A3CR1	1902-0186	8	4	DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR2	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR3	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR4	1902-0186	8		DIODE-ZNR 32.4V 5% DO-35 PD=.4W	28480	1902-0186
A3CR5	1901-0050	3	4	DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO35	28480	1901-0050
A3H1	0515-0372	2	2	SCREW-MACH M3 8MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A3H2	0624-0306	3	2	SCREW-TPG 2-28 .5-IN-LG PAN-HD-POZI STL	28480	0624-0306
A3H3	01630-01208	2	1	GROUND BRACKET	28480	01630-01208
A3H4	0515-0430	3	2	SCREW-MACH M3 6MM-LG PAN-HD TORX	00000	ORDER BY DESCRIPTION
A3J1 *	1250-1842	2	2	CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM See Section 7, Instrument History	28480	1250-1842
A3J2	1251-7162	3	1	CONNECTOR 24-PIN F MICRO-RIBBON	28480	1251-7162
A3J3	82169-60007	3	1	CONNECTOR HP-IL	28480	82169-60007
A3J4 *	1250-1842	2		CONNECTOR-RF BNC FEM SPCL-MTG 50-OHM See Section 7, Instrument History	28480	1250-1842
A3J5	1251-7666	2	1	CONNECTOR-16 PIN	28480	1251-7666
A3J6	1251-7664	0	1	CONNECTOR-14 PIN	28480	1251-7664
A3LS1	9164-0209	8	1	AUDIO TRANSDUCER	28480	9164-0209
A3MP1	01630-01204	8	1	BRACKET - HP-IL	28480	01630-01204
A3MP2	1251-5595	2	2	POLARIZING KEY-POST CONN (P/O J5)	28480	1251-5595
A3MP3	1251-5595	2		POLARIZING KEY-POST CONN (P/O J6)	28480	1251-5595
A3P1	1251-8729	0	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-8729
A3R1	0757-0283	6	8	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R2	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R3	0757-0446	3	2	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1502-F
A3R4	0698-3446	3	2	RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-TO-383R-F
A3R5	0698-3446	3		RESISTOR 383 1% .125W F TC=0+-100	24546	C4-1/8-TO-383R-F
A3R6	0757-0446	3		RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1502-F
A3R7	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R8	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A3R9	0698-4002	9	5	RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A3R10	0757-0389	3	3	RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-TO-33R2-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R11	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R12	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R13	0757-0389	3		RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A3R14	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R15	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R16 *	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100 See Section 7, Instrument History	24546	C4-1/8-T0-1002-F
A3R16 *	0757-0465	6	1	RESISTOR 100K 1% .125W F TC=0+-100 See Section 7, Instrument History	24546	C4-1/8-T0-1003-F
A3R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A3R18	0757-0480	5	1	RESISTOR 432K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-4323-F
A3R19	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R20	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A3R21	0757-0451	0	1	RESISTOR 24.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2432-F
A3R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R23	0698-4439	6	1	RESISTOR 3.24K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3241-F
A3R24	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A3R25	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A3R26	0757-0443	0	1	RESISTOR 11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1102-F
A3R27	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2611-F
A3R28	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A3R29	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5001-F
A3R30	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A3R31	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A3R32	0699-1000	3	2	RESISTOR-FXD 4.25K OHM .1%	28480	0699-1000
A3R33	0699-1000	3		RESISTOR-FXD 4.25K OHM .1%	28480	0699-1000
A3R34	0757-0389	3		RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A3R35	0698-6360	6	2	RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A3R36	0698-6360	6		RESISTOR 10K .1% .125W F TC=0+-25	28480	0698-6360
A3R37	2100-2655	1	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A3R38	0683-4705	8	1	RESISTOR-FXD 47 OHM .25W CC	28480	0683-4705
A3RP1	1810-0280	8	2	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3RP2	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222
A3RP3	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A3RP4	1810-0382	1	2	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A3RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A3RP6	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A3SW1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
A3TP1-5	1251-5395	0	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-5395
A3TP6-7	1251-6073	3	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-6073
A3U1E	1820-2024	3	8	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U1H	1820-2485	0	1	IC RCVR TTL LS BUS OCTL	01295	SN75160N
A3U1I	1820-2547	5	1	IC RCVR TTL LS OCTL	01295	SN75162N
A3U1J	1820-1198	0	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A3U1K	1820-1198	0		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
A3U1L	1820-1730	6	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U1M	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U2A	1820-2701	3	2	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
A3U2B	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A3U2C	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U2D	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U2E	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A3U2G	1820-2548	6	1	IC-TMS 9914	28480	1820-2548
A3U2O	1LR4-0002	2	1	IC HP-IL	28480	1LR4-0002
A3U2P	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U3A	1818-3059	1	8	IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3059
A3U3B	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3059
A3U3C	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3059
A3U3D	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-S	50167	1818-3059
A3U3E	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U3F	1820-2096	9	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U3H *	01630-80057	5	1	PROM 3 D2764-3	28480	01630-80057
A3U3I *	01630-80056	4	1	PROM 2 D2764-3	28480	01630-80056
A3U3J *	01630-80055	3	1	PROM 1 D2764-3	28480	01630-80055
A3U3K *	01630-80054	2	1	PROM 0 D2764-3 Before replacing PROMS A3U3H-K See Instrument Family History, Section 7	28480	01630-80054

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U3N	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U3O	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U3P	1820-3391	9	2	IC MUXR/DATA-SEL TTL 8-TO-1-LINE	01295	74ALS151
A3U3Q	1820-3391	9		IC MUXR/DATA-SEL TTL 8-TO-1-LINE	01295	74ALS151
A3U4A	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3059
A3U4B	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3059
A3U4C	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3059
A3U4D	1818-3059	1		IC NMOS 65536 (64K) DYN RAM 150-NS 3-5	50167	1818-3059
A3U4F	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
A3U4G	1820-1278	7	1	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
A3U4H *	01630-80061	1	1	PROM 7 D2764-3	28480	01630-80061
A3U4I *	01630-80060	0	1	PROM 6 D2764-3	28480	01630-80060
A3U4J *	01630-80059	7	1	PROM 5 D2764-3	28480	01630-80059
A3U4K *	01630-80058	6	1	PROM 4 D2764-3 Before replacing PROMS A3U4H-K See Instrument Family History, Section 7	28480	01630-80058
A3U4N	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U4O	1820-1238	9	3	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U4P	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U4Q	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A3U5A	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5B	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
A3U5C	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U5E	1820-1439	2	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A3U5F	1820-1309	5	4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U5G	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U5J	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U5N	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U5O	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5P	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U5Q	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U6A	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U6B	1820-1457	4	1	IC SHF-RGTR TTL S D-TYPE PRL-IN PRL-OUT	01295	SN74S299N
A3U6C	1818-3074	0	1	IC MEMORY ROM	28480	1818-3074
A3U6D	1820-2853	6	1	IC-MC68A45L	28480	1820-2853
A3U6E	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
A3U6F	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U6G	1820-1309	5		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S258N
A3U6I	1820-2854	7	1	IC-MPU MC68B09EL	28480	1820-2854
A3U6J	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A3U6L	1820-2911	7	1	IC-MMU MC68829L	28480	1820-2911
A3U6M	1820-3911	9	1	IC NMOS 16-BIT	34335	AM9513ADC
A3U6N	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
A3U6O	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U6P	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A3U7A	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U7B	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A3U7C	1820-1191	3	3	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U7D	1820-0694	9	1	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
A3U7F	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U7G	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U7H	1820-1210	7	1	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A3U7I	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U7K	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U7L	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A3U7M	1820-3124	6	5	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A3U7N	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U7O	1826-0609	8	1	IC MULTIPLXR ANLG 16-DIP-C PKG	06665	MUX08FQ
A3U7P	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A3U8C	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U8D	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U8F	1820-1191	3		IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A3U8G	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U8H	1820-1287	8	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS37N
A3U8I	1820-0697	2	1	IC DRVR TTL S NAND LINE DUAL 4-INP	01295	SN74S140N
A3U8J	1820-3125	1	3	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A3U8K	1820-3125	1		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A3U8L	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U8O	1826-0753	3	3	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A3U8P	1826-0753	3		IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A3U8Q	1826-0753	3		IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MC34004BL
A3U9D	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
A3U9E	1820-2150	6	1	IC MICPROC-ACCESS NMOS	34649	D8279-5
A3U9F	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U9G	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A3U9H	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
A3U9I	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A3U9J	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A3U9K	1820-3125	1		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A3U9L	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A3U9M	1820-1990	0	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10100L
A3U9N	1826-0856	7	1	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A3U10O	1826-0718	0	1	IC-MC1404	28480	1826-0718
A3UR4E	1810-0301	4	1	NETWORK-RES 16-DIP51.0 OHM X 8	01121	316B510
A3UR9O	1810-0613	1	5	RESISTIVE NETWORK	28480	1810-0613
A3UR9P	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR9Q	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR10P	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UR10Q	1810-0613	1		RESISTIVE NETWORK	28480	1810-0613
A3UT1	9100-4226	3	1	TRANSFORMER	28480	9100-4226
A3UY1D	1813-0275	7	1	OSCILLATOR-40 MHZ	28480	1813-0275
A3UY6Q	1813-0174	5	1	OSCILLATOR-4.00 MHZ	28480	1813-0174
A3XRP3	1200-1166	8	1	SOCKET 10-PIN-SIP	28480	1200-1166
A3XU3H	1200-0567	1	8	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3I	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3J	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU3K	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4H	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4I	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4J	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU4K	1200-0567	1		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A3XU6I	1200-0654	7	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A3XUY1D	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4	01630-66505	8	1	STATE MASTER ASSEMBLY	28480	01630-66505
				SAME AS 01630-66518 WITH THE FOLLOWING EXCEPTIONS:		
A4U2B	1820-1788	4	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2C	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2E	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2F	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2G	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2H	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2I	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U4L	1820-2451	0	1	IC LCH ECL D-TYPE NEG-EDGE-TRIG COM	04713	MC10168P
A4	01630-66509	2	1	STATE MASTER ASSEMBLY	28480	01630-66509
				SAME AS 01630-66518 WITH THE FOLLOWING EXCEPTIONS:		
A4U2B	1820-1788	4	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2C	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2E	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2F	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2G	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2H	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4U2I	1820-1788	4		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	F10016DC
A4	01630-66518	3	1	STATE MASTER ASSEMBLY	28480	01630-66518
A4C1	0160-6500	7	70	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C2	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C3	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C4	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C5	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C6	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C7	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C8	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C9	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C10	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C11	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C12	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C13	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C14	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C15	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C16	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C17	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C18	0160-5309	2	7	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C19	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C20	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C21	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C22	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C23	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C24	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C25	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C26	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C27	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C28	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C29	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C30	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C31	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C32	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C33	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C34	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C35	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C36	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C37	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C38	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C39	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C40	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C41	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C42	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C43	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C44	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C45	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C46	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C47	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C48	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C49	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C50	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C51	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C52	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C53	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C54	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C55	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C56	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C57	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C58	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C59	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C60	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C61	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C62	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C63	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C64	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C65	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A4C66	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C67	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C68	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C69	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C70	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C71	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C72	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C73	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C74	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C75	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C76	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C77	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4C78	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A4C79	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A4DL1	1810-0602	8	1	DELAY LINE- 7NS	28480	1810-0602
A4J1	1251-7705	0	3	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4J2	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4J3	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A4P1	1251-8729	0	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-8729
A4R1	0757-0418	9	6	RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R2	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R3	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R4	2100-3123	0	2	RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A4R5	2100-3123	0		RESISTOR-TRMR 500 10% C SIDE-ADJ 17-TRN	02111	43P501
A4R6	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R7	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A4R8	0698-3441	8	2	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A4R9	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F
A4R10	0757-0408	7	2	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-TO-243R-F
A4R11	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24946	C4-1/8-TO-215R-F
A4R12	0757-0408	7		RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-TO-243R-F
A4R13	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R14	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R15	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A4R16	0757-0418	9		RESISTOR 619 1% .125W F TC=0+-100	24546	C4-1/8-TO-619R-F

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4RP1	1810-0272	8	6	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP2	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP3	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP4	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP5	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP6	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A4RP7	1810-0382	1	28	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP10	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP14	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP16	1810-0219	3	1	NETWORK-RES 8-SIP220.0 OHM X 4	01121	208B221
A4RP17	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP18	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP19	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP20	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP21	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP22	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP23	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP24	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP25	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP26	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP27	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP28	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP29	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP30	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP31	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP32	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP33	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP34	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RP35	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A4RT1	0037-0046	9	2	THERMISTOR DISC 2K-OHM	28480	0037-0046
A4RT2	0037-0046	9		THERMISTOR DISC 2K-OHM	28480	0037-0046
A4TP1	1250-1737	4	2	COAXIAL TEST POINT	28480	1250-1737
A4TP2	1250-1737	4		COAXIAL TEST POINT	28480	1250-1737
A4U1A	1820-2848	9	11	IC-MC10H116P	28480	1820-2848
A4U1B	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1C	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1D	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1E	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1F	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1H	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1I	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1J	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U1K	1820-1944	4	1	IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
A4U1L	1820-0802	1	5	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U1M	1820-2450	9	1	IC INV ECL HEX	04713	MC10189P
A4U1N	1820-0827	0	1	IC DCDR ECL BIN 3-TO-8-LINE	04713	MC10161P
A4U2B	1820-4159	9	18	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2C	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2D	1820-1225	0	1	IC FF ECL D-M/S DUAL	04713	MC10231P
A4U2E	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2F	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2G	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2H	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2I	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	04713	MC10H016P
A4U2J	1820-0817	8	4	IC FF ECL D-M/S DUAL	04713	MC10131P
A4U2K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U2L	1820-1686	1	2	IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A4U2M	1820-0806	5	3	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U3A	1816-1591	8	7	IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3B	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3C	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U3E	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3F	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3G	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3I	1816-1591	8		IC ECL/10K 4096 (4K) STAT RAM 25-NS O-E	50167	MBM10474
A4U3J	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U3K	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U3L	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U3M	1820-0809	8	1	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC10115P
A4U3N	1820-1399	3	3	IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A4U4K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U4L	1820-2959	3	2	IC-MC10H158P	28480	1820-2959
A4U4M	1820-2860	5	1	IC-MC10H130P	28480	1820-2860
A4U5A	1820-1359	5	4	IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5B	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5C	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5D	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A4U5E	1816-1555	4	1	IC-RAM 10422-6	28480	1816-1555
A4U5F	1816-1555	4	3	IC-RAM 10422-6	28480	1816-1555
A4U5G	1816-1555	4		IC-RAM 10422-6	28480	1816-1555
A4U5I	1816-1555	4		IC-RAM 10422-6	28480	1816-1555
A4U5K	1820-2822	9	1	IC-MC10H105P	28480	1820-2822
A4U5L	1820-2849	0	8	IC-MC10H131P	28480	1820-2849
A4U5M	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U5N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U6A	1820-3128	0	5	IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U6B	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U6C	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U6D	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U6E	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U6F	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A4U6G	1820-0804	3	1	IC GATE ECL NOR TPL	04713	MC10106P
A4U6H	1816-1554	3	1	IC ECL/10K 64-BIT STAT RAM 6-NS	07263	10H145
A4U6I	1820-2962	8	1	IC-MC10H103P	28480	1820-2962
A4U6J	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U6K	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U6L	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A4U6M	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A4U6N	1820-2848	9		IC-MC10H116P	28480	1820-2848
A4U7B	1820-2823	0	1	IC-MC10H102	28480	1820-2823
A4U7C	1820-1686	1		IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A4U7D	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U7E	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U7F	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U7G	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U7H	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A4U7I	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A4U7J	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U7K	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A4U7L	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U7M	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U7N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8C	1820-2451	0	1	IC LCH ECL D-TYPE NEG-EDGE-TRIG COM	04713	MC10168P
A4U8D	1820-1400	7	1	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A4U8E	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8F	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8G	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8H	1820-3128	0		IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158
A4U8I	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A4U8J	1820-2891	2	1	IC-MC10H101P	28480	1820-2891
A4U8K	1820-2963	9	1	IC-MC10H210	28480	1820-2963
A4U8L	1820-2959	3		IC-MC10H158P	28480	1820-2959
A4U8M	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8N	1820-2849	0		IC-MC10H131P	28480	1820-2849
A4U8O	1820-2849	0		IC-MC10H131P	28480	1820-2849

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5	01630-66506	9	1	TIMING MASTER ASSEMBLY	28480	01630-66506
				USES THE SAME PARTS AS 01630-66524 WITH THE FOLLOWING EXCEPTIONS:		
				DELETE;		
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
				CHANGE;		
A5C25	0160-3879	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
				ADD;		
A5C26	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A5C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C29	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5L1	9100-2248	5	1	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A5L2	9100-2252	1	1	INDUCTOR RF-CH-MLD 270NH 10% .105DX.26LG	28480	9100-2252
A5L3	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5Q1	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A5R7	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A5R8	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A5R10	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A5R11	0698-4426	1		RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5Y1	0410-1335	7	1	CRYSTAL-QUARTZ 200 MHZ HC-18/U-HLDR	28480	0410-1335
A5	01630-66510	5	1	TIMING MASTER ASSEMBLY USES THE SAME PARTS AS 01630-66524 WITH THE FOLLOWING EXCEPTIONS:	28480	01630-66510
				DELETE;		
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
				CHANGE;		
A5C25	0160-3879	7	4	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
				ADD;		
A5C26	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A5C27	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C29	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C30	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5L1	9100-2248	5	1	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A5L2	9100-2252	1	1	INDUCTOR RF-CH-MLD 270NH 10% .105DX.26LG	28480	9100-2252
A5L3	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A5Q1	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A5R7	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A5R8	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A5R10	0698-0085	0	1	RESISTOR 2.61K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2611-F
A5R11	0698-4426	1		RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5Y1	0410-1335	7	1	CRYSTAL-QUARTZ 200 MHZ HC-18/U-HLDR	28480	0410-1335
A5	01630-66524	1	1	TIMING MASTER ASSEMBLY	28480	01630-66524
A5C1	0160-6500	7	52	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C2	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C3	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5C4	0160-5341	2	1	CAPACITOR-FXD 4UF 50VDC	28480	0160-5341
A5C5	0160-5342	3	1	CAPACITOR-FXD .4UF 50VDC	28480	0160-5342
A5C6	0160-5475	3	1	CAPACITOR-FXD PC .04UF 50VDC	28480	0160-5475
A5C7	0160-5415	1	1	CAPACITOR-FXD 3600PF 50VDC	28480	0160-5415
A5C8	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C9	0160-5506	1	3	CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C10	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C11	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C12	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C13	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C14	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C15	0160-5506	1		CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C16	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C17	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C18	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C19	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C20	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C21	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C22	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C23	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C24	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C25	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C26				NOT USED		
A5C27				NOT USED		
A5C28	0160-3874	2	1	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A5C29				NOT USED		
A5C30				NOT USED		
A5C31	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C32	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C33	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C34	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C35	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C36	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C37	0160-3879	7	1	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A5C38	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C39	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C40	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C41	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C42	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C43	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C44	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C45	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C46	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C47	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C48	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C49	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C50	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C51	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C52	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C53	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C54	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C55	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C56	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C57	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C58	0160-5506	1		CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A5C59	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C60	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C61	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C62	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C63	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C64	0180-0229	7	2	CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A5C65	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A5C66	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5C67	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A5J1	1251-7705	0	1	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A5MP1	1205-0484	1	2	HEAT SINK SOCKET	28480	1205-0484

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5P1	1251-8729	0	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-8729
A5R1	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0+-100	24546	C4-1/8-TO-681R-F
A5R2	0698-6735	9	1	RESISTOR 1.71K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1711-F
A5R3	0698-4426	1	1	RESISTOR 1.58K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1581-F
A5R4	0757-0407	6	2	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-TO-201-F
A5R5	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-TO-201-F
A5R6	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R7				NOT USED		
A5R8				NOT USED		
A5R9	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R10				NOT USED		
A5R11				NOT USED		
A5R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A5RP1	1810-0382	1	24	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP2	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP3	1810-0270	6	1	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
A5RP4	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP6	1810-0275	1	1	NETWORK-RES 10-SIP1.0K OHM X 9	01121	210A102
A5RP7	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP10	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP14	1810-0350	3	2	NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A5RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP16	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP17	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP18	1810-0350	3		NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A5RP19	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP20	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP21	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP22	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP23	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP24	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP25	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP26	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP27	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5RP28	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A5TP1	1250-1737	4	1	COAXIAL TEST POINT	28480	1250-1737
A5U1J	1820-1686	1	1	IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A5U1K	1820-4159	9	7	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U1L	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U2A	1858-0058	8	2	TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	MPQ3906
A5U2D	1820-0810	1	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A5U2G	1820-0825	8	1	IC SHF-RGTR ECL D-TYPE PRL-IN PRL-OUT	04713	MC10141L
A5U2H	1820-1225	4	3	IC FF ECL D-M/S DUAL	04713	MC10231P
A5U2I	1820-4080	5	3	IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135P
A5U2J	1820-0806	5	2	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A5U2K	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U2L	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U3A	1858-0021	5	2	TRANSISTOR ARRAY 16-PIN PLSTC	3L585	CA3083
A5U3B	1858-0021	5		TRANSISTOR ARRAY 16-PIN PLSTC	3L585	CA3083
A5U3C	1858-0058	8		TRANSISTOR ARRAY 14-PIN PLSTC TO-116	04713	MPQ3906
A5U3D	1820-0802	1	6	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U3E	1820-1400	7	2	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U3F	1820-2848	9	5	IC-MC10H116	28480	1820-2848
A5U3G	1820-2849	0	7	IC-MC10H131P	28480	1820-2849
A5U3H	1820-4080	5		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135P
A5U3I	1820-1788	4	1	IC CNTR FCL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A5U3J	1820-1359	5	5	IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U3K	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U3L	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5U4C	1820-1399	3	3	IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A5U4D	1820-0827	0	1	IC DCDR ECL BIN 3-TO-8-LINE	04713	MC10161P
A5U4E	1820-2848	9		IC-MC10H116	28480	1820-2848
A5U4F	1810-0931	2	2	DELAY LINE- 17NS X 4	28480	1810-0931
A5U4G	1820-2823	0	1	IC-MC10H10Z	28480	1820-2823
A5U4H	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A5U4I	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U4J	1820-0817	8	2	IC FF ECL D-M/S DUAL	04713	MC10131P
A5U4K	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U4L	1820-1359	5		IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A5U5B	1813-0425	9	1	OSCILLATOR 200 MHZ	28480	1813-0425
A5U5C	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A5U5D	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U5E	1820-2848	9		IC-MC10H116	28480	1820-2848
A5U5F	1810-0931	2		DELAY LINE- 17NS X 4	28480	1810-0931
A5U5G	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U5H	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A5U5I	1820-0804	3	1	IC GATE ECL NOR TPL	04713	MC10106P
A5U5J	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U5K	1820-2475	8	2	IC LCH ECL GATED D NEG-EDGE-TRIG COM	04713	MC10133P
A5U5L	1820-2475	8		IC LCH ECL GATED D NEG-EDGE-TRIG COM	04713	MC10133P
A5U6A	1820-2848	9		IC-MC10H116	28480	1820-2848
A5U6B	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A5U6C	1820-2847	8	1	IC-MC10153P	28480	1820-2847
A5U6D	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176P
A5U6F	1820-2905	9	2	IC-SC25647	28480	1820-2905
A5U6I	1816-1462	2	8	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6K	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U6L	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U7A	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U7B	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U7C	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U7D	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U8B	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U8C	1820-2875	2	2	IC-MC10H164P	28480	1820-2875
A5U8D	1820-2875	2		IC-MC10H164P	28480	1820-2875
A5U8F	1820-2905	9		IC-SC25647	28480	1820-2905
A5U8I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8K	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U8L	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A5U9B	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A5U9C	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U9D	1820-2849	0		IC-MC10H131P	28480	1820-2849
A5U9E	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A5U9F	1820-0806	5		IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A5U9G	1820-2848	9		IC-MC10H116	28480	1820-2848
A5U9H	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A5U9I	1820-2821	8	1	IC-MC10159P	28480	1820-2821
A5U9J	1820-4080	5		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135P
A5U9K	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5U9L	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A5XU6F	1200-1001	0	2	SOCKET-68 PIN	28480	1200-1001
A5XU8F	1200-1001	0		SOCKET-68 PIN	28480	1200-1001

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A7	01630-66504	7	1	KEYBOARD ASSEMBLY (INCLUDES KEYCAPS)	28480	01630-66504
				SAME AS 01630-66530 WITH THE FOLLOWING EXCEPTIONS:		
				ADD:		
	1200-0474	9	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
				DELETE:		
W1	8120-3784	7	1	CABLE KEYBD-14 CONDUCTOR	28480	8120-3784
A7	01630-66527	4	1	KEYBOARD ASSEMBLY (INCLUDES KEYCAPS)	28480	01630-66527
				SAME AS 01630-66530 WITH THE FOLLOWING EXCEPTIONS:		
				ADD:		
	1200-0474	9	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
				DELETE:		
W1	8120-3784	7	1	CABLE KEYBD-14 CONDUCTOR	28480	8120-3784
A7	01630-66527	4	1	KEYBOARD ASSEMBLY (INCLUDES KEYCAPS)	28480	01630-66527
W1	8120-3784	7	1	CABLE KEYBD-14 CONDUCTOR	28480	8120-3784
	3101-2947	7	38	KEY SWITCH-SPST	28480	3101-2947
	5041-0433	6	1	KEY CAP (BLUE)	28480	5041-0433
	5041-0655	4	1	KEY CAP-INSERT	28480	5041-0655
	5041-0900	2	1	KEYCAP-A	28480	5041-0900
	5041-0901	3	1	KEYCAP-B	28480	5041-0901
	5041-0902	4	1	KEYCAP-C	28480	5041-0902
	5041-0903	5	1	KEYCAP-D	28480	5041-0903
	5041-0906	8	1	KEYCAP-0	28480	5041-0906
	5041-0907	9	1	KEYCAP-1	28480	5041-0907
	5041-0908	0	1	KEYCAP-2	28480	5041-0908
	5041-0909	1	1	KEYCAP-3	28480	5041-0909
	5041-0910	4	1	KEYCAP-4	28480	5041-0910
	5041-0911	5	1	KEYCAP-5	28480	5041-0911
	5041-0912	6	1	KEYCAP-6	28480	5041-0912
	5041-0913	7	1	KEYCAP-7	28480	5041-0913
	5041-0914	8	1	KEYCAP-8	28480	5041-0914
	5041-2777	5	1	KEYCAP-PREV	28480	5041-2777
	5041-2778	6	1	KEYCAP-NEXT	28480	5041-2778
	5041-2779	7	1	KEYCAP-CHART	28480	5041-2779
	5041-2780	0	1	KEYCAP-WFORM	28480	5041-2780
	5041-2781	1	1	KEYCAP-SYSTEM	28480	5041-2781
	5041-2782	2	1	KYCP-ARROW UP LT	28480	5041-2782
	5041-2783	3	1	KYCP-DON'T CARE	28480	5041-2783
	5041-2784	4	1	KEYCAP-E	28480	5041-2784
	5041-2785	5	1	KEYCAP-F	28480	5041-2785
	5041-2786	6	1	KYCP-ARROW SIDE DK	28480	5041-2786
	5041-2787	7	1	KYCP-ARROW UP DK	28480	5041-2787
	5041-2788	8	1	KEYCAP-RUN	28480	5041-2788
	5041-2789	9	1	KEYCAP-STOP	28480	5041-2789
	5041-2790	2	1	KEYCAP-PRINT	28480	5041-2790
	5041-2791	3	1	KYCP-CLEAR ENTRY	28480	5041-2791
	5041-2792	4	1	KEYCAP-LIST	28480	5041-2792
	5041-2793	5	1	KEYCAP-FORMAT	28480	5041-2793
	5041-2794	6	1	KEYCAP-TRACE	28480	5041-2794
	5041-2795	7	1	KEYCAP-CHS	28480	5041-2795

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8	01630-66508	1	1	TIMING SLAVE ASSEMBLY (1630D ONLY)	28480	01630-66508
A8C1	0160-6500	7	35	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C2	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C3	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C4	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C5	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C6	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C7	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C8	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C9	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C10	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C11	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C12	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C13	0160-5506	1	1	CAPACITOR-FXD 300PF 50VDC	28480	0160-5506
A8C14	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C15	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C16	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C17	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C18	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C19	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C20	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C21	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C22	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C23	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C24	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C25	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C26	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C27	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C28	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C29	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C30	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C31	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C32	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C33	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C34	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C35	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C36	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A8C37	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A8C38	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
A8J1	1251-7705	0	1	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A8MP1	1205-0484	1	2	HEAT SINK SOCKET	28480	1205-0484
A8P1	1251-8729	0	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-8729
A8R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A8RP1	1810-0382	1	13	NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP2	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP3	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP4	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP5	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP6	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP7	1810-0350	3	2	NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A8RP8	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP9	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP10	1810-0350	3		NETWORK-RES 8-SIP100.0 OHM X 4	01121	208B101
A8RP11	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP12	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP13	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP14	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8RP15	1810-0382	1		NETWORK-RES 10-SIP100.0 OHM X 9	01121	210A101
A8U1C	1820-2848	9	4	IC-MC10H116	28480	1820-2848
A8U1D	1820-2848	9		IC-MC10H116	28480	1820-2848
A8U2C	1820-2848	9		IC-MC10H116	28480	1820-2848
A8U2D	1820-2821	8	1	IC-MC10159P	28480	1820-2821
A8U2F	1820-4080	5	2	IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135P
A8U2H	1820-4159	9	3	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A8U2I	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A8U3A	1820-1686	1	1	IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A8U3B	1820-0802	1	3	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U3C	1810-0931	2	2	DELAY LINE- 17NS X 4	28480	1810-0931
A8U3D	1810-0931	2		DELAY LINE- 17NS X 4	28480	1810-0931

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A8U3E	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U3F	1820-1400	7	2	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A8U3H	1820-2023	2	1	IC GATE ECL AND HEX 2-INP	04713	MC10197P
A8U3I	1820-2847	8	1	IC-MC10153P	28480	1020-2847
A8U3J	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A8U4C	1820-2905	9	2	IC-SC25647	28480	1820-2905
A8U4F	1816-1462	2	8	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4G	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U4J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5C	1820-2905	9		IC-SC25647	28480	1820-2905
A8U5F	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5G	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5I	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U5J	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	S0167	MBM10422H
A8U6A	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A8U6B	1820-2849	0	1	IC-MC10H131P	28480	1820-2849
A8U6C	1820-2848	9		IC-MC10H116	28480	1820-2848
A8U6D	1820-1225	4	2	IC FF ECL D-M/S DUAL	04713	MC10231P
A8U6E	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A8U6F	1820-1946	6	1	IC GATE ECL DUAL	04713	MC10117L
A8U6G	1820-1400	7		IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A8U6H	1820-4080	5		IC FF ECL J-BAR K-BAR COM CLOCK DUAL	04713	MC10135P
A8U6I	1820-1788	4	1	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A8XU4C	1200-1001	0	2	SOCKET-68 PIN	28480	1200-1001
A8XU5C	1200-1001	0		SOCKET-68 PIN	28480	1200-1001

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A9	10271A	6	3	STATE MASTER PROBE	28480	10271A
A9MP1				NOT ASSIGNED		
A9MP2				NOT ASSIGNED		
A9MP3				NOT ASSIGNED		
A9MP4	10271-63201	9	1	CLIP ASY-10 CHAN	28480	10271-63201
A9MP5	5959-0288	4	1	GRABBER ASSY (SET OF 20)	28480	5959-0288
	7121-3655	2	1	LABEL-STAT POD 3	28480	7121-3655
	7121-3656	3	1	LABEL-STAT POD 2	28480	7121-3656
	7121-3660	9	1	LABEL-STAT POD 4	28480	7121-3660
	7121-3738	2	1	LABEL-ID 10271A	28480	7121-3738
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901
A10	10272A	7	AR	TIMING PROBE (1631A QTY 1, 1631D QTY 2)	28480	10272A
A10MP1				NOT ASSIGNED		
A10MP2				NOT ASSIGNED		
A10MP3				NOT ASSIGNED		
A10MP4	10272-63201	0	1	CLIP ASSY-8 CHAN	28480	10272-63201
A10MP5	5959-0288	4	1	GRABBER ASSY (SET OF 20)	28480	5959-0288
	7121-3661	0	1	LBL-ST/TIM POD 0	28480	7121-3661
	7121-3662	1	1	LBL-ST/TIM POD 1	28480	7121-3662
	7121-3737	1	1	LABEL-ID 10272A	28480	7121-3737
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11	01630-66517	2	1	STATE SLAVE ASSEMBLY (1630G ONLY)	28480	01630-66517
A11C1	0160-5298	8	80	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C2	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C3	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C4	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C5	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C6	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C7	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C8	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C9	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C10	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C11	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C12	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C13	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C14	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C15	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C16	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C17	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C18	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C19	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C20	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C21	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C22	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C23	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C24	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C25	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C26	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C27	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C28	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C29	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C30	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C31	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C32	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C33	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C34	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C35	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C36	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C37	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C38	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C39	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C40	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C41	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C42	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C43	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C44	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C45	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C46	0160-3508	9	3	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C47	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C48	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C49	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A11C50	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C51	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C52	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C53	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C54	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C55	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C56	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C57	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C58	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C59	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C60	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C61	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C62	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C63	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C64	0160-5309	2	1	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A11C65	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11C66	0160-5329	6	1	CAPACITOR-FXD 47PF +-5% 200VDC CER	28480	0160-5329
A11C67	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C68	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C69	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C70	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C71	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C72	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C73	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C74	0180-0228	6	1	CAPACITOR-FXD 22UF +-10% 15VDC TA	56289	150D226X9015B2
A11C75	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C76	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C77	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C78	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C79	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C80	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C81	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C82	0180-1746	5	2	CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A11C83	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C84	0180-1746	5		CAPACITOR-FXD 15UF +-10% 20VDC TA	56289	150D156X9020B2
A11C85	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C86	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A11C87	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C88	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A11C89	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11C90	0160-5298	8		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-5298
A11CR1	1902-3002	3	1	DIODE-ZNR 2.37V 5% DO-7 PD=.4W	28480	1902-3002
A11DL1	1810-0602	8	1	DELAY LINE 7NS	28480	1810-0602
A11J1	1251-7705	0	3	CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11J2	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11J3	1251-7705	0		CONNECTOR-28 CONTACT (MALE)	28480	1251-7705
A11P1	1251-8729	0	1	CONNECTOR-100 CONTACT (FEMALE)	28480	1251-8729
A11Q1	1853-0006	6	1	TRANSISTOR PNP SI TO 5 PD=600MW	04713	2N3134
A11R1	0757-0401	0	3	RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R2	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0 +-100	24546	C4-1/8-TO-51R1-F
A11R3	0757-0446	3	1	RESISTOR 15K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1502-F
A11R4	2100-2655	1	1	RESISTOR TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
A11R5	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1002-F
A11R6	0698-3226	7	1	RESISTOR 6.49K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-6491-F
A11R7	0699-1000	3	4	RESISTOR 4.25K .1%	28480	0699-1000
A11R8	0699-1000	3		RESISTOR 4.25K .1%	28480	0699-1000
A11R9	0699-1000	3		RESISTOR 4.25K .1%	28480	0699-1000
A11R10	0698-6360	6	4	RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R11	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R12	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R13	0698-6360	6		RESISTOR 10K .1% .125W F TC=0 +-25	28480	0698-6360
A11R14	0699-1000	3		RESISTOR 4.26K .1%	28480	0699-1000
A11R15	0757-0419	0	1	RESISTOR 681 1% .125W F TC=0 +-100	24546	C4-1/8-TO-681R-F
A11R16	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1001-F
A11R17	0757-0404	3	1	RESISTOR 130 1% .125W F TC=0 +-100	24546	C4-1/8-TO-130R-F
A11R18	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-5111-F
A11R19	0757-0401	0		RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R20	0757-0401	0		RESISTOR 100 1% .125W F TC=0 +-100	24546	C4-1/8-TO-101-F
A11R21	0757-0280	3		RESISTOR 1K 1% .125W F TC=0 +-100	24546	C4-1/8-TO-1001-F
A11RP1	1810-0272	8	7	NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP2	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP3	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP4	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP5	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP6	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP7	1810-0272	8		NETWORK RES 10-SIP 330 OHM X 9	01121	210A331
A11RP8	1810-0382	1	14	NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP9	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP10	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11RP11	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP12	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP13	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP14	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP15	1810-0411	7	1	NETWORK RES 10-SIP 50 OHM X 9	56289	256CK500X2PD
A11RP16	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP17	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP18	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP19	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9	01121	210A101
A11RP20	1810-0275	1	3	NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP21	1810-0275	1		NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP22	1810-0275	1		NETWORK RES 10-SIP 1000 OHM X 9	01121	210A102
A11RP23	1810-0382	1		NETWORK RES 10-SIP 100 OHM X 9	01121	210A101
A11RP24	1810-0277	3	2	NETWORK RES 10-SIP 2200 OHM X 9	01121	210A222
A11RP25	1810-0277	3		NETWORK RES 10-SIP 2200 OHM X 9	01121	210A222
A11RP26	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9100	01121	210A33
A11RP27	1810-0382	1		NETWORK RES 10-SIP 330 OHM X 9100	01121	210A33
A11U1A	1820-3461	4	9	IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1B	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1C	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1D	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1E	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1F	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1G	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1H	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1I	1820-3461	4		IC LINE RCVR ECL QUAD	04713	MC10H115P
A11U1K	1820-0806	5	1	IC GATE ECL OR-NOR DUAL 4-5-INP	04713	MC10109P
A11U1L	1820-2508	8	2	IC GATE ECL EXCL-OR QUAD 2-INP	04713	MC10113P
A11U1M	1820-2508	8		IC GATE ECL EXCL-OR QUAD 2-INP	04713	MC10113P
A11U2B	1820-4159	9	11	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2C	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2D	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2E	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2F	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2G	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2H	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2I	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2J	1820-1399	3	4	IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176P
A11U2K	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2L	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U2M	1820-4159	9		IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	85008	MC10H016P
A11U3A	1816-1591	8	13	IC RAM 1K X 4	28480	1816-1591
A11U3B	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3C	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3D	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3E	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3F	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3G	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3H	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3I	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3J	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3K	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3L	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U3M	1816-1591	8		IC RAM 1K X 4	28480	1816-1591
A11U4A	1826-0718	0	1	IC VOLTAGE REGULATOR	28480	1826-0718
A11U4B	1816-1555	4	4	IC RAM 10422-6	28480	1816-1555
A11U4D	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4F	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4H	1816-1555	4		IC RAM 10422-6	28480	1816-1555
A11U4J	1NB4-5009	0	1	IC COUNTER 20 BIT GRAY CODE	28480	1NB4-5009
A11U4M	1826-0271	0	1	IC OP AMP GP 8-DIP-P PKG	01295	SN72741P
A11U5K	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176P
A11U5L	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176P
A11U5M	1820-1399	3		IC FF ECL D-M/S POS-EDGE-TRG COM CLOCK	04713	MC10176P
A11U6B	1826-0753	3	1	IC OP AMP LOW-BIAS-H-IMPD QUAD 14-DIP-C	04713	MS34004BL
A11U6C	1826-0856	7	2	IC CONV 8-BIT-D/A 20-DIP-PKG	34335	AM6080APC
A11U6D	1826-0856	7		IC CONV 8-BIT-D/A 20-DIP-PKG	34335	AM6080APC

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A11U6E	1818-3366	3	4	IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1818-3366
A11U6G	1818-3366	3		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1818-3366
A11U6H	1818-3366	3		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1818-3366
A11U6J	1818-3366	3		IC PROM ELECTRICALLY ERASEABLE (EEPROM)	28480	1818-3366
A11U6K	0960-0530	7	1	IC OSCILLATOR 25MHZ	28480	0960-0530
A11U6L	1820-3124	6	3	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A11U6M	1820-3125	7	4	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A11U7B	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A11U7C	1820-1216	3	1	IC DC DR TTL LS 3-TO-8-LINE 2-INP	01295	SN74LS138N
A11U7D	1820-3299	6	1	IC BFR TTL HC LINE DRVR DUAL-QUAD	28480	1820-3299
A11U7E	1820-3399	7	1	IC FF TTL HC D-TYPE OCTAL	04713	74HC273
A11U7F	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
A11U7G	1820-1917	1	1	IC BFR TTL LS LINE DRVR DUAL-QUAD	01295	SN74LS240N
A11U7H	1820-2096	9	2	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A11U7I	1820-0802	1	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A11U7J	1820-3400	1	1	IC GATE ECL NOR DUAL 3-INP 3-OUT	04713	MC10H211
A11U7K	1820-0817	8	4	IC FF ECL D-M/S DUAL	04713	MC10131P
A11U7L	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U7M	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U8C	1820-3125	7		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A11U8D	1820-3125	7		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A11U8E	1820-3125	7		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A11U8F	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A11U8G	1820-3124	6		IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124P
A11U8H	1820-2096	9		IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
A11U8I	1820-0810	1	1	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A11U8J	1820-2891	2	1	IC MC10H101P	28480	1820-2891
A11U8K	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A11U8L	1820-0803	2	1	IC GATE ECL OR-NOR TPL	04713	MC10105P
A11U8M	1820-0827	0	2	IC DCDR ECL BIN 3-TO-8 LINE	0713	MC10161P
A11U8N	1820-0827	0		IC DCDR ECL BIN 3-TO-8 LINE	0713	MC10161P
A11UR5A	1810-0613	1	2	NETWORK RES 8-DIP	28480	1810-0613
A11UR6A	1810-0613	1		NETWORK RES 8-DIP	28480	1810-0613

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A12	10273A	8	3	STATE SLAVE PROBE (1630G ONLY)	28480	10273A
A12MP1				NOT ASSIGNED		
A12MP2				NOT ASSIGNED		
A12MP3				NOT ASSIGNED		
A12MP4	10273-63201	1	1	CLIP ASSY-10 CHANNEL	28480	10273-63201
A12MP5	5959-0288	4	1	GRABBER ASSEMBLY (SET OF 20)	28480	5959-0288
	10271-90901	3	1	OPERATING NOTE	28480	10271-90901

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13	01631-66501	5	1	ANALOG ACQUISITION BOARD	28480	01631-66501
A13C1	0160-6500	7	51	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C2	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C3	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C4	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C5	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C6	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C7	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C8	0160-5330	9	6	CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C9	0160-5330	9		CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C10	0160-6500	7		CAPACITOR-FXD .01UF +-20% 1000VDC CER	28480	0160-6500
A13C11	0160-5330	9		CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C12	0160-6500	7		CAPACITOR-FXD .01UF +-20% 1000VDC CER	28480	0160-6500
A13C13	0160-5326	3	1	CAPACITOR-FXD 27PF +-5% 200VDC CER	28480	0160-5326
A13C14	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C15	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C16	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C17	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C18	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C19	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C20	0180-0229	7	4	CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A13C21	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C22	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C23	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C24	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C25	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A13C26	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C27	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C28	0180-0291	3	2	CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035B2
A13C29	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C30	0160-5315	0		CAPACITOR-FXD 3300PF +-20% 100VDC CER	28480	0160-5315
A13C31	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C32	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C33	0160-5315	0		CAPACITOR-FXD 3300PF +-20% 100VDC CER	28480	0160-5315
A13C34	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C35	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C36	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C37	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C38	0160-5312	7	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-5312
A13C39	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C40	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C41	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C42	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C43	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C44	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C45	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C46	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C47	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C48	0160-3874	2	2	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A13C49	0160-0574	3	2	CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A13C50	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A13C51	0160-0574	3		CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-0574
A13C52	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9010B2
A13C53	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C54	0160-5330	9		CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C55	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C56	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A13C57	0180-0229	7		CAPACITOR-FXD 33UF +-10% 10VDC TA	56289	150D336X9010B2
A13C58	0180-0116	1	4	CAPACITOR-FXD 6.8UF +-10% 35VDC TA	56289	150D685X9035B2
A13C59	0180-0116	1		CAPACITOR-FXD 6.8UF +-10% 35VDC TA	56289	150D685X9035B2
A13C60	0160-5309	2	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A13C61	0160-5330	9		CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C62	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C63	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C64	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C65	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13C66	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C67	0160-5330	9		CAPACITOR-FXD 56PF +-5% 200VDC CER	28480	0160-5330
A13C68	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C69	0180-0116	1		CAPACITOR-FXD 6.8UF +-10% 35VDC TA	56289	150D685X9035B2
A13C70	0180-0116	1		CAPACITOR-FXD 6.8UF +-10% 35VDC TA	56289	150D685X9035B2
A13C71	0160-5309	2		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-5309
A13C72	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C73	0160-5313	8	4	CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-5313
A13C74	0160-5313	8		CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-5313
A13C75	0160-5299	9	3	CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-5299
A13C76	0160-5299	9		CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-5299
A13C77	0160-5299	9		CAPACITOR-FXD .022UF +-20% 100VDC CER	28480	0160-5299
A13C78	0160-5313	8		CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-5313
A13C79	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C80	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C81	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C82	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C83	0160-6500	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-6500
A13C84	0160-5313	8		CAPACITOR-FXD 1000PF +-5% 100VDC CER	28480	0160-5313
A13C85	0160-3879	7	3	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C86	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13C87	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A13CR1	1901-0040	1	5	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13CR5	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A13H1	0515-0430	3	2	SCREW-MACH M3 X 0.5 6MM-LG PAN-HD-TORX	28480	ORDER BY DESCRIPTION
A13H2	0515-0658	7	2	SCREW-MACH M2 X 0.4 6MM-LG PAN-HD-TORX	28480	ORDER BY DESCRIPTION
A13H3	0515-1401	0	2	SCREW-MACH M2 X 0.4 16MM-LG PAN-HD TORX	28480	ORDER BY DESCRIPTION
A13J1	1250-1842	2	3	CONNECTOR-RF BNC FEM SPCL-MTG 500HM	28480	1250-1842
A13J2	1250-1842	2		CONNECTOR-RF BNC FEM SPCL-MTG 500HM	28480	1250-1842
A13J3	1250-1842	2		CONNECTOR-RF BNC FEM SPCL-MTG 500HM	28480	1250-1842
A13K20C	0490-0617	4	2	RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A13K20F	0490-0617	4		RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A13L1	9100-1788	6	6	CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L2	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L3	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L4	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L5	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L6	9100-1788	6		CHOKE-WIDE BAND ZMAX=680 OHM @ 180MHZ	02114	VK200 20/48
A13L7	9100-1629	4	2	INDUCTOR RF-CH-MLD 47UH 5%	28480	9100-1629
A13L8	9100-1629	4		INDUCTOR RF-CH-MLD 47UH 5%	28480	9100-1629
A13MP1	01631-00601	8	3	SHIELD-RF	28480	01631-00601
A13MP2	01631-00602	9	1	SHIELD-BOTTOM	28480	01631-00602
A13MP3	01631-00603	0	1	SHIELD-TOP	28480	01631-00603
A13P1	1251-7986	9	1	CONNECTOR FEMALE 50-PIN	28480	1251-7986
A13Q1	1853-0036	2	3	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A13Q2	1854-0628	0	7	TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q3	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q4	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q5	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q6	1853-0354	7	8	TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q7	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q8	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q9	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q10	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q11	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q12	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A13Q13	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A13Q14	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q15	1853-0354	7		TRANSISTOR PNP SI TO-92 PD=350MW	28480	1853-0354
A13Q16	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q17	1855-0062	8	3	TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0062
A13Q18	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17

See introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13Q19	1855-0062	8		TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0062
A13Q20	1854-0628	0		TRANSISTOR NPN SI TO-92 PD=625MW	04713	MPS-1+17
A13Q21	1855-0062	8		TRANSISTOR J-FET N-CHAN D-MODE SI	28480	1855-0062
A13R1	2100-0568	1	1	RESISTOR TRMR 100 10% C SIDE-ADJ 2-TRN	28480	2100-0568
A13R2	0757-0427	0	1	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1501-F
A13R3	0698-3447	4	4	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A13R4	0757-0449	6	2	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2002-F
A13R5	0757-0449	6		RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2002-F
A13R6	0757-0442	0	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A13R7	0757-0283	6	2	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A13R8	0698-4416	9	1	RESISTOR 169 1% .125W F TC=0+-100	24546	C4-1/8-TO-169R-F
A13R9	0698-3430	5	2	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-TO-21R5-F
A13R10	0698-3441	8	5	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A13R11	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A13R12	0698-4002	9	5	RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R13	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R14	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R15	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R16	0698-4207	6	1	RESISTOR 44.2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4422-F
A13R17 *	0698-4442	1	1	RESISTOR 4.42K 1% .125W F TC=0+-100 See Section 7 History #30	24546	C4-1/8-TO-4421-F
A13R18	0757-0200	7	6	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-TO-21R5-F
A13R20	0698-4453	4	9	RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R21	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A13R22	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A13R23	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-TO-422R-F
A13R24	0757-0280	3	11	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R25	0757-0388	2	2	RESISTOR 30.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-30R1-F
A13R26	0757-0273	4	1	RESISTOR 3.01K 1% .125W F TC=0+-100	24546	C4-1/8-TO-3011-F
A13R27	0757-0388	2		RESISTOR 30.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-30R1-F
A13R28	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R29	0757-0401	0	5	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A13R30	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A13R31	0757-0411	2	11	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R32	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R33	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R34	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R35	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R36	0698-4037	0	2	RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
A13R37	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R38	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A13R39	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A13R40	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R41	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R42	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R43	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R44	0698-4037	0		RESISTOR 46.4 1% .125W F TC=0+-100	28480	0698-4037
A13R45	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R46	0698-5137	3	1	RESISTOR 46.4 1% .25W F TC=0+-100	24546	C5-1/4-TO-47R0-D
A13R47	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-TO-101-F
A13R48	0698-3435	0	4	RESISTOR 38.3 1% .125W F TC=0+-100	24546	C4-1/8-TO-38R3-F
A13R49	0698-3439	4	3	RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-TO-178R-F
A13R50	0698-3558	6	2	RESISTOR 4.02K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4021-F
A13R51	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R52	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R53	0698-4453	4		RESISTOR 402 1% .125W F TC=0+-100	24546	C4-1/8-TO-402R-F
A13R54	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R55	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-TO-511R-F
A13R56	0698-3558	6		RESISTOR 4.02K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4021-F
A13R57	0757-0409	8	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A13R58	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R59	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R60	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-TO-562R-F
A13R61	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R62	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R63	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13R64	0698-6250	3	2	RESISTOR 2.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2501-F
A13R65	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R66	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-TO-178R-F
A13R67	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R68	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R69	0757-0200	7		RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5621-F
A13R70	0757-0420	3	1	RESISTOR 750 1% .125W F TC=0+-100	24546	C4-1/8-TO-751-F
A13R71	0757-0417	8		RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-TO-562R-F
A13R72	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R73	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R74	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R75	0698-6250	3		RESISTOR 2.5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2501-F
A13R76	0698-4002	9		RESISTOR 5K 1% .125W F TC=0+-100	24546	C4-1/8-TO-5001-F
A13R77	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A13R78				NOT ASSIGNED		
A13R79	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A13R80	0757-0404	3	1	RESISTOR 130 1% .125W F TC=0+-100	24546	C4-1/8-TO-131-F
A13R81	0698-3439	4		RESISTOR 178 1% .125W F TC=0+-100	24546	C4-1/8-TO-178R-F
A13R82	0757-0409	8		RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A13R83	2100-0567	0	1	RESISTOR TRMR 2K 10% C TOP-ADJ 1-TRN	28480	2100-0567
A13R84	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R85	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A13R86	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R87	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R88	0698-3435	0		RESISTOR 38.3 1% .125W F TC=0+-100	24546	C4-1/8-TO-38R3-F
A13R89	0698-3441	8		RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-TO-215R-F
A13R90	0757-0283	6		RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2001-F
A13R91	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R92	0698-3435	0		RESISTOR 38.3 1% .125W F TC=0+-100	24546	C4-1/8-TO-38R3-F
A13R93	0757-0394	0	2	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A13R94	0757-0274	5	1	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1211-F
A13R95	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R96	0698-8957	1	6	RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R97	0698-8957	1		RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R98	0698-3435	0		RESISTOR 38.3 1% .125W F TC=0+-100	24546	C4-1/8-TO-38R3-F
A13R99	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A13R100	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1211-F
A13R101	0757-0411	2		RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-TO-332R-F
A13R102	0698-8957	1		RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R103	0698-8957	1		RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R104	0698-8957	1		RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R105	0698-8957	1		RESISTOR 500K 1% .125W F TC=0+-100	28480	0698-8957
A13R106	0698-6320	8		RESISTOR 5K 0.1% .125W F TC=0+-25	24546	0698-6320
A13R107	0699-0273	0	1	RESISTOR 2.15K 0.1% .125W F TC=0+-25	24546	0699-0273
A13RP1	1810-0272	8	7	NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP2	1810-0382	1	6	NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP3	1810-0382	1		NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP4	1810-0382	1		NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP5	1810-0382	1		NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP6	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP7	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP8	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP9	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP10	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP11	1810-0272	8		NETWORK-RES 10-SIP 330.0 OHM X 9	01121	210A331
A13RP12	1810-0495	7	1	NETWORK-RES 8-SIP 51.0 OHM X 7	28480	1810-0495
A13RP13	1810-0382	1		NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP14	1810-0382	1		NETWORK-RES 10-SIP 100.0 OHM X 9	01121	210A101
A13RP15	1810-0755	2	3	NETWORK-RESISTOR SPECIAL	28480	1810-0755
A13RP16	1810-0755	2		NETWORK-RESISTOR SPECIAL	28480	1810-0755
A13RP17	1810-0755	2		NETWORK-RESISTOR SPECIAL	28480	1810-0755
A13U1A	1816-1462	2	12	IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U2A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U3A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U3C	1820-4159	9	7	IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U3D	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P

See Introduction to this section for ordering information

Table 6-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A13U3E	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U3F	1820-2821	8	2	IC MUX ECL QUAD 2-INP	04713	MC10159P
A13U3H	1820-3125	7	3	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A13U3I	1826-1246	1	3	IC CONV 12-B-D/A 28-DIP-P PKG	28480	1826-1246
A13U3K	1826-1246	1		IC CONV 12-B-D/A 28-DIP-P PKG	28480	1826-1246
A13U3L	1826-1246	1		IC CONV 12-B-D/A 28-DIP-P PKG	28480	1826-1246
A13U4A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U5A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U5C	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U5D	1820-2962	8	2	IC GATE ECL OR QUAD 2-INP	04713	MC10H103P
A13U5E	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U5F	1820-2821	8		IC MUX ECL QUAD 2-INP	04713	MC10159P
A13U5H	1820-3125	7		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A13U5I	1820-1858	9	1	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
A13U5J	1826-0856	7	3	IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A13U5K	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A13U5L	1826-0856	7		IC CONV 8-B-D/A 20-DIP-P PKG	34335	AM6080APC
A13U6A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U7A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U7C	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U7D	1820-4159	9		IC CNTR ECL PROGRAMMABLE DIV-BY-16	04713	MC10H016P
A13U7E	1820-2849	0	7	IC FF ECL DUAL M-S	04713	MC10H131P
A13U7F	1820-3831	2		IC MUX ECL DUAL 4-INP	04713	MC10H174
A13U7H	1820-2522	6	1	IC BFR ECL NON-INV HEX	18324	GXB10188P
A13U7I	1820-2496	3	2	IC LTCH ECL D-TYPE POS-EDGE-TRIG COM	04713	MC10175L
A13U7J	1820-2496	3		IC LTCH ECL D-TYPE POS-EDGE-TRIG COM	04713	MC10175L
A13U7K	1820-0810	1	2	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A13U8A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U8F	1826-1099	2	2	IC VOLTAGE REFERENCE	28480	1826-1099
A13U9A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U9C	1820-2962	8		IC GATE ECL OR QUAD 2-INP	04713	MC10H103P
A13U9D	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MLM324P
A13U9F	1826-1099	2		IC VOLTAGE REFERENCE	28480	1826-1099
A13U9H	1820-0827	0	1	IC DCDR ECL BIN 3-TO-8-LINE	04713	MC10161P
A13U9I	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U9J	1820-3125	7		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125P
A13U9K	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A13U10A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U11A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U11H	1820-3337	3	1	IC GATE ECL AND QUAD 2-INP	04713	MC10H104
A13U11I	1820-0802	1	1	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A13U11J	1820-1686	1	2	IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A13U11K	1820-1400	7	1	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A13U12A	1816-1462	2		IC ECL/10K 1024 (1K) STAT RAM 10-NS O-E	50167	MBM10422H
A13U12D *	1NB4-5013	6	2	IC HYBRID A/D See Section 7 Instrument History	28480	1NB4-5013
A13U12F *	1NB4-5013	6		IC HYBRID A/D See Section 7 Instrument History	28480	1NB4-5013
A13U13H	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U13I	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U13J	1820-1686	1		IC GATE ECL OR QUAD 2-INP	04713	MC10103P
A13U14A	1858-0058	8	1	IC TRANSISTOR ARRAY	28480	1858-0058
A13U15E	1820-0810	1		IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10116P
A13U15F	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U15G	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U15H	1820-2849	0		IC FF ECL DUAL M-S	04713	MC10H131P
A13U17A	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N
A13U17C	1NB7-8033	2	1	IC HYBRID AMPLIFIER	28480	1NB7-8033
A13U20A	1826-0433	6	3	IC OP AMP LOW-BIAS-H-IMPD 8-DIP-P PKG	27014	LF356BN
A13U20B	1826-0433	6		IC OP AMP LOW-BIAS-H-IMPD 8-DIP-P PKG	27014	LF356BN
A13U20D	1826-0433	6		IC OP AMP LOW-BIAS-H-IMPD 8-DIP-P PKG	27014	LF356BN
A13XU3F	1200-0567	0	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A13XU3K	1200-0567	0		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A13XU3L	1200-0567	0		SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
A13XU12	1200-1162	4	2	SOCKET-HYBRID 65-PIN	28480	1200-1162
A13XU12	1200-1162	4		SOCKET-HYBRID 65-PIN	28480	1200-1162

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
C0633	RIFA	BROMMA	SE	
S0167	FUJITSU LTD	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
1B546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92806
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	N.V. PHILIPS-ELCOMA DEPARTMENT	EINDHOVEN	HL	02876
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52763	STETTNER ELECTRONICS INC	CHATTANOOGA	TN	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
73138	BECKMAN INSTRUMENTS INC HELIPOT DIV	FULLERTON	CA	92634
75915	LITTELFUSE INC	DES PLAINES	IL	60016

SECTION VII
INSTRUMENT CHANGES

7-1. INTRODUCTION

This section contains information describing how this manual documents changes in the instrument. Because of the service philosophy for this instrument, this service manual is not shipped with every instrument. This service manual is therefore required to cover all versions (serial prefixes) of the 1630A/D/G and 1631A/D families simultaneously. As a result, the organization of change information is different in this manual than it is in most Hewlett-Packard service manuals.

7-2. MANUAL CHANGES

This manual applies directly, or with changes, to instruments having serial prefixes as noted on the manual title page. If the serial prefix of your instrument is not mentioned on the title page, a Manual Changes Supplement may need to be ordered.

An attempt has been made to put change information in close proximity to the information it replaces. For example, changes to an assembly part list are located in Section VI in the assembly part list affected (see Section VI). Differences in schematics due to changes are located on the schematic changed or in close proximity to it. The purpose of this section, Section VII, is to provide a synopsis of the changes made in the instrument family whether or not covered directly by a different serial prefix.

7-3. HP 1630A/D/G, 1631A/D INSTRUMENT CHANGES

Table 7-1 shows the relationship between serial prefixes and the complement of boards in an HP 1630A/D/G or 1631A/D as shipped from the factory. This table should not be used to determine what number to use to order a replacement board because recent boards usually directly replace older ones. For this same reason, a given instrument may have different boards than it was originally shipped with if a Blue-stripe exchange was used to repair it.

Instruments are also up and down-gradable to other versions within the family. For example, A 1630A can be converted to a 1630D or 1630G and the 1630G can be converted to a 1630D. This can cause different relationships between model numbers, serial prefixes, and board complements, than is shown in this manual.

Table 7-2 gives a quick reference to parts that have been changed on the major assemblies since the introduction of the instrument. If there is a discrepancy with a part on one of your assemblies you can check under the assembly reference to see if it has been part of any changes. The History No. reference on the left shows where in the Instrument Family History additional information may be found about that change. Any part change applies to all instruments of the family being built at that time unless otherwise noted in the History # column.

Unless otherwise noted, changes made in a revision of a board/assembly will be present in subsequent revisions of that board/assembly.

The Instrument Family History, paragraph 7-4, gives a brief description of each change noted in table 7-2. References are made to schematics and other information which may be helpful in discerning how the change applies to the instrument being serviced.

Table 7-1. Board Complements vs. Serial Prefixes.

	BOARD NUMBERS USED[1]									
SERIAL PREFIXES	A1 POWER SUPP	A2 M.B.	A3 CPU[9]	A4 STATE MSTR	A5 TIMING MSTR	A6 DISPLY	A7 KYBRD	A8[2] TIMING SLV	A11[3] STATE SLV	A13[4] ANALG
1630A - 2242A 1630D - 2234A	66502		66503	66505	66506					
1630A/D - 2311A			66503	66509		0950- 0894				
1630A/D - *NOTE 5*			66512	66909	66510					
1630A/D - 2412A	66514	– –	66522	– –		– –	66504	– –		
1630G - 2415A	66514		66519		66524		– –			
1630A - 2428A 1630D - 2424A	*NOTE 6*		66515		*NOTE 7*	*NOTE 8*				
1630G - 2425A	*NOTE 6*	– –	66526	– –	– –	*NOTE 8*		– –	– –	
1631A - 2451A 1631D - 2446A										
1631A - 2505A 1631D - 2503A			66528							
1630A/D - 2511A	– –	– –					66527			
1630G - 2510A	66525		66526							
1631A - 2509A		66501		66518				66508		
1631D - 2510A			66528							
1630A - 2515A							*NOTE*			
1630D - 2514A			66532		66524		*10*		66517	
1631A - 2525A 1631D - 2518A			66532			0950- 1692				
1631A - 2540A		– –	66533							66501
1630A - 2605A 1630D - 2602A			66533							
1630G - 2602A			66526							
1631A - 2605A/2645A	66529						66530			
1631D - 2551A/2641A	– –	– –	66533							
1631A - 2714A 1631D - 2713A										
1630A - 2715A 1630D - 2720A			66535							
1630A/D/G - 2812A 1631A/D - 2811A	66534									

NOTES:

1. All board numbers except the display and analog board should be prefixed with "01630-".
2. 1630D and 1631D only.
3. 1630G only.
4. 1631A/D only. Board is prefixed "01631-".
5. Serial numbers: 1630A, 2311A00231 and up; 1630D, 2311A00791 and up.
6. Change to 66525 board is indefinite.
7. Change to 66524 board is indefinite.
8. Change to 0950-1692 board is indefinite. See #15 in Instrument Family History.
9. 1630A/D Option 007 uses a different CPU, see parts list.
10. Change to 66530 board is indefinite. See #25 in Instrument Family History.

Table 7-2. Part Changes Quick-reference Table.

	MAJOR ASSEMBLIES							
HIS-TORY #	**MAINFRAME**	**A1 POWER SUPPLY**	**A3 CPU**	**A4 STATE MASTER**	**A5 TIMING MASTER**	**A8[5] TIMING SLAVE**	**A11[1] STATE SLAVE**	**A13[2] ANALOG**
1				U3J-L U7B U5E U6H				
2			U3A-D,U4A-D	U8K				
3				U6B-E U7E-H	U1K,L U2K,L U7C U9K,L	U2H,I		
4			C1,2 CR1,2 T1					
5	A4,A5			U4L U8K				
6			A3A1					
7					C26			
8	A3		C1,2 CR1,2 T1					
9		RV2						
10			U3F U4F					
11	A1,A3,A4 B1,MP1-5,W5			U3A-C,E-G,I U2B-C,E-I				
12		E1,2 RT1,2						
	1630G STARTS							
13[1]			U3H-K U4H-K					
14	A3		HP-IL J1,J2 U2D U3P,Q					
15	A6							
16	A1	MP8						
17	A5							
18		R15			200MHz osc			
19			U3A-D,U4A-D					
20[1]			U3H,I U4H					
	1631A/D STARTS							
21[2]			U3H-K,U4H-K					
22			J1,J4					
23			C35,R16					
24	A3[3] H7-9,19,20 MP4,6,9-11,20-22							
25	A7		C61,62				C82,84	R16,17 R36,44,55
26[4]	A3		U3H					
27			U6M U7M 8J-L U9I-L	U2B,C,E-I,L U3J-L,N U6B-E,L,M U7C,E-H	U1J-L U2I,K,L U3H U4C,5C,6D U7C U9J-L	U2F,H,I U3A U6H	U2B-M U5K-M U6L,M U8C-G	U3C-E U5C,E U7C,D U11J,13J
28	A1, A3, B1	E5,6 H3-5 R37,43 P2	U4H,I					
29		RT3		U5F,G,I	U4F,5F	U3C,D		
30[2]								R17 U12D,F
31[4]			U3H-K U4H-K					
32	B1							
33	1631A/D Probes	R19,50	U20					
34	A1							

NOTES: 1. 1630G only, 2. 1631A/D only, 3. 1630A/D only, 4. 1630/31A/D only, 5. 1630/31D only

7-4. INSTRUMENT FAMILY HISTORY

Following is a history of the major changes in the 1630 models. A change applies to all models unless otherwise specified.

1. **State Master Board (01630-66505)**

   Change to higher speed parts.

   a) U3J-L changed to 1820-3102
   b) U5E changed to 1816-1555
   c) U6H changed to 1816-1554
   d) U7B changed to 1820-2823

2. **CPU (01630-66503) and State Master (01630-66505) Boards**

   On the CPU the RAM was changed to a plastic part, 1818-3005.

   On the State Master U8K was changed to 1820-2495.

3. **State Master (01630-66505), Timing Master (66506), Timing Slave (66508) Boards**

   Parts were changed, on the State Master and Timing Master and Slave boards, to a preferred part. Most (not all) 1820-1788 were changed to 1820-3102. On the State Master A4, U2B-C, E-I were not changed because the new part is not compatable with the RAM that these parts drive. Parts involved were:

   a) On State Master A4; U6B-E; U7E-H.
   b) On Timing Master A5; U1K,L; U2K,L; U7C; U9K,L.
   c) On Timing Slave A8; U2H,I.

4. **CPU Board (01630-66503); RFI**

   An RFI problem necessitated isolating part of the HP-IL circuitry on the CPU board A3. Several parts were removed from the main board, 01630-66503, and mounted on a small board piggy-backed to the main board. There was no serial prefix change.

   a) Effective instruments were:
      1) 1630A - serial number 2242A00121 and up.
      2) 1630D - serial number 2234A00241 and up.

   b) Parts affected were:
      1) Removed from 01630-66503 were C1,2; CR1,2; T1.
      2) Piggy-back board was 01630-66511 loaded with the parts listed above.

5. Serial Prefix Change; State Master (01630-66505/09), Timing Master (66506/10)

1630A from 2234A to 2311A
1630D from 2242A to 2311A

a) State Master board changed from 01630-66505 to 01630-66509. The 66509 directly replaces the 66505.

1) U4L changed from 1820-2451 to 1820-2959.
2) U4L circuitry layed out to accomodate the new part (schematic 8C-7).
3) Traces removed between U3N-14 and U4M-4 (schematics 8C-2 and 8C-7).
4) Traces removed between U3N-15 and U4L-10/U6K-5 (schematics 8C-2 and 8C-7).
5) Traces to U6G-12, 13, 14, and 15 removed (schematic 8C-4).
6) U8K changed from 1820-2495 to 1820-2963 (prefered part).

b) Timing Master board changed from 01630-66506 to 01630-66510. The 66510 directly replaces the 66506.

The gate of U7D comprised of pins 9, 12, 13 and 15 was swapped with the gate of U7D comprised of pins 2, 4, 5. See Schematic 8D-3.

6. CPU Board (01630-66503); ESD

An electrostatic discharge (ESD) problem with the HP-IL chip on the CPU board necessitated the addition of protective parts. A small PC board was made to hold the HP-IL chip, U2O, and the added parts and that was plugged into the HP-IL chip socket. There was no instrument serial prefix change or CPU board number change. This is also covered by Service Note 1630A/D-1.

a) The parts added were:

1) PC board, A3A1	01630-66513(includes all other parts)
2) Resistor, A3A1R1	0683-4705
3) Capacitor, A3A1C1	0160-5246
4) Diodes, A3A1CR1-4	1901-0050
5) Socket	1200-0567
6) 14 pin post set (2)	1251-5064

b) Schematic documentation for this change is on schematic 8B-7.

7. Timing Master Board (01630-66510); C26

The trimmer capacitor for the 200MHz oscillator, C26, was changed from a 5.5-18pF to a 2-8pF to increase start-up reliability. See Service Note 1630A/D-2.

8. CPU Board (01630-66503/12); RFI

This change incorporated the final fix for the RFI problem on A3 CPU which was corrected without prefix change (#4 above). It also incorporated a change to the reset timing circuitry on the CPU. There was no instrument serial prefix change.

a) Effective instruments were:
1) 1630A - serial number 2311A00231 and up.
2) 1630D - serial number 2311A00791 and up.

b) A3 CPU changed from 01630-66503 to 01630-66512. The 66503 board is directly replaced by the 66512 board.

c) The small piggy-back board with the HP-IL transformer (#4 above) was deleted and the parts on it were moved back to the main board.

d) The new A3 incorporated a re-layout which moved the connection of U3 pin 11 from U7 pin 1 to U7 pin 7. Schematic changes are noted on schematic 8B-2.

e) U2O pin 2 was pulled up to +5V using RP2 pin 9, schematic 8B-7.

9. Power Supply Board (01630-66502); RV2

A turn-on surge problem when running the instrument with 240VAC input was corrected on A1, Power Supply. Transient suppressor RV2 was changed to a higher voltage value. This is a prefered part change and the new part should be used for all replacements.

10. CPU Board (01630-66512); U3F and U4F

U3F and U4F were changed for production economics reasons. The part number in the present parts list should be used.

11. Serial Prefix Change; Mainframe, Fan, Power Supply (01630-66502/14), CPU (66512/22), State Master (66509/18)

1630A from 2311A to 2412A
1630D from 2311A to 2412A

a) Several mainframe parts were changed to allow more direct retrofit of the 1630A and 1630D to the new 1630G. Changes are noted in the parts list. One of the changed parts was the top cover and pouch. The old top cover and pouch are no longer available.

The old pouch will not fit the new top cover so a new pouch must be ordered if the top cover is replaced.

Also, the rear card cage cover and door were changed. The new parts are not compatable with the old, and the old are no longer available, so both must be replaced if one or the other is needed.

b) To eliminate turn-on surge problems the fan was changed from a 120V type to a 120/240V model. This also necessitated the change of the power supply board from 01630-66502 to 01630-66514. The 66514 board directly replaces the 66502 board but a new fan must be used with the new power supply board. Schematic changes are on Schematic 8A-1.

c) The CPU board was changed from 01630-66512 to 01630-66522. This allowed the basic board (with different PROM and part number) to be used in the 1630G. Schematic changes are noted on Schematic 8B-1.

d) The State Master board was changed from 01630-66509 to 01630-66518. The 66518 board directly replaces the 66509 board. Schematic changes are noted on Schematic 8C-7. Parts changes are noted in the Parts List.

NOTE: The primary parts changed were U3A-C,E-G,I from 1816-1492 to 1816-1591 and U2B-C,E-I from 1820-1788 to 1820-3102. When replacing any of these parts it should be noted that the new RAM, 1816-1591, will work with the old counter, 1820-1788, but the new counter, 1820-3102, will not work with the old RAM, 1816-1492. Any replacement of counters on older boards must use the older part number.

12. Power Supply Board (01630-66514); E1-E2, RT1-RT2

Ineffectiveness coupled with reliability problems necessitated the removal of several parts on the power supply board. Neon bulbs A1E1 and A1E2 were removed from the circuit. In addition, RT1 and RT2, in series with E1 and E2 respectively, were removed. See Service Note 1631A/D/G-4. Effective instruments were:

1630A - serial number 2412A00809 and up.
1630D - serial number 2412A03411 and up.
1630G - serial number 2415A00172 and up

13. CPU Board (01630-66519/26); PROM (1630G Only)

The 1630G CPU, 01630-66519 or 016730-66526, had a PROM change to correct firmware bugs. This is also covered in Service Note 1630G-5(5A). All eight PROMs were changed.

14. Serial Prefix Change; CPU ESD (01630-66515/19/22/26), U3P, U3Q, U2P

1630A	from 2412A to 2428A
1630D	from 2412A to 2424A
1630G	from 2415A to 2425A

This change incorporated a change in CPU boards. This was the final fix for the changes in #6 above. The parts on the ESD board were incorporated on the main CPU board. The CPU for the 1630A/D was changed from 01630-66522 to 01630-66515. The CPU for the 1630G was changed from 01630-66519 to 01630-66526. Both new boards directly replace the older boards.

Two new ICs were added. To make room for the new parts, U3P was moved and it's reference changed to U2P. The new parts were referenced U3P and U3Q.

15. Display Driver Board (0950-0894/1692)

The Display Driver board is supported as a complete replacement part only. During the run of prefixes 2428A (1630A), 2424A (1630D), and 2425A (1630G) the part number was changed from 0950-0894 to 0950-1692. There was no exact changeover time, so any instrument with these prefixes may have either board. The only effect of this change reflects in the way the board is adjusted. There is an added adjustment on the later board. See Section V of this manual for additional information.

16. Power Supply Board (01630-66514/25)

The power supply board was changed from 01630-66514 to 01630-66525. There was no serial prefix change for this board change. The new board directly replaces the old board. The changes to the parts complement of the board were minimal. Most changes were related to trace layout. Any part changes are shown in the parts lists.

17. Timing Master Board (01630-66510/24); 200MHz Osc

The Timing Master board for the 1630A and 1630D was changed from 01630- 66510 to 01630-66524. There was no serial prefix change for this board change. The new board directly replaces the old board. The new board incorporates a packaged 200MHz oscillator rather than one of discrete components. This board was used in all 1630G but incorporated into the 1630A and 1630D later.

18. Power Supply Board (01630-66525); R15

A resistor was changed on the power supply board to prevent a start-up current limit problem due to increased demand by the 1630G. R15 was changed from 68.1Ω to 51.1Ω (0757-0394). This change was covered in Service Note 1630G-2.

19. CPU Board (01630-66515/26); RAM

The dynamic RAM on all versions of the CPU board was changed to a faster part. The part number was changed from 1818-3005 to 1818-3059. The new part directly replaces the old part on all CPU boards.

20. CPU Board (01630-66526); PROM (1630G ONLY)

Three PROMs were changed to correct minor bugs in the firmware. There was no serial prefix or board number changes for this change. These parts are changed in the field as the errors become known. Only the new parts are listed in the Parts List. The old parts cannot be ordered. The affected parts are A3U3I, A3U3H, and A3U4H. Additional information is covered in Service Note 1630G-5A.

21. Serial Prefix Change (01630-66528); CPU PROM (1631A/D ONLY)

1631A from 2451A to 2505A
1631D from 2446A to 2503A

Beginning with these prefixes, the new PROMs corrected several firmware bugs. The PROM change is a warranty always repair and all 1631A/D with the older prefixes should have their entire PROM set changed to the new devices. The part number for the CPU board was not changed for the new PROMs and instrument prefixes are not changed when new PROMs are installed as part of the warranty repair. See Service Note 1631A/D-1A for further information about this warranty repair. The parts list for the CPU board A3 (Section 6) reflects the new PROMs.

22. CPU Board (01630-66526/28); BNC

The CPU output BNCs were changed to an all-metal type to reduce RFI in the 1631A/D. Care should be taken when replacing plastic BNCs with metal ones. Some board traces are routed under the BNC and may short to the BNC if precautions are not taken. Plastic BNCs which have pins that are soldered to the board (1250-1774) should be replaced with the same type. See the Parts Lists in Section 6.

23. CPU Board (01630-66515/26/28); C35 and R16

On the CPU board, high field failures of C35 were corrected by changing it to a film type part. The value of C35 was reduced to conform to size constraints. The value of R16 was changed to maintain the proper time constant in the circuit. Replacement of C35 should be with the newer part so R16 must be changed as well. See Parts List in Section 6.

There is no serial prefix or serial number tracking on this change. This change is also covered by Service Note 1630A/D/G 1631A/D-1.

24. Serial Prefix Change; Metric Mainframe, CPU (01630-66515/28)

1630A	from 2428A to 2511A
1630D	from 2424A to 2511A
1630G	from 2425A to 2510A
1631A	from 2505A to 2509A
1631D	from 2503A to 2510A

The primary change for this prefix was incorporation of metric mainframe parts. New and old parts are noted in the Parts List, Section 6.

One part changed is the top cover. The new top cover has a metric screw. The old top cover is obsolete. The new top cover is supplied with a non-metric screw and retaining ring which can be installed to use the cover on a non-metric instrument.

On the 1630A/D, the CPU board was changed from 01630-66515 to 01630-66528. The 66528 board does not directly replace the 66515 board. The 66515 board has firmware which uses HP-IL (cassette drive) for mass storage transfer and the 66528 board firmware uses HP-IB (floppy disk drive) for mass storage transfer. This was a change to the same board already used in the 1631A/D.

25. CPU (01630-66526/28), State Slave (66517), Analog (01631-66501), and Keyboard (01630-66527/30)

The following changes were made without a serial prefix change.

A capacitor on the + and - 12V lines was changed to provide a greater voltage rating margin. On the CPU C61 and 62 and on the State Slave C82 and C84 were changed.

On the 1631A/D analog board R16 was changed from 50K to 44.2K and R17 from 3.01K to 3.48K to optimize the thresholds in the A/D converter. R36 and R44 were changed from 68.1Ω to 46.4Ω to increase the pull-down current in the output of the A/D converter. R55 was changed from 402Ω to 511Ω to increase the trigger sensitivity.

All replacements in the above cases should use the parts listed in the present parts list. In the case of the resistor pairs, R16 and R17, if one is changed to the new value the other must be changed to the new value as well.

The keyboard was changed by soldering the cable directly to the board to prevent intermittent problems. The new board (01630-66530) directly replaces the old board (01630-66527). Since the new board comes with a cable the old cable may be discarded. The old cable is available for replacement purposes and is listed in the parts list.

26. Serial Prefix Change; CPU PROM (1630A/D, 1631A/D)(01630-66528/32)

1630A	from 2511A to 2515A
1630D	from 2511A to 2514A
1631A	from 2509A to 2525A
1631D	from 2510A to 2518A

One CPU PROM was changed to correct a bug in the 1630A/D firmware. U3H was changed from 01630-80046 to 01630-80051. The CPU board part number was changed from 01630-66528 to 01630-66532. The 66532 board directly replaces the 66528 board. Service Note 1630A/D-6 covers this change.

27. CPU Boards (01630-66515/26/32) U6M, IC Part Number Changes (all digital boards)

On the CPU board System Timing Controller, U6M, was upgraded to a more up-to-date version. The parts list gives only the new part, which should be used for all replacements.

For production economics reasons, several ICs were changed from ceramic to plastic packages. There was no prefix change for this change. The CPU and all acquisition boards are affected by the changing of one or more of these parts. The old and new parts are completely interchangable. See table 7-2 for parts changed.

OLD PART	NEW PART
1820-0820	1820-4080
1820-1052	1820-3125
1820-1173	1820-3124
1820-1831	1820-1686
1820-2193	1820-1399
1820-3102	1820-4159

28. Serial Prefix Change; Fan, Power Supply (01630-66525/29), CPU PROM (01630-66532/33)

1630A	from 2515A to 2605A
1630D	from 2514A to 2602A
1630G	from 2510A to 2602A
1631A	from 2525A to 2540A to 2605A
1631D	from 2518A to 2551A

These prefix changes incorporate two changes in the 163X family. Both changes were made at the same time (on a given family member) with exception of the 1630G which did not get the PROM change and the 1631A in which the changes were done in two steps.

a. Two CPU PROMs were changed to correct a firmware bug in which showed up only in the 1631A. It was necessary to change the 1631A right away. However to simplify matters, the PROM changes to the other family members were incorporated into the next prefix change. The PROM changes also changed the part number of the CPU board for the 1630/31A/D from 01630-66532 to 01630-66533. The 01630-66533 directly replaces the 01630-66532. The 1630G uses a completely different PROM set so it was not affected by this change.

b. In the second change, the fan was changed to a DC model. The power supply board was changed to accomodate this. The fan connector was changed, a resistor in series with the fan was added, and R37 was changed to increase the current limit of the +5V power supply.

   The new power supply board, 01630-66529, directly replaces the old board, 01630-66525, with the provision that the fan is changed also. If an older instrument needs a new power supply, the factory service department should be consulted for additional information.

   In addition, the material used between devices and heatsinks was changed from thermal compound to a special thermal conductive part, E5 and E6 in the parts list.

29. Power Supply (01630-66529), Timing Master (66508), Timing Slave (66524), State Master (66518)

The following changes were made without a serial prefix change.

a. On power supply board 01630-66529, RT3 was changed from 2.5Ω to 5Ω to provide more input surge protection. The new part is preferred and should be used for all replacements of RT3.

b. On the Timing Master and Timing Slave boards the delay IC was changed to a 17 ns part. The new part is compatible with the old and should be used for all replacements.

c. On State Master 01630-66518, U5F, U5G, and U5I were changed to a different part number. The new part is compatible with old parts and should be used for all replacements.

30. Serial Prefix Change; 1631A/D, Analog Board (01631-66501)

1631A from 2605A to 2645A
1631D from 2551A to 2641A

The serial prefix was changed to provide tracking of a change in the ADC hybrids, U12D and U12F. In conjunction with the new hybrid was a change of R17, from 3.48K to 4.42K, to provide more optimal biasing.

R17, 4.42K, as listed in the parts list, is compatible with all ADCs and should be used for any replacement.

On instruments with any serial prefix, if an ADC is changed (U12D or F), R17 should be checked. It should be changed if it is not 4.42K.

31. Serial Prefix Change; CPU PROM (01630-66533/35)

1630A	from 2605A to 2715A
1630D	from 2602A to 2720A
1631A	from 2645A to 2714A
1631D	from 2641A to 2713A

The CPU board part number was changed from 01630-66533 to 66535. This reflects a change in the PROMS. The new board is a direct replacement for the old.

All CPU PROMS were changed to correct firmware bugs. If a PROM must be changed because of failure, the entire set must be replaced. The parts list reflects the new parts.

32. Fan Change

The fan was changed to a more reliable part. The parts list reflects the new fan, which is a preferred part.

33. CPU 01630-66515/26/33/35, Power Supply 01630-66529, 1631A/D Divider Probes.

Several changes were made without prefix changes.

a. The HP-IL IC part number was changed from 1LB3-0003 to 1LR4-0002. The parts list reflects the new part which is a preferred part.

b. A change was made on the power supply assembly to optimize performance. One resistor, R19, was changed from 619K to 68.1K and R50, 75K, was added. The parts list and schematic for the 66529 board reflect the changes.

c. The probes shipped with the 1631A/D were changed to a model from a new probe family. The old probe was 10017A and the new, 10435A.

34. Serial Prefix Change; New Power Supply (01630-66529/34)

1630A	from 2715A to 2812A
1630D	from 2720A to 2812A
1630G	from 2602A to 2812A
1631A	from 2714A to 2811A
1631D	from 2713A to 2811A

A serial prefix change incorporated an updated power supply. Several changes were made to increase reliability. Changes were extensive enough to require a separate parts list and schematic.

SECTION VIII
SERVICE

8-1. INTRODUCTION

The service section provides theory, block diagrams, and schematics for troubleshooting the logic analyzer.

This section consists of six sections or service groups:

8A - Power Supply and Motherboard
8B - CPU, Keyboard, and Display
8C - State Master Acquisition
8D - Timing Master Acquisition
8E - Timing Slave Acquisition
8F - Analog Acquisition

Each service group contains its own table of contents, theory, block diagrams, and schematics pertaining to that subsystem.

8-2. SAFETY CONSIDERATIONS

Read the Safety Summary at the front of this manual before servicing this instrument. Before performing each procedure, review it for cautions and warnings. For example, when working around the power supply and display circuitry, caution should be taken to avoid potentially lethal voltages.

CAUTION

An external cooling fan is required to cool PC boards inserted into the service connecter. An adequate fan should be available to any service organization.

8-3. BLOCK DIAGRAM THEORY (see figure 8-1)

POWER SUPPLY BOARD. The power supply board supplies +15, +12, -12, +5, -2.4, and -5.2 V to the different boards in the analyzer. The power supply uses the "switching technique" for converting AC to the six DC voltages.

CPU BOARD. The CPU board is the interface between the operator and the system. The CPU board provides measurement programming of the state and timing boards, keyboard control, display generation, HP-IB and HP-IL interfacing, and waveform formatting.

STATE MASTER BOARD. The State Master board receives 27 bits of data and three clocks from Pods 2, 3, and 4. State may also receive either 8 or 16 more bits of data if one or both of the two timing boards are in the State mode.

TIMING MASTER BOARD. The timing master board receives 8 bits of data from a timing pod for timing and glitch analysis. Timing master may be run in the State mode.

STATE SLAVE BOARD. The State Slave board is provided only in the 1630G. The State Slave board takes the place of the Timing Slave in the block diagram. Full coverage of this board is covered in Section 8F. It receives thirty channels of data from the target system and stores it under control of the State Master. Relative and absolute counting of stored states and time is provided by this board. The State Slave board also provides non-volatile storage of one instrument set-up and microprocessor disassembler.

TIMING SLAVE BOARD (1630D and 1631D only). The timing slave receives 8 bits of data from its own pod, allowing Timing Analysis to be as much as 16 bits wide. Slave timing may also be run in the State mode. For 35-bit wide state analysis, only the Timing Slave board can be run in the State mode. In the 35- bit mode the Timing Master must be used for timing, since it contains the timing qualification circuitry.

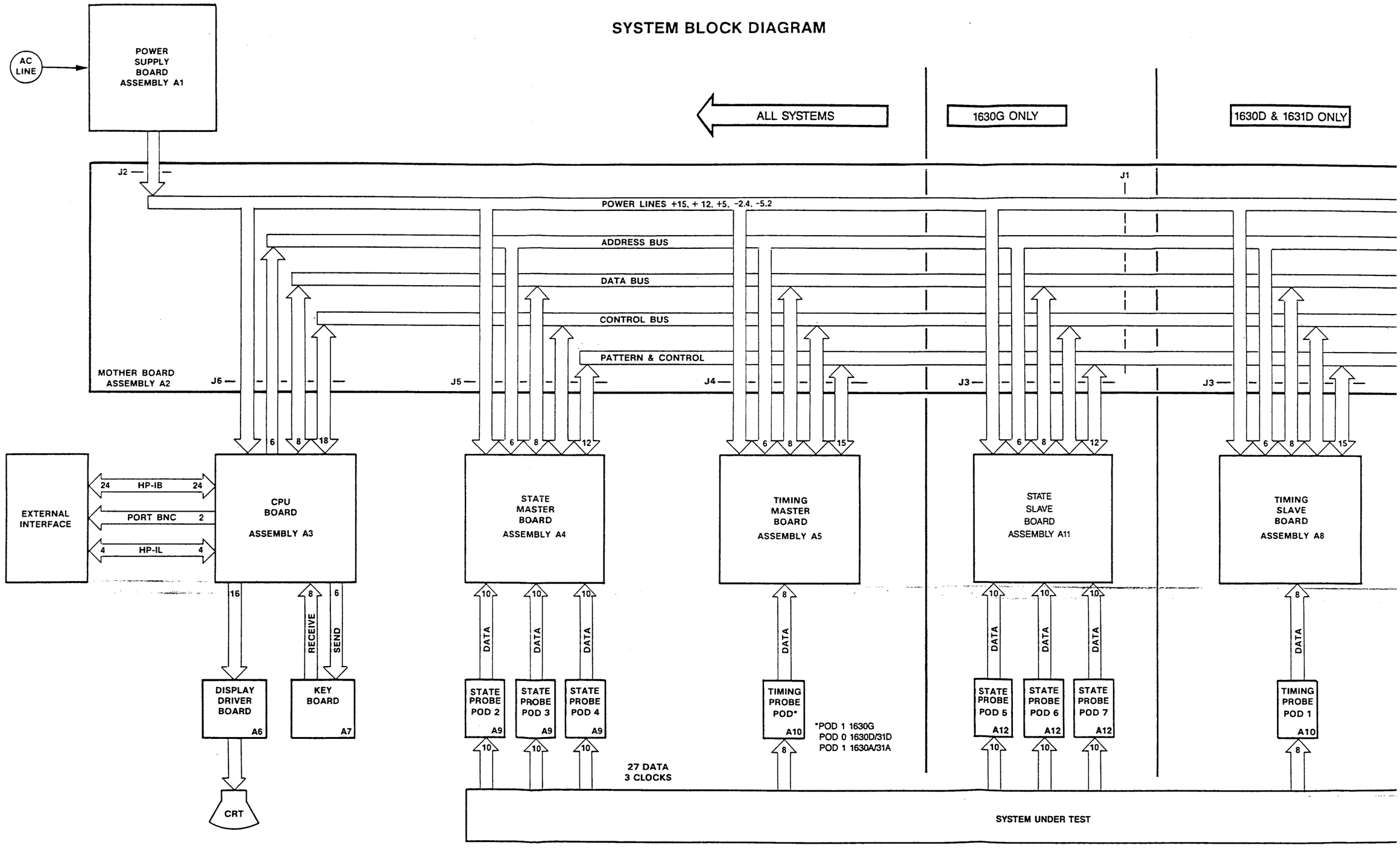
ANALOG BOARD (1631A/D only). The Analog Board digitizes two channels of analog waveform. It has an external trigger input or it can be triggered by the signal from either channel. It can be run as a slave to the other acquisition systems or it can be master to them. The full scale input range is from 40mV to 2.5V.

EXTERNAL INTERFACE. The CPU board may communicate with compatible external devices via HP-IB and HP-IL. HB-IB is a parallel bi-directional form of communication, whereas, HP-IL is a bit-serial unidirectional loop. Devices connected to HP-IB and HP-IL may be either talkers, listeners, or controllers. The 8 switch dip SW1 configures the logic analyzer on one of these buses.

The rear panel Port BNC can supply six acquisition signals on a multiplexed basis. An additional BNC supplies a +5 volt output for accessories such as a pre-processor option.

DISPLAY BOARD AND CRT. The display driver is an OEM assembly, not serviced by HP. The display assembly receives video and timing information from the CPU board.

SYSTEM BLOCK DIAGRAM



SYSTEM BLOCK DIAGRAM

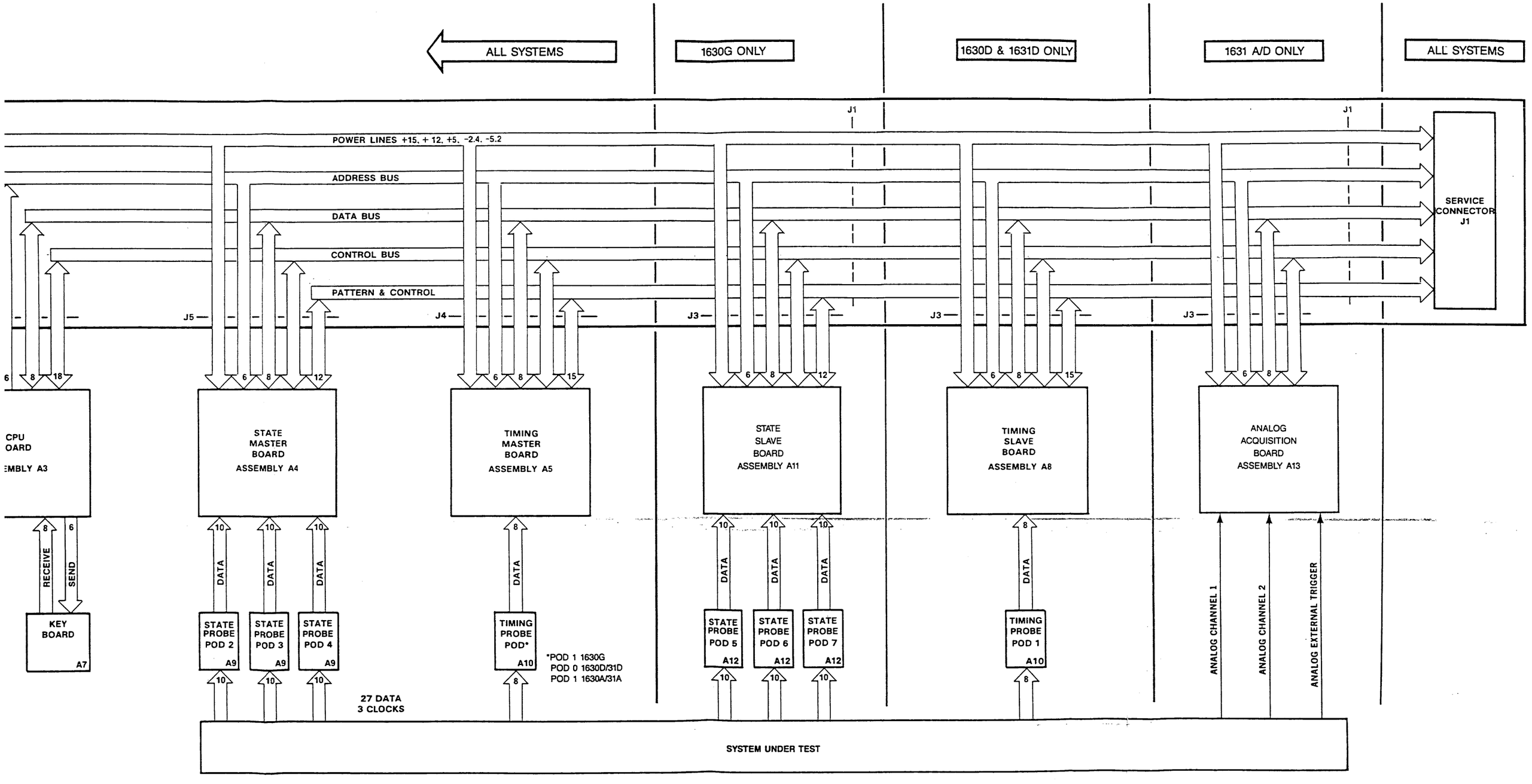


Figure 8-1. System Block Diagram

8-4. LOGIC CONVENTION

Logic states are defined as follows:

0 - False, negated, inactive, or unasserted state.

1 - True, active, or asserted state.

Voltage levels representing logic states:

LOW (L) The more negative of two voltage levels.

HIGH (H) The more positive of two voltage levels.

Signals may be either HIGH true, or LOW true, as indicated by the mnemonics on the schematics.

The logic analyzer includes both TTL and ECL ICs. Worst case voltage levels for troubleshooting and signature analysis purpose are as follows (IC data sheet specifications may be more accurate):

TTL Voltage Levels

Level	Voltage
LOW	less than 0.8 V
HIGH	greater than 2.0 V

ECL Voltage Levels

Level	Voltage
LOW	less than -1.50 V
HIGH	greater than -1.10 V

8-5. ECL ATTRIBUTES

Because ECL inputs are pulled down inside the IC, an unconnected ECL input is LOW.

ECL outputs may be tied together in the same way as open-collector TTL outputs. Thus, they may be wire-ANDed or wire-ORed.

Table 8-1. Logic Symbols, (sheet 1 of 3)

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

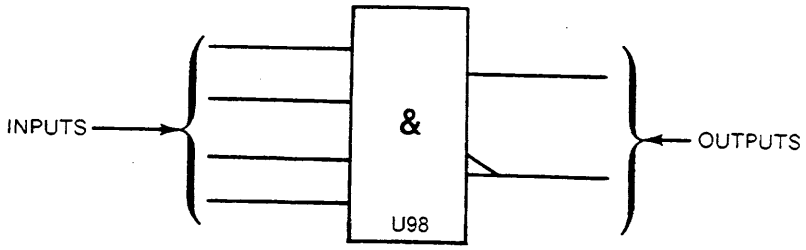
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

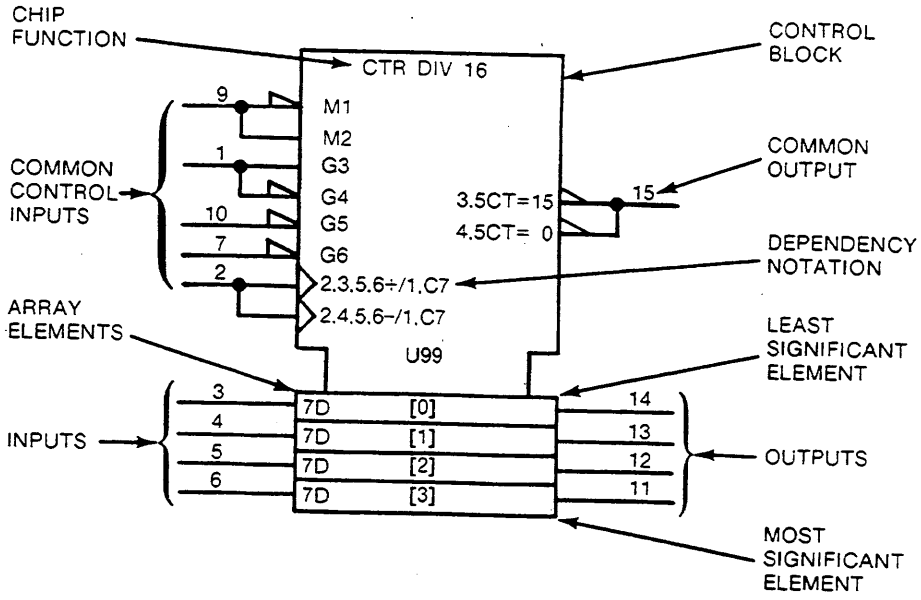
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in [ ]).

LS-08-09-82 - 1

Table 8-1. Logic Symbols, (sheet 2 of 3)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (complements state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

LS-08-09-82 - 2

Table 8-1. Logic Symbols, (sheet 3 of 3)

OTHER SYMBOLS

- Analog Signal
- & AND
- Bit Grouping
- Buffer
- ! Compare
- Dynamic
- =1 Exclusive OR
- Hysteresis
- ? Interrogation
- Internal Connection
- Inversion
- O Negation
- Nonlogic Input/Output
- Open Circuit (external resistor)
- Open Circuit (external resistor)
- ≥1 OR
- Passive Pull Down (internal resistor)
- Passive Pull Up (internal resistor)
- Postponed
- Shift Left (or up)
- Shift Right (or down)
- / Solidus (allows an input or output to have more than one function)
- Tri-State
- , Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
- ( ) Used for factoring terms using algebraic techniques.
- [ ] Information not defined.
- Φ Logic symbol not defined due to complexity.

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

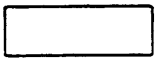
DELAY and MULTIVIBRATORS

- Astable
- 100 ns Delay
- Nonretriggerable Monostable
- NV Nonvolatile
- Retriggerable Monostable

LS-08-09-82 - 3

Table 8-2. Schematic Diagram Notes

ETCHED CIRCUIT BOARD



FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO.

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

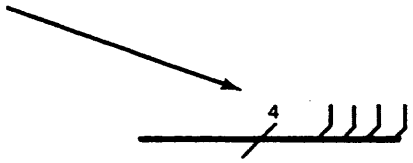
NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

SOURCE (DESTINATION) OF A SIGNAL FROM (TO) ANOTHER ASSEMBLY. LETTER GIVES SERVICE GROUP AND NUMBER REFERENCES SCHEMATIC WITHIN THAT GROUP.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

8-6. REMOVAL AND INSTALLATION OF MAINFRAME COMPONENTS

This section contains removal instructions for the system PC boards and the CRT. Read the Safety Summary at the front of this manual before servicing this instrument. Ali removal procedures are based on the 163XD systems. The removal procedures also apply to the 163XA systems except that they contain one less board.

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and display driver boards to discharge before servicing this instrument. Wear safety glasses!!!

CAUTION

Never install or remove any circuit board with the power switched ON. Component damage may occur!!!

NOTE

When a board is installed verify that it is fully seated into the connector.

8-7. Acquisition Board Removal (State and Timing)

a. Switch power OFF and disconnect the AC power cord.

b. Completely remove the two screws that secure the rear door. See figure 8-2.

c. Carefully remove the probe cable plugs by their plastic housing. See figure 8-3.

d. Remove the four screws that secure the rear cover and remove cover. See figure 8-3.

e. Carefully remove the desired acquisition board by inserting the "board puller" into the removal holes located at the rear of the board. See figure 8-4.

An acquisition board can be installed by reversing the removal procedure.

8-8. CPU Board Removal

a. Follow steps (a) through (d) of the Acquisition board removal procedure.

b. Completely remove the two screws securing the CPU board to the rear panel. See figure 8-5.

c. Remove the two plastic standoffs and loosen the screw that secures the bottom cover. See figure 8-5.

d. Carefully tilt the instrument on its side and remove the bottom cover.

e. Disconnect the cables from the CPU board that go to the keyboard and the display driver board. See figure 8-6.

f. Carefully remove the CPU board by inserting the "board puller" into the appropriate removal holes located at the rear of the board. See figure 8-4.

The CPU board can be installed by reversing the CPU board removal procedure.

8-9. Power Supply Board Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

CAUTION

Be certain that the perforated side cover is installed on the right-hand side of the instrument (as you face the front of the unit). If the side covers are mis-installed, insufficient air flow will result and component damage may occur.

a. Follow steps (a) through (d) of the Acquisition board removal procedure.

b. Completely remove the two screws securing the CPU board to the rear panel. See figure 8-5.

c. Remove the four plastic standoffs and loosen the two screws that secure the top and bottom covers and remove the covers. See figure 8-7.

d. Loosen the screw that secures the perforated side panel and remove. See figure 8-7.

e. Remove the two screws that attach the handle and the side cover to the frame. Remove cover.

f. Carefully tilt instrument on its side and remove the four screws holding the rear panel to the bottom of the frame. See figure 8-8.

g. Disconnect the cables from the CPU board to the keyboard and display driver boards. See figure 8-6.

h. Lay the instrument back on its base. Carefully remove all of the boards from the frame by inserting the "board puller" into the appropriate removal holes located at the rear of each board. See figure 8-4.

i. CAREFULLY remove the power switch shaft with a 1/4 inch wrench. See figure 8-9.

j. Remove the two screws by the line plug and the two screws securing the rear panel to the card cage. See figure 8-10.

k. Remove the four screws that attach the plastic power supply cover and ground strap to the top of the frame. See figure 8-9.

l. Unplug the fan from the power supply and gently push out on each corner from the inside of the rear panel. The rear panel and the fan assembly should remove as one unit.

m. Remove the three screws securing the power supply board to the card cage bracket. See figure 8-11.

n. Pull the power supply board straight back from the motherboard connector and remove from the frame.

The power supply board can be installed by reversing the removal procedure. See figure 8-4 for the card cage slot for each board.

8-10. Motherboard Removal

a. Follow steps (a) through (n) of the power supply board removal procedure.

b. Remove the six screws that secure the motherboard to the keyboard cover. See figure 8-12.

The motherboard can be installed by reversing the removal procedure.

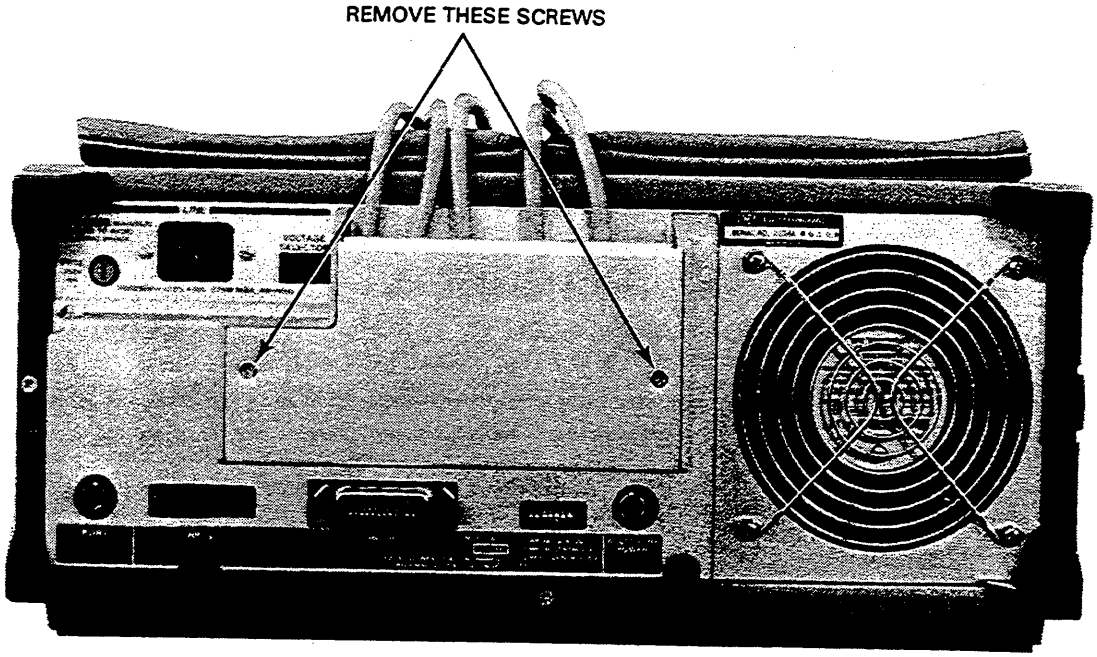


Figure 8-2.

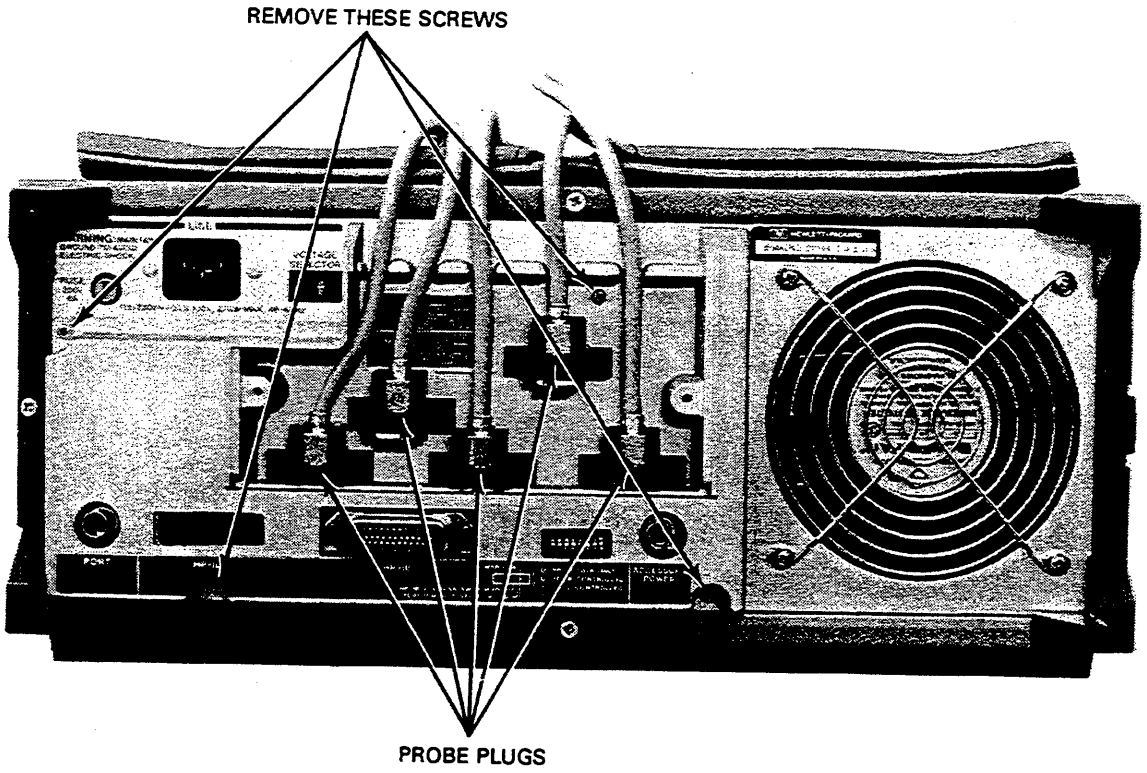


Figure 8-3.

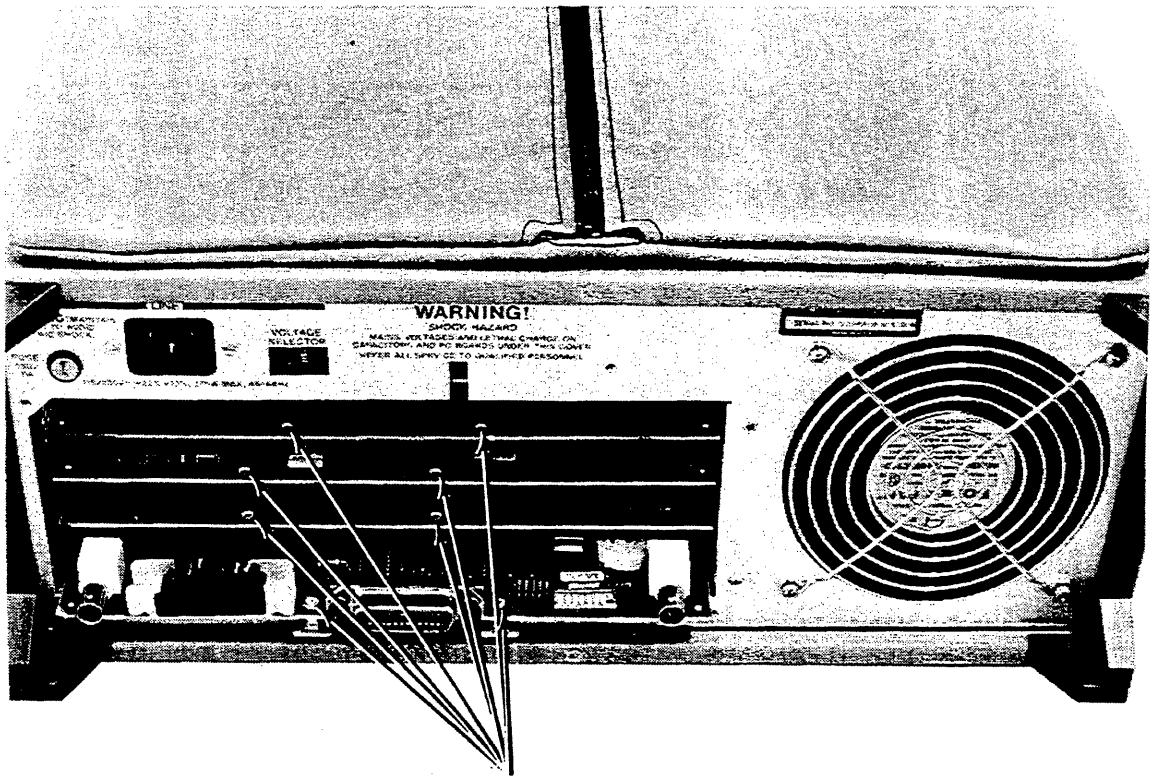


Figure 8-4.

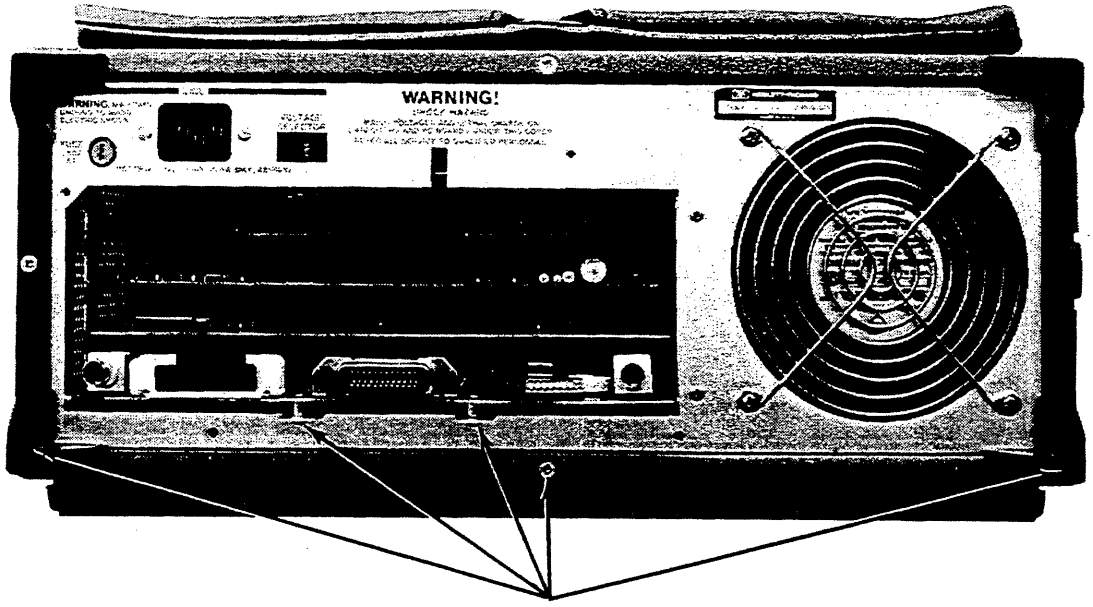


Figure 8-5.

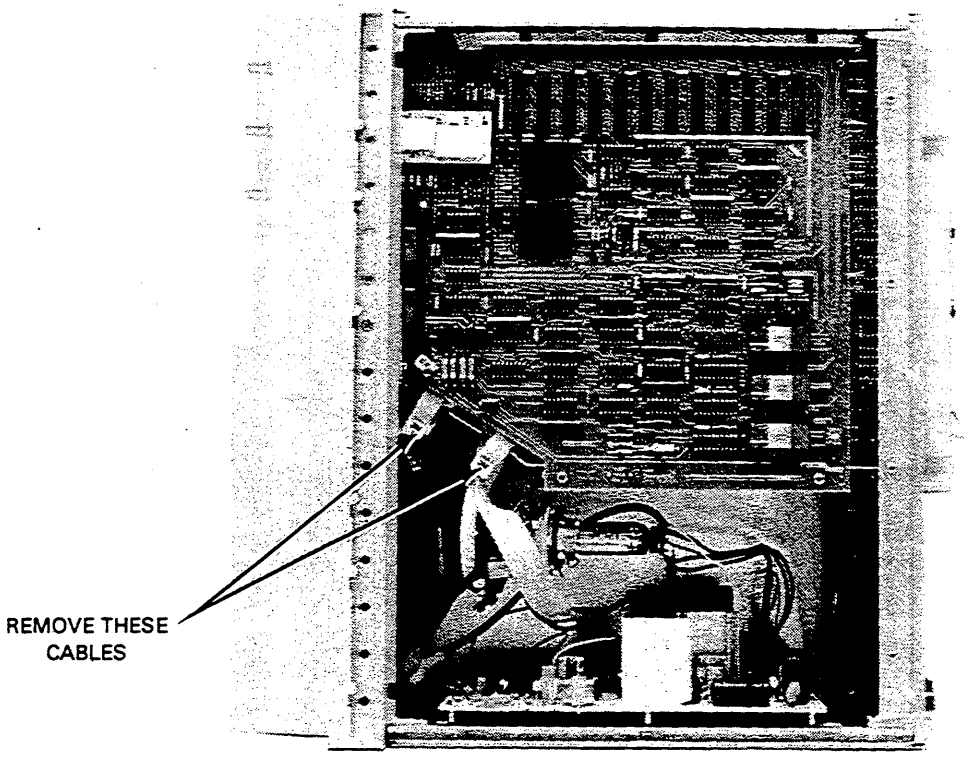


Figure 8-6.

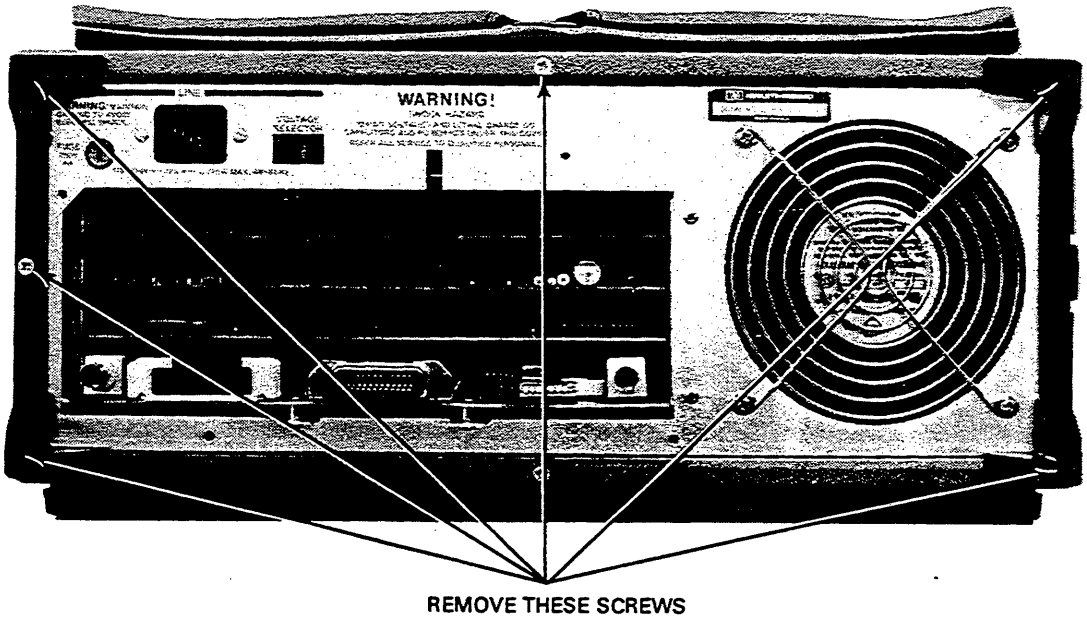


Figure 8-7.

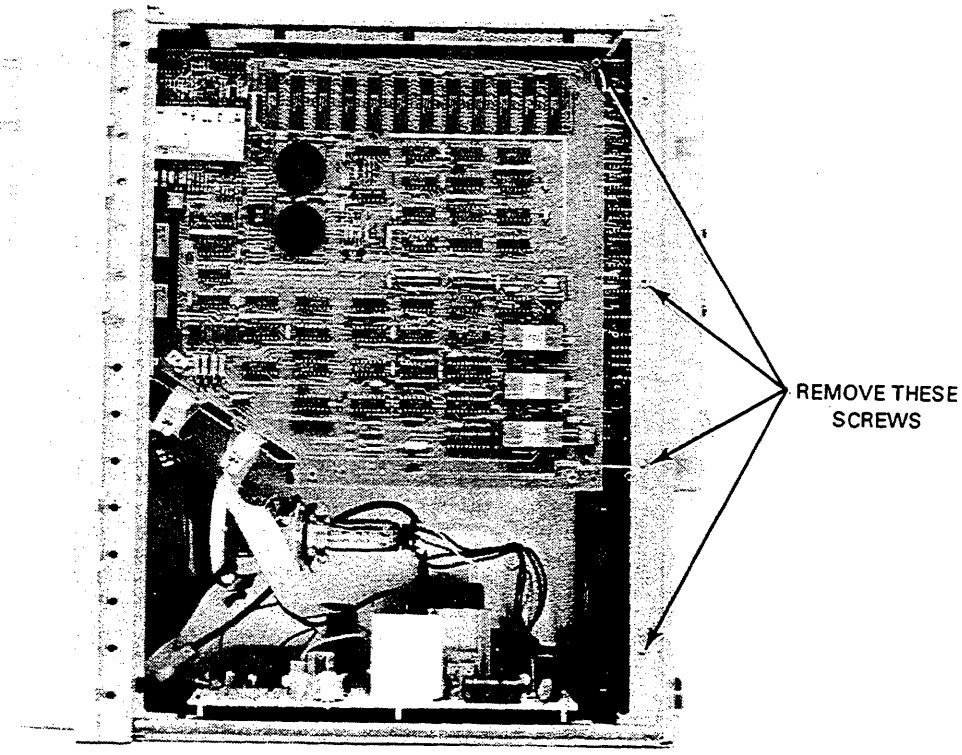


Figure 8-8.

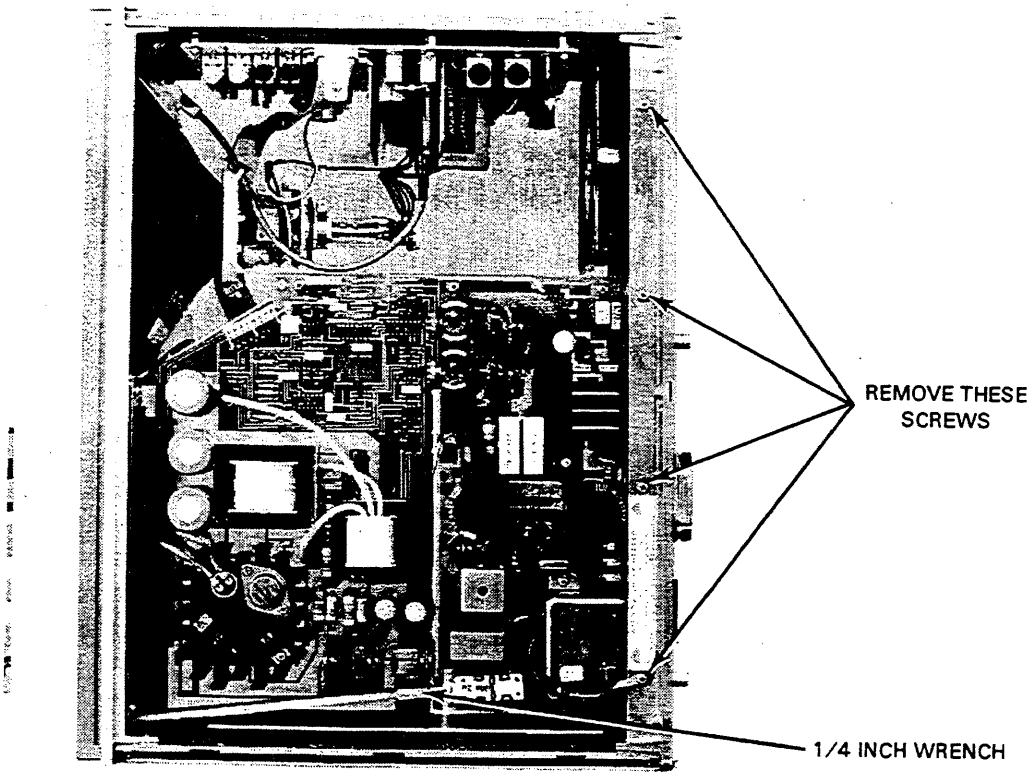


Figure 8-9.

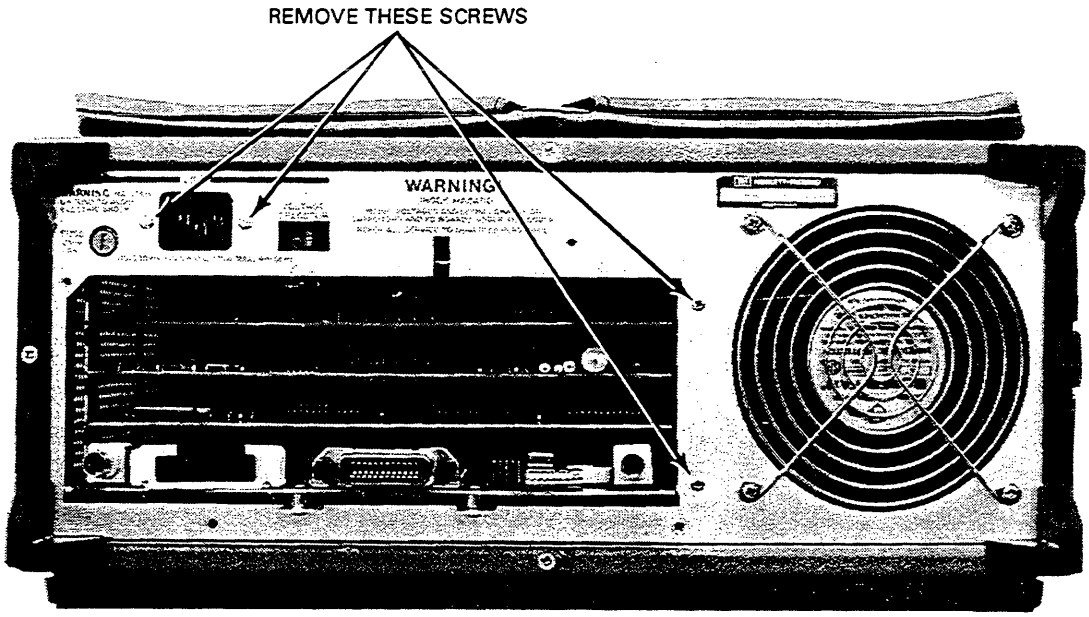


Figure 8-10.

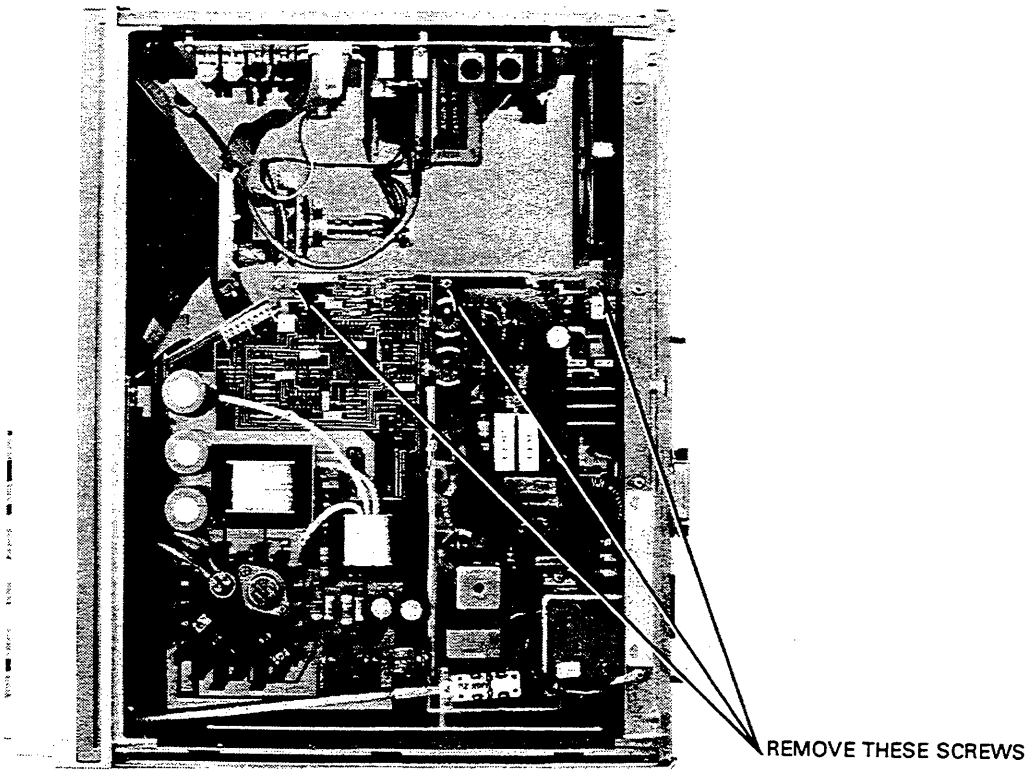


Figure 8-11.

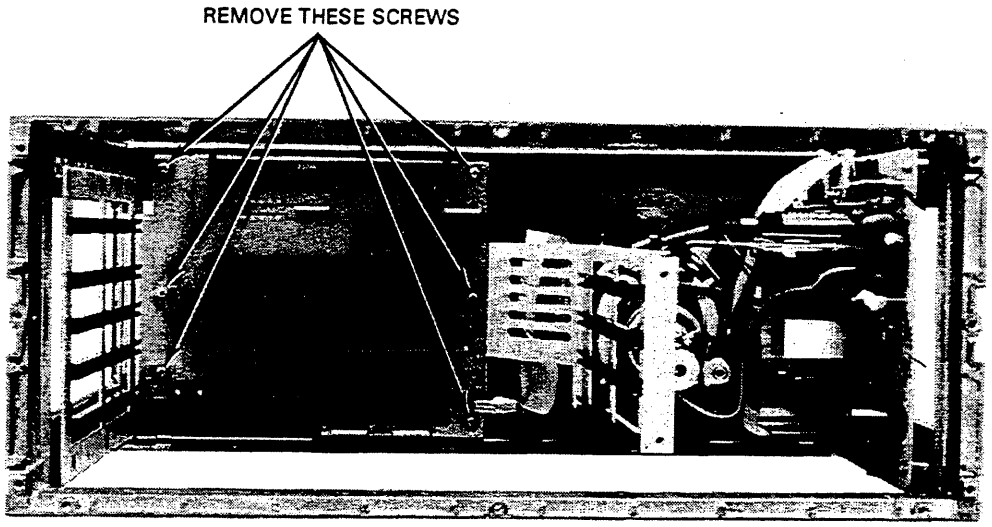


Figure 8-12.

8-11. Keyboard Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

a. Remove the four plastic standoffs and loosen the two screws that secure the top and bottom covers. See figure 8-7.

b. Tilt the instrument on its side and remove the screw indicated in figure 8-13 and the bottom cover.

c. Carefully lay unit in its proper bottom down position and remove the top cover.

d. Carefully pry up and remove the top plastic trim strip and remove the screw indicated in figure 8-14.

e. Slowly peel the two side vinyl adhesive trim strips being careful not to tear them.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

f. Short out the charge on the CRT by connecting a jumper lead between the ground lug of the CRT and the shaft of a screwdriver. Slip the screwdriver under the protective rubber cup of the post accelerator lead and then momentarily touch the screwdriver to the metal clip of the post accelerator lead. See figure 8-14.

g. Disconnect the post accelerator lead from the CRT by firmly squeezing on the rubber cup until the metal clip disengages from the CRT.

h. Disconnect the cable connecting the cathode of the CRT to the display driver. See figure 8-14.

i. Disconnect the two cables connecting the CRT yoke to the display driver. See figure 8-14.

j. Carefully pull and remove the black wire connecting the CRT ground lug to the display driver. See figure 8-14.

k. Remove the four side screws (two screws to a side) that secure the front bezel to the frame. These are located under the adhesive side trim strips. See figure 8-15.

l. Carefully pull the front bezel away from the frame being careful not to scratch the bezel or break the line switch shaft.

m. Remove the four screws and washers connecting the keyboard to the front bezel. See figure 8-16.

To install a keyboard reverse the removal procedure.

8-12. CRT Removal

a. Follow steps (a) through (l) of the keyboard removal procedure. All WARNINGS and CAUTIONS apply for the CRT removal procedure.

b. Remove the four screws and washers securing the CRT to the front bezel. See figure 8-16.

To install a CRT, reverse the removal procedure.

8-13. Display Driver Removal

a. Turn OFF instrument and remove AC power cord.

b. Remove the two plastic standoffs and loosen the screw that secures the top cover to the frame. Remove top cover. See figure 8-7.

c. Remove the two screws that connect the handle and the side panel to the frame. Remove side cover.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

NOTE

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

d. Short out the charge on the CRT by connecting a jumper lead between the ground lug of the CRT and the shaft of a screwdriver. Slip the screwdriver under the protective rubber cup of the post accelerator lead and then momentarily touch the screwdriver to the metal clip of the post accelerator lead. See figure 8-14.

e. Disconnect the post accelerator lead from the CRT by firmly squeezing on the rubber cup until the metal clip disengages from the CRT.

f. Disconnect the cable connecting the cathode of the CRT to the display driver. See figure 8-14.

g. Disconnect the two cables connecting the CRT yoke to the display driver. See figure 8-14.

h. Carefully pull and remove the black wire connecting the CRT ground lug to the display driver. See figure 8-14.

i. Remove the six screws that mount the display driver on the frame and remove board. See figure 8-17.

To install a display driver board reverse the removal procedure.

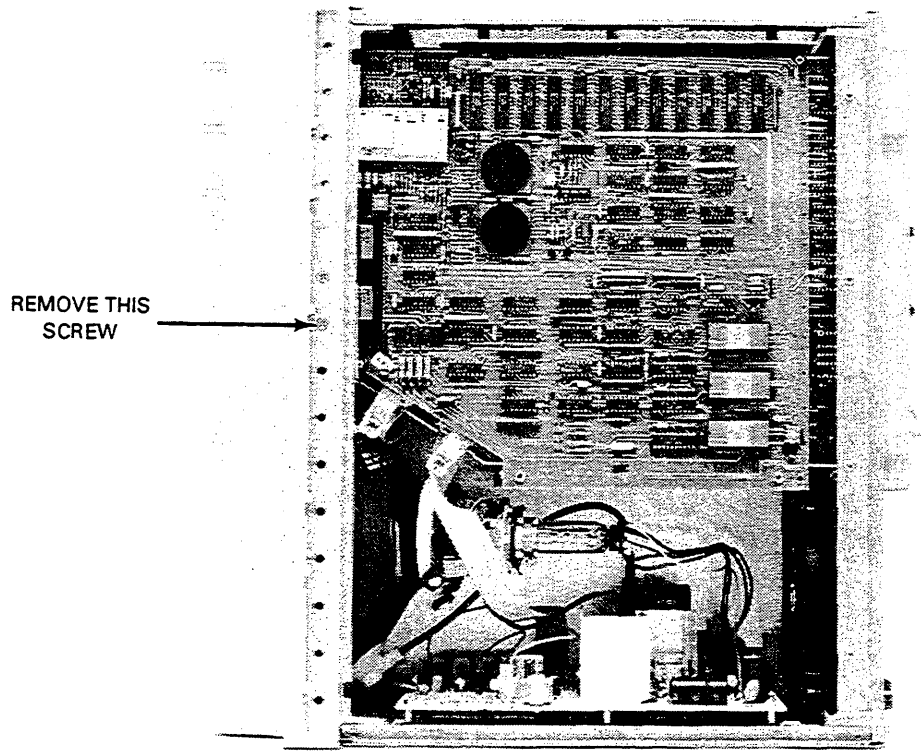
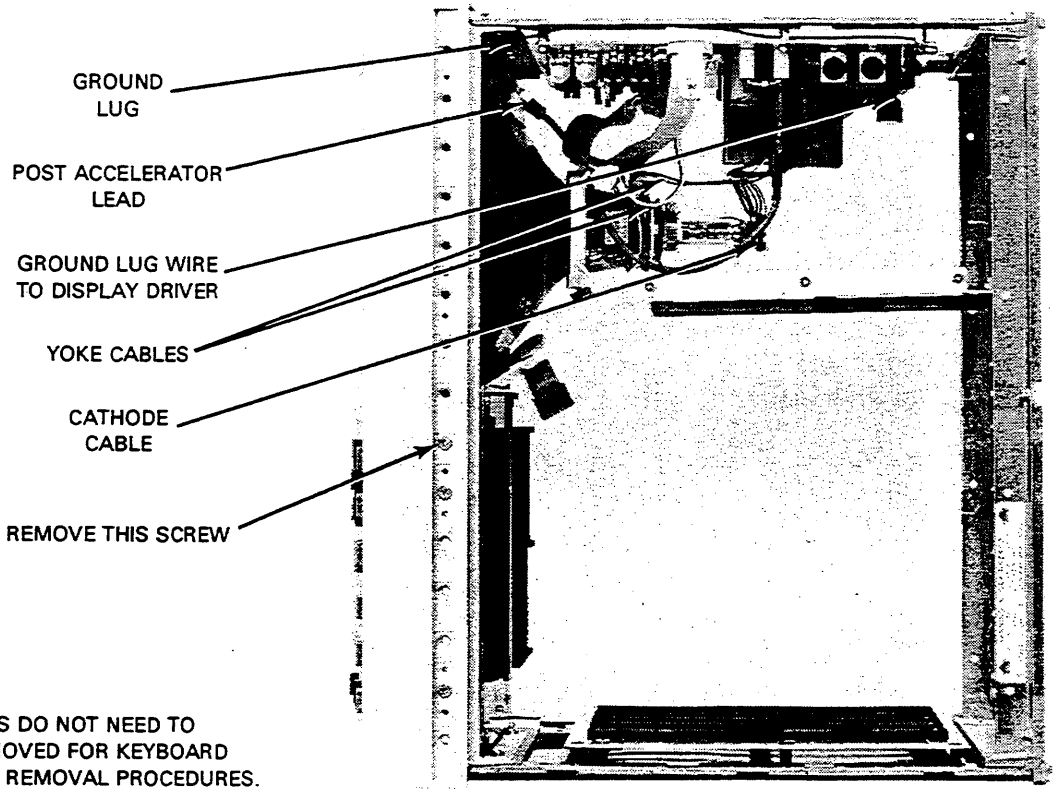


Figure 8-13.



NOTE
BOARDS DO NOT NEED TO
BE REMOVED FOR KEYBOARD
OR CRT REMOVAL PROCEDURES.

Figure 8-14.

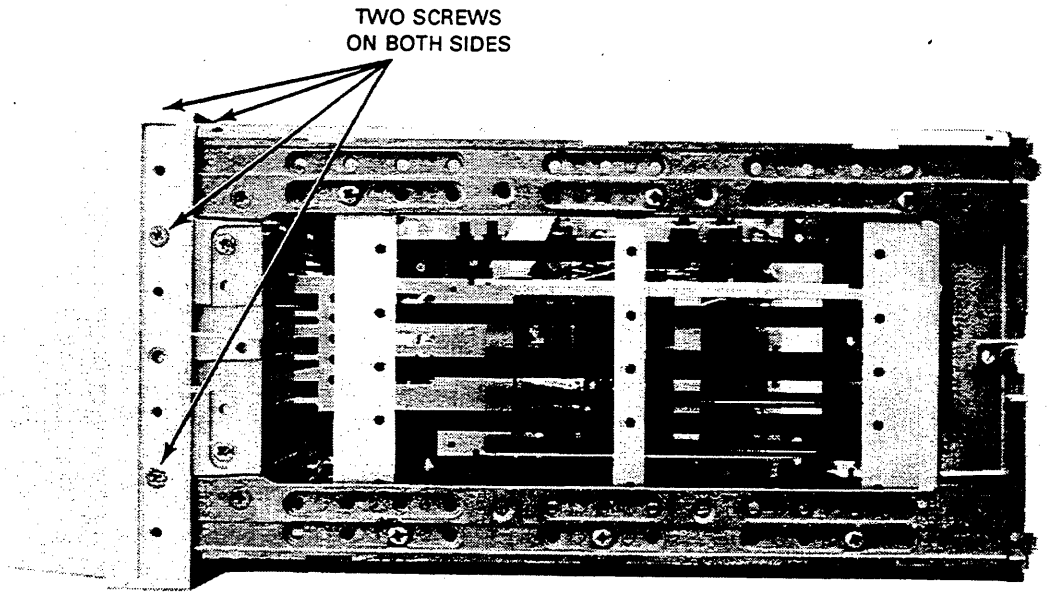


Figure 8-15.

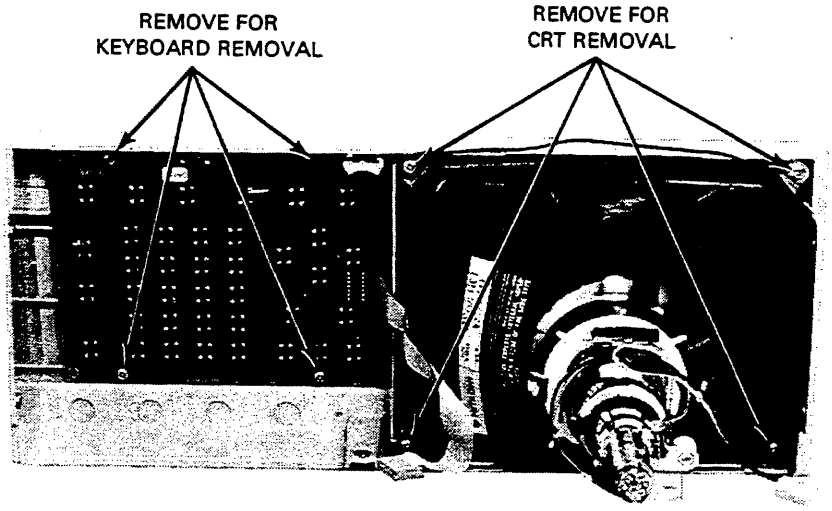


Figure 8-16.

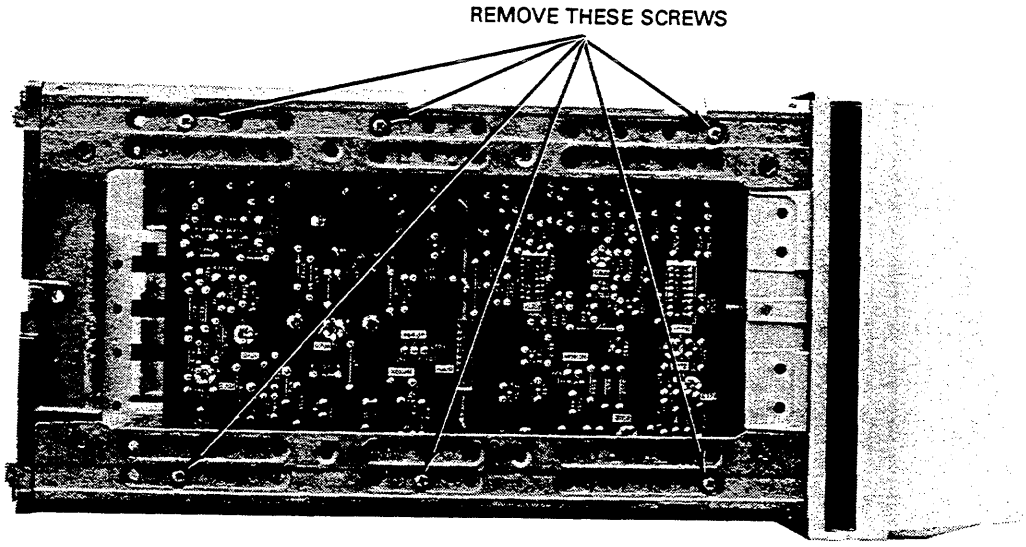


Figure 8-17.

8-14. Analog Board Removal

a. Turn OFF instrument and remove AC power cord.

b. Turn instrument onto it's top and remove the bottom rear feet.

c. Using the screw in the rear center of the bottom cover remove the cover.

d. Remove the nuts and washers from the three BNCs at the front of the instrument.

e. Remove the two screws along the inside edge of the analog board.

f. Carefully slide the board out of the instrument.

The Analog Board can be installed by reversing the above procedure.

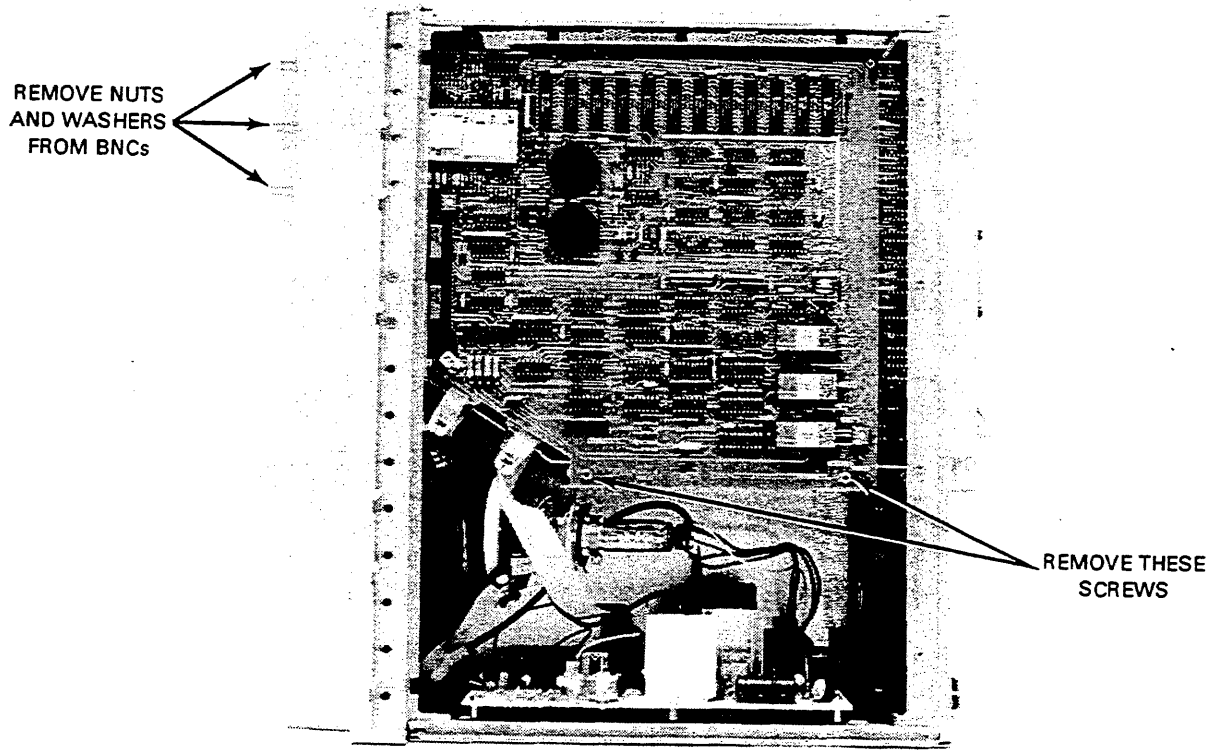


Figure 8-18.

Service Group 8A Table of contents

Paragraph		Page
8A-1.	Introduction	8A-1
8A-2.	Specifications	8A-1
8A-3.	Safety Considerations	8A-1
8A-4.	Power Supply Block Diagram	8A-2
8A-5.	Power Supply Theory Of Operation	8A-4
8A-6.	Primary Section	8A-4
8A-7.	115 VAC Operation	8A-4
8A-8.	230 VAC Operation	8A-4
8A-9.	Surge Current Protection	8A-4
8A-10.	Overvolt Protection	8A-4
8A-11.	RFI Suppression	8A-4
8A-12.	Control Section	8A-4
8A-13.	PWM Overview	8A-4
8A-14.	Modulation Control	8A-5
8A-15.	Power on Reset	8A-5
8A-16.	PWM Soft Start	8A-5
8A-17.	PWM Switching Frequency	8A-5
8A-18.	Current Switching Operation	8A-6
8A-19.	Control Power Supply	8A-6
8A-20.	PWM Failure Modes	8A-6
8A-21.	PWM Failure Execution	8A-6
8A-22.	PWM Current Limiting	8A-6
8A-23.	+5 Current Limit	8A-7
8A-24.	-2.4 Current Limit	8A-7
8A-25.	U3 and U4 Operation	8A-7
8A-26.	Primary Current Limit	8A-7
8A-27.	Thermal Shutdown	8A-7
8A-28.	+5 Overvoltage	8A-7
8A-29.	-5.2 Overvoltage	8A-7
8A-30.	Secondary Section	8A-8
8A-31.	+5, -5.2, And -2.4 Secondaries	8A-8
8A-32.	+15, +12, And -12 Secondaries	8A-8
8A-33.	LED Failure Indications	8A-8
8A-34.	Motherboard Information	8A-8
8A-35.	Mnemonics	8A-11

List of Illustrations

Figure		Page
8A-1.	Power Supply Block Diagram	8A-3
8A-2.	Functional Block Diagram of a PWM	8A-5
8A-3.	Foldback Current Limiting	8A-6
8A-4.	Troubleshooting Flowchart for LED Failure Indicators	8A-9
8A-5.	Power Supply Component Locator (01630-66529 and earlier)	8A-12
8A-6.	Power Supply Component Locator (01630-66534 and later)	8A-14
8A-7.	Mother Board Component Locator	8A-16

List of Tables

Table		Page
8A-1.	Power Supply Specifications	8A-1
8A-2.	Mnemonics	8A-11
8A-3.	Motherboard Connections and Signal Distribution	8A-17

List of Schematics

Schematic		Page
8A-1.	Power Supply (01630-66529 and earlier)	8A-13
8A-2.	Power Supply (01630-66534 and later)	8A-15

SERVICE GROUP 8A
POWER SUPPLY AND MOTHERBOARD

8A-1. INTRODUCTION

This Service Group contains block and component level theory, troubleshooting and schematic information necessary to service the logic analyzer power supply and motherboard. Service group 8A is separated into two sections: theory and troubleshooting.

8A-2. SPECIFICATIONS

The power supply used in the logic analyzer is a switching power supply that converts the AC line input to six regulated DC voltages. Table 8A-1 contains individual specifications for each voltage.

8A-3. SAFETY CONSIDERATIONS

WARNING

Several parts of the power supply have lethal voltage and current potentials associated with them. Primary filter capacitors C10 and C11 are very large and have 300 volts across them, + or - 150 Vdc to ground. This provides a great deal of potential energy. With their respective bleeders R4 and R5, the discharge time constant is 60 seconds so even with the supply turned OFF it can be dangerous! Therefore, wait at least three minutes for the supply to discharge before servicing.

Table 8A-1. Power Supply Specifications

INPUT

115 volt range: 90 to 127 VAC Input Imax = 4 Amps
230 volt range: 180 to 253 VAC Input Imax = 2 Amps
Frequency Range: 48 to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
+15	5	0.8
+12	5	0.25
+5	5	8.7
-2.4	10	8.0
-5.2	-5, +10	25.0
-12	5	0.25

8A-4. POWER SUPPLY BLOCK DIAGRAM

Use figure 8A-1 for reference. The power supply is separated into three basic sections; Primary, Control and Secondary. The following is a brief outline of each section.

PRIMARY SECTION. The primary section is responsible for providing a rectified and conditioned switching source of approximately plus and minus 150 VDC, along with transformation for control power. The primary section also provides protection to the supply from AC input surge current and overvoltage conditions. This section also drives the internal cooling fan.

CONTROL SECTION. Control voltage generation, modulation and switching are the main functions of the control section. However, LED failure indication and failure execution is also a function of this section.

SECONDARY SECTION. The secondary section is responsible for filtering, rectification and feedback for the DC power supplies. Also, this section outputs all of the supplies to the test connector and the motherboard.

POWER SUPPLY CHANGES. Because of continuing improvement in the power supply, the block diagram is not exact for all versions of the supply. For example, some fans are connected to the AC line input and boards with numbers 01630-66529 and earlier do not have the Power-on reset circuitry. The schematic diagrams with corrections show changes.

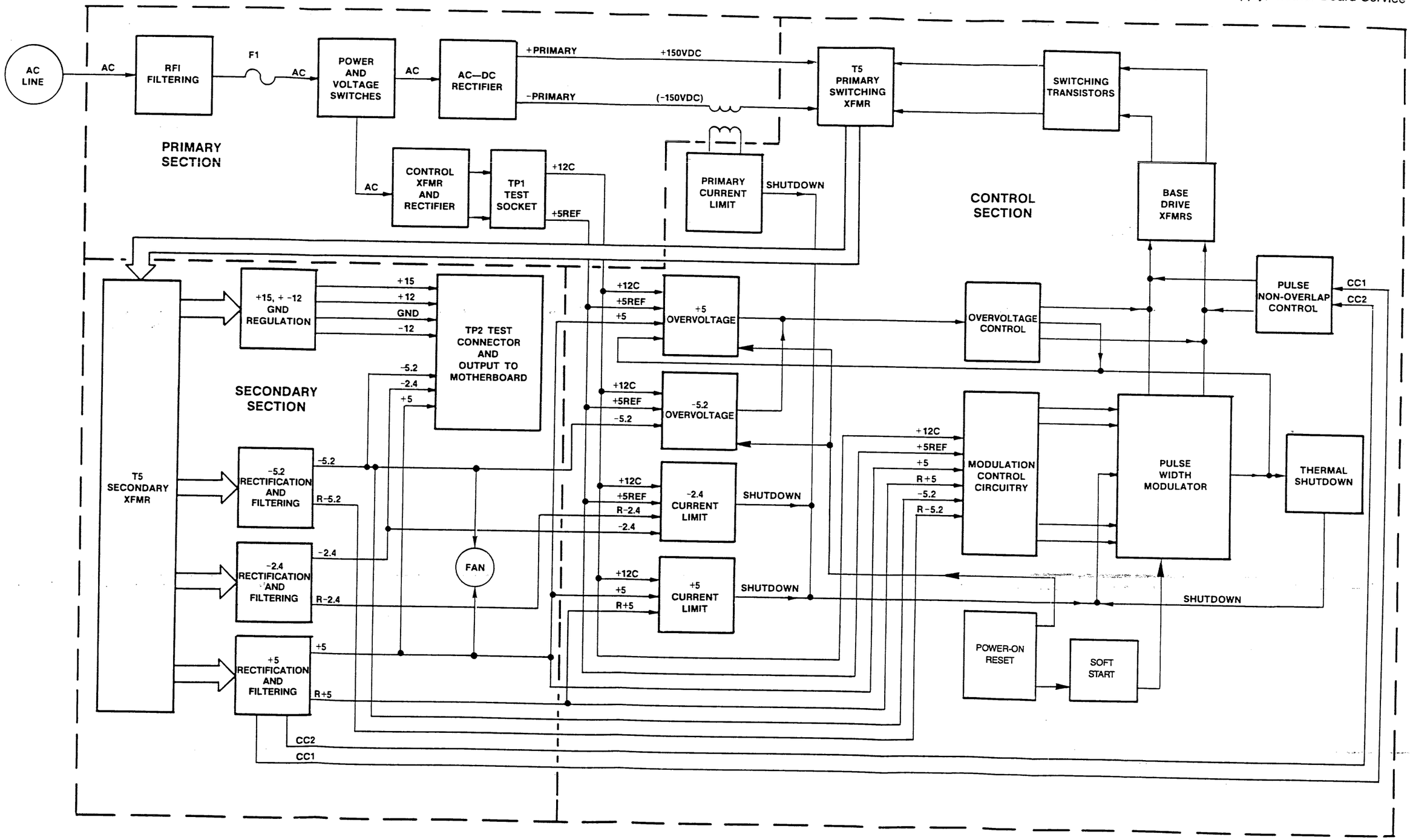


Figure 8A-1. Power Supply Block Diagram

8A-5. POWER SUPPLY THEORY OF OPERATION

The theory of operation gives detailed operation of power supply circuitry. For reference, refer to power supply schematics 8A-1 (boards 01630-66529 and earlier) and 8A-2 (boards 01630-66534 and later).

8A-6. Primary Section

The power supply begins operation when the power switch (SW2) is turned ON providing AC line to FL1 which filters the AC for radio frequency interference (RFI). According to the setting of the line select switch (SW1), the primary section operates in two modes, either 115 VAC or 230 VAC.

There are two versions of AC fan connection in the primary circuit. Later supplies have a dc fan at the output of the supply. Two-wire AC fans (115 V) connect across the upper primary of T1. Four wire AC fans (115/230 V) connect across both primarys of T1.

The varistors RV1 (115 V) and RV2 (230 V) on the primary side of T1 are for transient suppression. The 66534 board has only the 230 V varistor, which is designated RV1. Thermistor RT3 (RT1 on schematic 8A-2), provides surge current protection for CR4.

8A-7. 115 VAC OPERATION. The junction of C10 and C11 (at the output of the bridge rectifier (CR4), with T1 pin 2, is wired through SW1 to the Neutral side of the line input. Only two of the diodes of the bridge are used, the two top ones of CR4, connected to the Line side of the AC input. This configuration produces ≈300V across the + and - outputs of CR4. In the 115 VAC mode this circuitry forms a half wave voltage doubler. While in the 115 VAC mode the primaries of T1 are in parallel so there is 115 VAC across each primary. The outputs of T1 are in parallel and have the same voltage across them during either the 115 or 230 VAC modes.

8A-8. 230 VAC OPERATION. When SW1 is in the 230 VAC mode, all four diodes in the bridge rectifier (CR4) are used. However, the voltage across the + and - outputs of CR4 is still ≈300V. During the 230 VAC mode this circuitry forms a full wave rectifier. While in the 230 VAC mode the primary inputs of T1 are in series and still have 115 VAC across each primary winding. The connection of the junction of C10 and C11 to the junction of the T1 primaries splits the dc voltage load on C10 and C11.

8A-9. SURGE CURRENT PROTECTION. Because input filter capacitors C10 and C11 are connected directly across the rectified line, a form of surge current protection is provided to limit line surges during turn on. RT3 (RT1 on schematic 8A-2) provides this protection.

8A-10. OVERVOLT PROTECTION (Schematic 8A-2). During an AC overvolt situation V1, V2, and RT2 provide protection to the supply. When the tubes (V1 and V2) reach their maximum voltage limit (~240 V), they drop to a low impedance and shunt the overvoltage through RT2. A similar circuit, on the other side of CR4, was used on some boards prior to 01630-66529 but was later removed to improve reliability. A service note covered removal of the surge supressors (designated E1 and E2 on those boards).

8A-11. RFI SUPPRESSION. Inductors L2 (balun) and L1 prevent RFI generated by the switching supply from being conducted back into the AC line.

8A-12. Control Section

The control section mainly consists of the circuitry needed to control the operation of the pulse width modulator (PWM). Also covered is the error detection and execution circuitry needed to control modulation.

8A-13. PWM OVERVIEW (see Figure 8A-2). A pulse width modulator (PWM) requires four signals for proper modulation: a reference voltage, a feedback from the output to compare with the reference voltage for error detection, feedback current from the output for output current limiting, and a predetermined switching frequency.

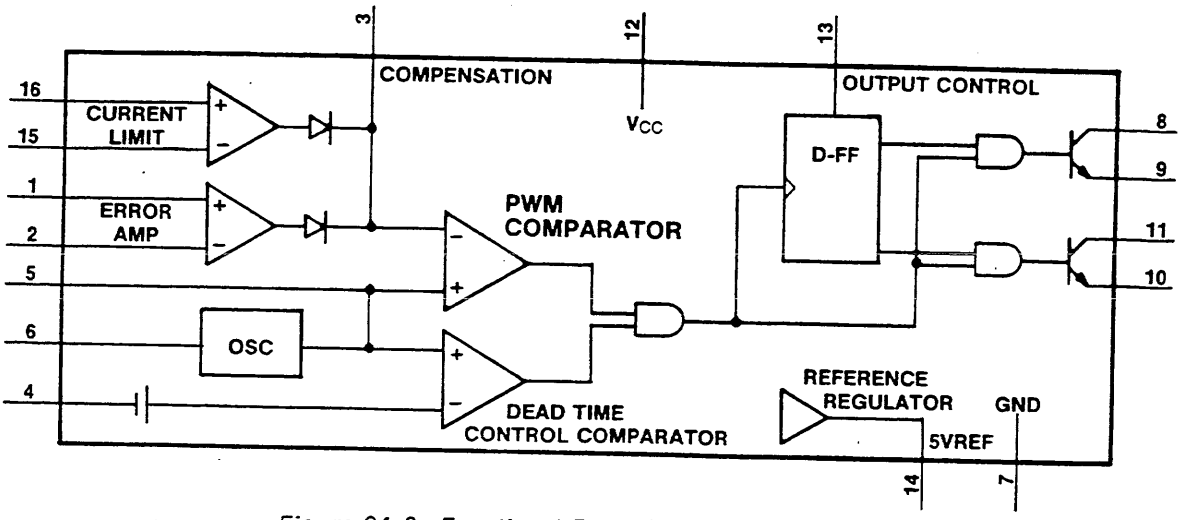


Figure 8A-2. Functional Block Diagram of a PWM

A PWM modulates it's output transistors pulse width (ON time) according to the demands of the system. In this manner it controls the amount of current each switching transistor delivers and therefore controls the power. The PWM configuration used by this supply is for push-pull modulation. Push-pull modulation means that each internal open collector output transistor is turned ON alternately by the pulse-steering flip-flop. This configuration is determined by the output control input (OC) pin 13 being tied to the PWM's internal 5V reference regulator, pin 14.

8A-14. MODULATION CONTROL. If the +5V feedback voltage at pin 1, U5, is higher than the reference voltage at pin 2, the PWM determines that the output voltage is too high. It then reduces its output transistors pulse widths to within limits.

8A-15. POWER ON RESET. This circuit is on 01630-66534 and later boards (schematic 8A-2). This circuit provides an orderly start-up when power is turned on. U7 has two inputs, PWM+5VREF and +12VC. The reference, PWM+5VREF reachs its level first so the outputs of U7A and U7B are low. This keeps the overvoltage circuitry disabled through U7A pin 1 and prevents operation of the soft-start circuit through U7B pin 7. At some time during powerup, +12VC goes high enough and U7 outputs switch, enabling the overvoltage and soft-start circuits.

8A-16. PWM SOFT START. Soft start is used to prevent large current surges which may occur on power up. Also, a soft start prevents a false signal, possibly created by the control circuitry, from resetting the PWM during power up.

For boards 66534 and later (refer to schematic 8A-2), during early powerup Q3 is turned on by the low output of U7B so the dead-time input of U5 (pin 4) is high, 100% dead-time. When pin 7 of U7B goes low Q3 turns off and C21 starts to discharge through the 4700 ohm resistance in Q3's collector. As the voltage at U5 pin 4 drops the PWM slowly starts up, dead-time decreases, and full power is gradually allowed.

For boards 66529 and earlier (refer to schematic 8A-1), when AC is switched ON, capacitor C21 has not charged. This forces the dead-time control input, pin 4 of U5, to the 5V reference regulator output, pin 14. As C21 charges through RP2 (pins 5 and 6), the voltage across this part of RP2 slowly drops and the output pulse widths are allowed to modulate slowly until dead-time is low and 100% modulatio is allowed.

8A-17. PWM SWITCHING FREQUENCY. The 42 KHz internal oscillation frequency of the PWM is determined by the RC time constant of R21 and C22 connected to pins 6 and 5 of U5. Therefore, each open collector output transistor (pins 8 and 11) is turning ON and OFF alternately at about 21 KHz.

8A-18. CURRENT SWITCHING OPERATION (see schematic). The open collector outputs, pins 11 and 8 of U5, are complementary and non-overlapping. For zero on-time (zero modulation time), both outputs are high. As demand increases, each output stays low (at different times, non-overlapping) for a longer period until one is going high as the other is going low or until one of the feedback signals limits the pulse duration. The outputs are inverted through U2F,G, another open collector device, and alternately cause changing current through the primaries of T2 and T3. These transformers alternately turn Q1 and Q2 ON and OFF which causes the current in the primary of T5 to alternate.

The signals CC1 and CC2 (from U2B,C) prevent or delay the switching of Q1 and Q2. For example, suppose the following condition exists. The power supply is experiencing a heavy demand and must allow close to 100% modulation to meet it. Q1 has turned ON per the request of the PWM and has pulled the one node of T5 to the + primary voltage. Then the PWM tells Q1 to turn OFF and Q2 to turn ON. Q2 can turn ON immediately, but Q1 cannot turn OFF that quickly because of charge storage. The CC2 signal is a feedback signal from the secondary of T5 senses this condition and and will not allow Q2 to turn ON until Q1 turns OFF and the voltage on the secondary of T5 stabilizes. To allow Q2 to turn ON sooner would have the effect of shorting the + primary voltage to the - primary voltage for a short period of time (an enormous waste of power not to mention damage to components).

8A-19. Control Power Supply

As soon as AC is switched ON, CR1 rectifies AC and starts charging C3, a ripple filter for the 12 volt regulator VR1. The output of VR1 lags the input by about 1 V on power up until it stabilizes at +12 V. VR1 is the regulator for +12C (the control power supply, used only on the power supply board). +12C also supplies U1 which is the +5 reference source (+5REF).

8A-20. PWM Failure Modes

8A-21. PWM FAILURE EXECUTION. There are seven failure execution circuits in the power supply. One of these failures, -5.2 current limit, affects the current limit input, U5 pins 15 and 16, of the PWM. Four of the failures affect the Compensation/PWM Comparator input (COMP) pin 3, U5. The COMP input must be allowed to float during normal operation. If an error occurs with the +5 or -2.4 current limit, primary current limit, or thermal shutdown pin 3 is pulled high and the PWMs' output transistors are shut OFF. Two of the failures, +5 and -5.2 overvoltage act directly on the drive lines to the Primary Base Drive Transformers.

Several of these failures have LED indicators which indicate the nature of the failure.

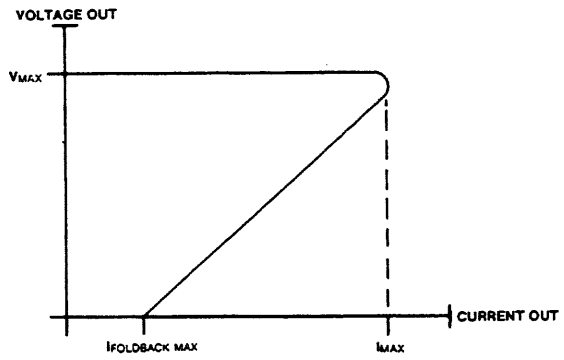


Figure 8A-3. Foldback Current Limiting

8A-22. PWM CURRENT LIMITING. This power supply uses fold-back current limiting (see figure 8A-3). The actual current limit value is determined by sensing the DC voltage developed across the internal resistance of T6 pins 2,11 and 3,10 (T6 contains six internal inductors). Current limiting of the -5.2V supply works by developing a voltage across C20 that is proportional to the maximum load current times the internal resistance of T6 pins 2,11 and 3,10. The voltage across C20 is then compared to the reference voltage at pin 15 of U5. The foldback of the maximum current limit value is determined by the decrease in the voltage across R17. When the voltage across R17 decreases, the voltage required across C20 also decreases. The decrease across C20 causes the PWMs internal

comparator to go more positive and reduce modulation until the -5.2 output voltage across R16 increases, allowing C20 to charge to the value of the reference voltage.

8A-23. +5 CURRENT LIMIT. This circuit operates similarly on the PWM except: the DC component is taken from T6 pins 1 and 12; the voltage on C43 sets the current limit value; R36 sets the foldback limit; and P/O RP3 pins 4 and 3 adjust the foldback limit. When current limit occurs, pin 14 of U6D goes high and biases CR17, which makes pin 3 of U5 more positive and reduces modulation.

8A-24. -2.4 CURRENT LIMIT. This circuit operates similarly to the +5 current limit except: the DC component is taken from T6 pins 4 and 9; C45 sets the current limit value; P/O RP3 pins 5 and 6 set the foldback limit; and R4 adjusts the foldback limit. When a current limit occurs, pin 8 of U6C goe high and biases CR16, which makes pin 3 of U5 more positive and reduces modulation.

8A-25. U3 AND U4 OPERATION. U3 and U4 are overvoltage sensors. U3 and U4 turn ON LEDs if an error condition is detected, and either can generate SHUTDOWN. U3 and U4 work in the following manner. When the voltage at pin 2 exceeds the voltage at pin 7 by 2.6 volts, the output pin 8 latches high to turn ON the failure LED and generate SHUTDOWN. The capacitor on pin 3 and pin 4 of U3 and U4 determine the minimum amount of time that an error must exist before they turn ON, thus providing transient protection.

8A-26. PRIMARY CURRENT LIMIT. U4 detects an error via T4. The primary side of T4 is in the return loop of the minus primary voltage for the switching transistors. The change of current through the primary of T4 establishes a voltage drop in the secondary, rectified by CR10, divided by R14 and R15, and detected at pin 2 of U4. If the voltage at pin 2 of U4 is greater than 2.6 volts, (a slight delay is provided by C19), U4 latches and turns ON the primary current limit LED "PL" and sets SHUTDOWN high which turns OFF U5.

8A-27. THERMAL SHUTDOWN. The circuitry for U3 detects an over temperature condition and generates SHUTDOWN. For boards 66529 and earlier a normally closed thermal switch (SW3) is mounted on heatsink MP9. When the heatsink exceeds 105 C, the thermal switch opens and U3 detects an error. When pin 8 latches high, the thermal shutdown LED "TH" is turned ON. Then SHUTDOWN is generated and U5 is turned OFF.

For boards 66534 and later the thermal switch is replaced by a positive temperature coeficient switch, a thermistor with a very non-linear resistance change with temperature. It has a resistance of about 100 ohms at 25 degrees C, which increases by a factor of nearly 100 with 5 degrees increase in temperature. Its effect on the thermal shutdown circuitry is the same as the thermal switch on older boards.

8A-28. +5 OVERVOLTAGE. An overvoltage failure occurs when the +5 volt supply exceeds 6 volts making the voltage at pin 3 of U6A greater then the 5V reference on pin 2. This in turn makes pin 1 of U6A go high forcing two operations to occur. The first operation biases CR13 which keeps pin 3 of U6A high regardless of the overvolt condition. The second operation biases CR11, thus making the outputs of U2A, U2D and U2E low. With U2E low, the "OV" (overvoltage) LED (P/O DS1) goes ON indicating an overvoltage failure. Furthermore, with U2A and U2D low, U2F and U2G are be unable to deliver a switching frequency to the base drive transformers. This turns OFF the supplies. Note, that with CR13 biased on, the circuit is latched and power must be cycled OFF/ON to reset the overvoltage circuitry.

8A-29. -5.2 OVERVOLTAGE. Except for polarity considerations, the -5.2 overvoltage circuitry operates the same as the +5 overvoltage circuit. This circuit activates at -6.2 volts.

8A-30. Secondary Section

8A-31. +5, -5.2, AND -2.4 SECONDARIES. Three of the four switching supply secondaries operate relatively the same. The +5 supply is used as an example of their operation.

The alternating voltage in the center tapped secondary of T5 is full wave rectified by two Schottky diodes (CR20) mounted on a heatsink (MP9). The R27/C28 combination is a snubber network that limits the dv/dt to protect the diodes. CC1 and CC2 (cross conduction 1 and 2) prevent both switching transistors from being ON at the same time and shorting the + and - primary voltages together. P/O T6 and C49 are the filter for the supply. The LED "NORM" being ON indicates that the supply is operating properly.

Except for polarity and the lack of an indicator, the -2.4 and -5.2 supplies are the same as the +5 supply.

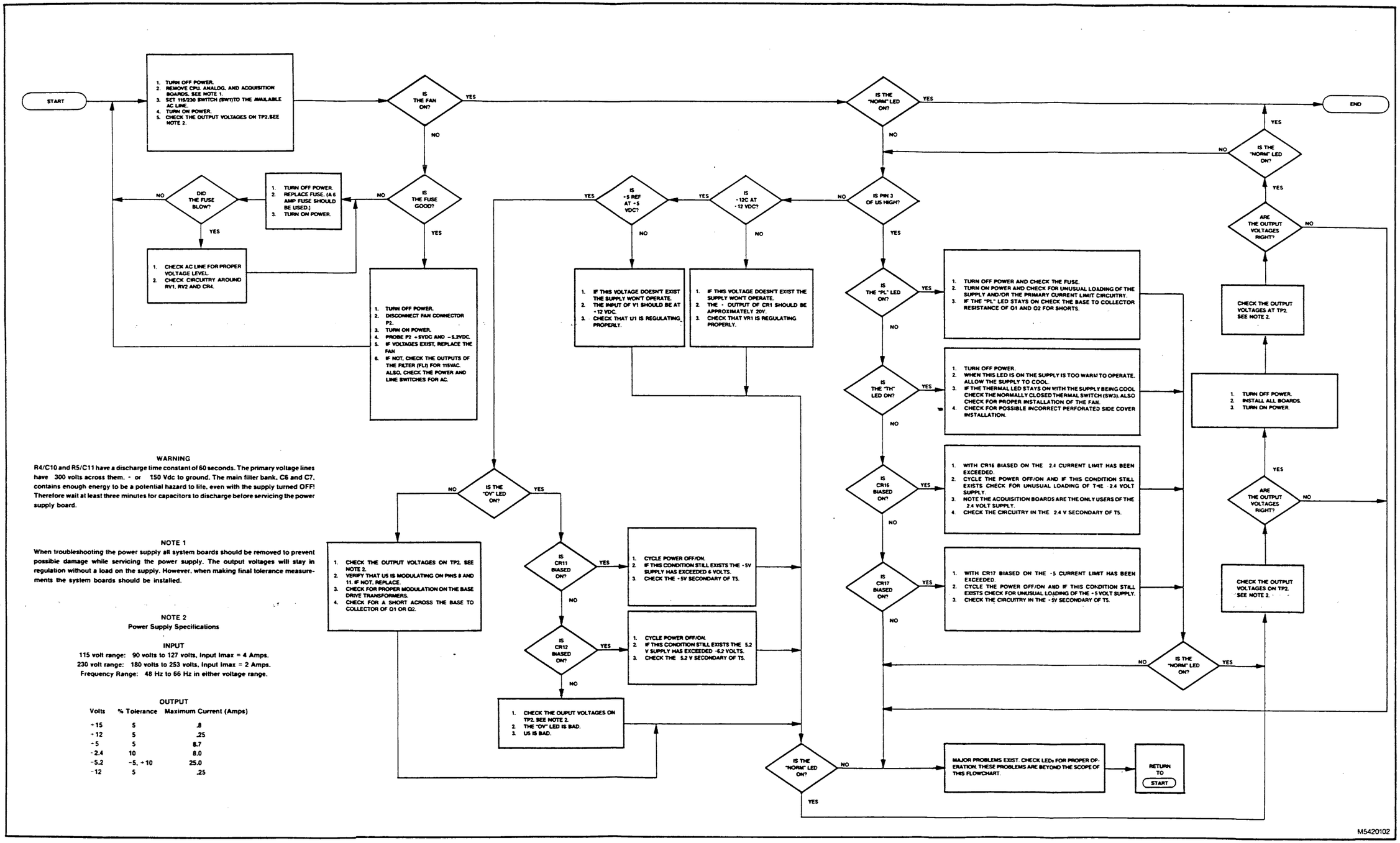
8A-32. +15, +12, AND -12 SECONDARIES. The alternating voltage of T5 is full wave rectified by CR15. R24 and C23 form a snubber network to protect CR15. P/O T6, C25 and C26 filter the outputs of CR15 before they are regulated by VR2, VR3 and VR4. The outputs of the regulators are filtered by C29-31 before the +15, +12 and -12 voltages are supplied to the motherboard.

8A-33. LED FAILURE INDICATIONS

Figure 8A-4 is a flow chart that guides the user to the faulty circuit(s) indicated by a power supply failure LED.

8A-34. MOTHERBOARD INFORMATION

The motherboard connects and distributes all of the signals from the power supply, CPU, and State and Timing boards. Figure 8A-7 is a component locator for the parts on the motherboard. Table 8A-3 gives the motherboard connections and instrument signal distribution for all instruments.



WARNING

R4/C10 and R5/C11 have a discharge time constant of 60 seconds. The primary voltage lines have 300 volts across them, - or 150 Vdc to ground. The main filter bank, C6 and C7, contains enough energy to be a potential hazard to life, even with the supply turned OFF! Therefore wait at least three minutes for capacitors to discharge before servicing the power supply board.

NOTE 1

When troubleshooting the power supply all system boards should be removed to prevent possible damage while servicing the power supply. The output voltages will stay in regulation without a load on the supply. However, when making final tolerance measurements the system boards should be installed.

NOTE 2

Power Supply Specifications

INPUT

115 volt range: 90 volts to 127 volts, Input Imax = 4 Amps.
230 volt range: 180 volts to 253 volts, Input Imax = 2 Amps.
Frequency Range: 48 Hz to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
+15	5	.8
+12	5	.25
+5	5	8.7
-2.4	10	8.0
-5.2	-5, +10	25.0
-12	5	.25

Figure 8A-4. Troubleshooting Flow Chart For LED Failure Indicators

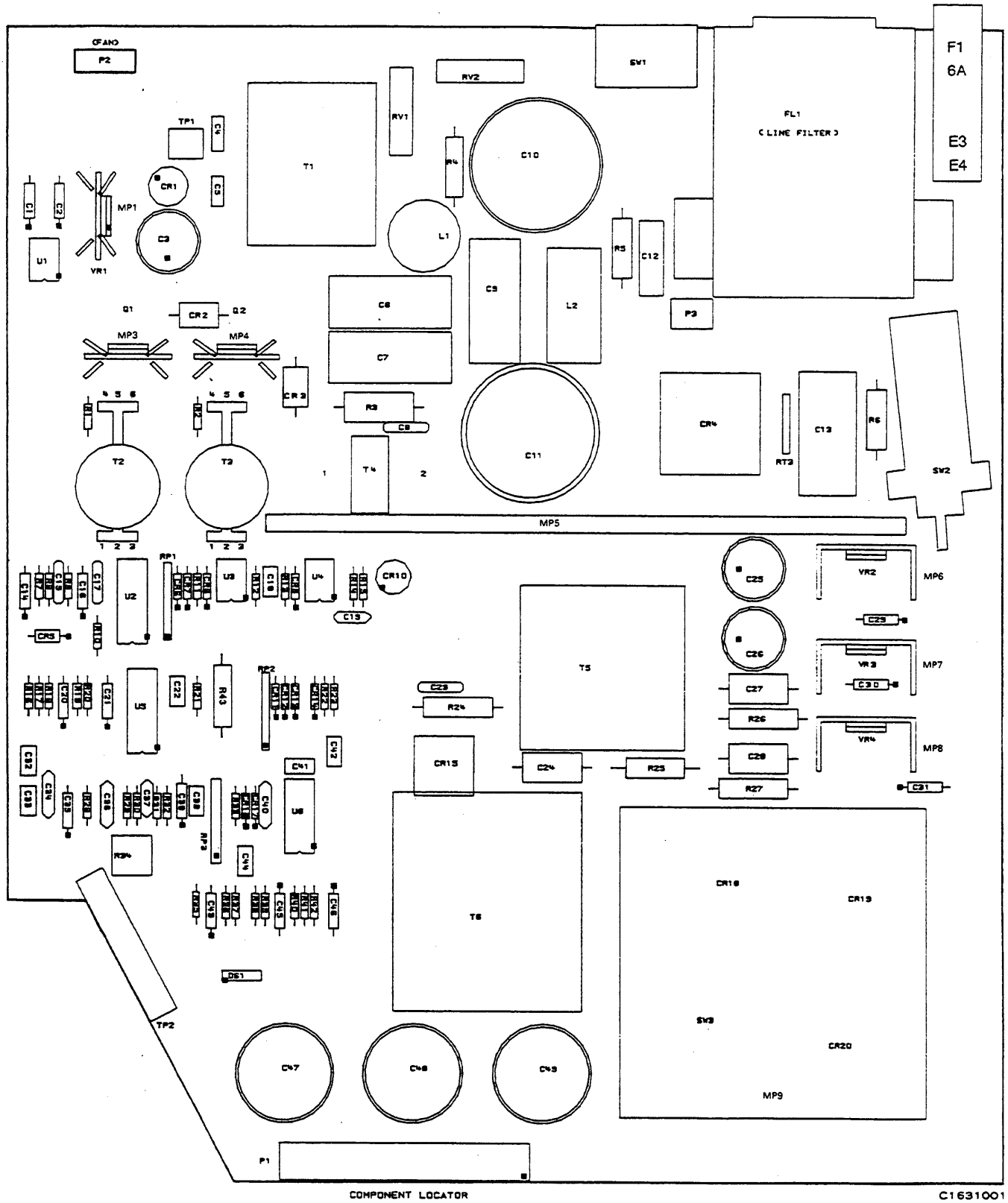
NOTES

8A-34. MNEMONICS

Signals on the power supply board have been assigned mnemonics that describe the function of the signal (see table 8-1. Logic Symbols). A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. An "H" prefix indicates that the function is active in the "high" state; an "L" prefix indicates that the function is active in the "low" state. The following table is a listing of the mnemonics used on the schematic.

Table 8A-2. Mnemonics

Mnemonic	Description
+12C	+12 V Control. This is the control voltage used throughout the supply. If +12C is not in regulation, the supply will not operate properly.
CC1,2	Cross Conduction 1 and 2. Complementary signals used to prevent both switching transistors from being ON at the same time.
NORM	Normal. When this LED is ON, the power supply is working correctly.
OV	Over Voltage. When this LED is ON, either the +5 or -5.2 volt supply has exceeded its voltage limits. When asserted, the PWM U5 will be shut OFF.
PL	Primary Limit. When this LED is ON, a non-linear surge in current has occurred in the primary section. When asserted, the PWM U5 will be shut OFF.
PWM5VREF	Pulse Width Modulator 5 V Reference. A +5 volt reference from U5's internal reference regulator.
R+5	Return +5. The voltage on this line is the DC component of the +5 volt supply. It is used to set the current foldback limit of the +5 current limit circuit.
R-2.4	Return -2.4. The voltage on this line is the DC component of the -2.4 volt supply. It is used to set the current foldback limit of the -2.4 current limit circuit.
R-5.2	Return -5.2. The voltage on this line is the DC component of the -5.2 volt supply. It is used by the PWM U5 to set the foldback current limit of the -5.2 volt supply.
SHUTDOWN	This signal is generated in several places and is responsible for turning OFF the PWM U5 by pulling pin 3 high.
TH	Thermal. Thermal switch SW3 opens when the internal temperature of the supply is greater than 105 degrees C. When the TH LED is ON, PWM U5 is turned OFF.



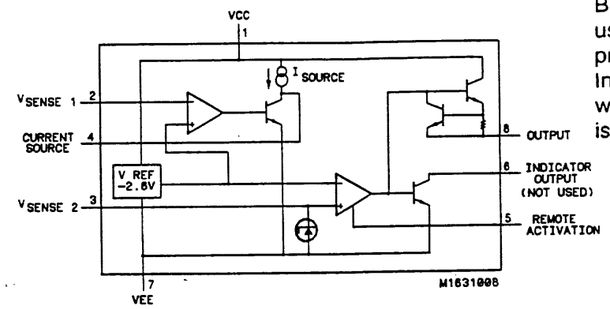
Power Supply Board Component Locator

NOTE 1

Probing these pins may cause unwanted symptoms.

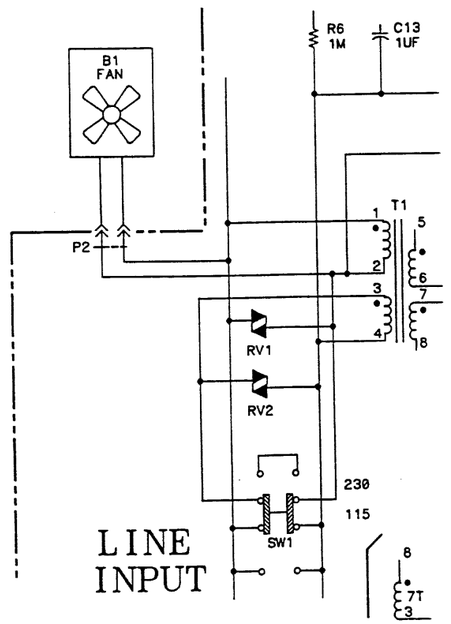
NOTE 2

Functional diagram for U3 and U4



NOTE 3

Below is the 120 V fan and input circuit used in 1630A/D with serial prefixes before 2412A.

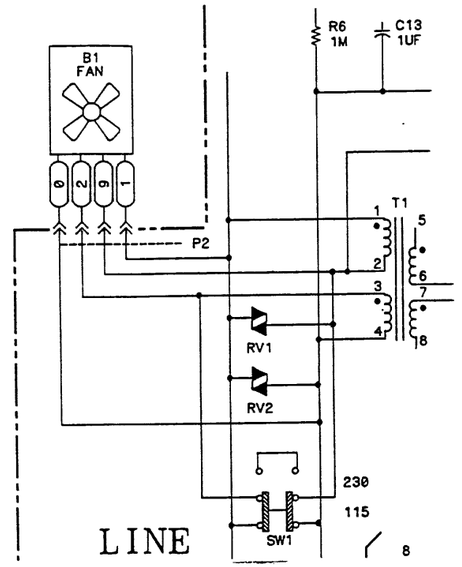


NOTE 4

R15 was changed from 68.1Ω to 51.1Ω to solve a start-up current limiting problem on the 1630G. See Service Note 1630G-2.

NOTE 5

Below is the 120/240 V fan and input circuit used in 1630A/D/G and 1631A/D with serial prefixes from 2412A to approximately 2603A. Instruments can be recognized by the four wires between the fan and power supply. R37 is 56.2K on these and older instruments.



NOTE 6

On early boards, R19 is 619K and R50 is not used. See instrument history.

NOTE 7

On 66514/25/29 boards the pin numbering of T5, as marked on the board, is different from the schematic.

Schem.	1	2	3	4	5	6	7	8	9	10
Board	5	4	3	2	1	10	9	8	7	6

B1 FAN

RT1 5

RT3 5

V1

V2

RT2 5

R6i 1MI

C13 1UF

CR4

C10 560UF

C11 560UF

P3

L2

L1

R4 100K

R5 100K

C9 1UF

C12 0.022UF

WARNING

HAZARDOUS VOLTAGES ARE PRESENT ON THESE LINES

WARNING

C10 & C11 REMAIN CHARGED AFTER POWER IS REMOVED. WAIT THREE MINUTES FOR CAPS TO DISCHARGE BEFORE SERVICING THIS CIRCUITRY.

P2

R43 3.3

-5.2V

+5V

SEE NOTE 3

SEE NOTE 5

RV1

RV2

T1

16VAC RMS

C5 0.01UF

C4 0.01UF

CR1

TP1 TEST CONNECTOR

MP1

VR1

U1

+12VC

+5VREF

C3 330UF

C2 1UF

C1 1UF

VR1-4

CONTROL SECTION POWER SUPPLY

230

115

SW1

SW2

OFF

ON

F1

FL1

L

N

AC INPUT

LINE INPUT

P/O T5 (SECONDARIES)

FOR T5 NUMBERING SEE NOTE 7

SECONDARY SECTION

7T

7T

C23 2200

R24 75

CR15

P/O T6

C25 330UF

MP7

VR3

C30 1UF

MP6

VR2

C29 1UF

C26 330UF

VR4

MP8

C31 1UF

W5

2T

W4

2T

W3

R25 12

C24 0.039UF

CR18

P/O T6

C47 3300UF

C51 0.47UF

-5.2VRET

-5.2V

4

1T

6

1T

5

R26 12

C27 0.039UF

CR19

C48 3300UF

C54 0.47UF

-2.4VRET

-2.4V

1

2T

9,10

2T

2

R27 12

C28 0.039UF

CR20

C49 3300UF

P/O DS1 "NORM"

C50 0.47UF

+5VRET

+5V

CC1

CC2

NC

1,2

P1

+15V

3,4

OUTPUT TO MOTHERBOARD

+12V

5,6

GND

9-24

-12V

7,8

-5.2V

37-50

-2.4V

31-36

+5V

25-30

+5V

5

-2.4V

4

-5.2V

3

-12V

2

GND

1,8

+12V

6

+15V

7

TEST CONNECTOR

TP2

+5VREF

R42 392K

+12VC

P/O RP3 4700

-2.4VRET

R40 130K

-2.4V

C45 1UF

+.06V

U6C

C41 0.01UF

CR16

-2.4 CURRENT LIMIT

P/O RP3 4700

+5V

+12VC

C43 1UF

R35 909K

R36 2000

+5VRET

FOR R37 NOTE 5

R37 31.6K

U6D

CR17

4700 P/O RP3

C40 2000

4700 P/O RP3

+5V CURRENT LIMIT

+5V OVERVOLTAGE

P/O RP2 4700

CR13

PWM +5VREF

P/O DS1 "OV"

R38 10K

+5V

R39 56.2K

C44 0.01UF

U6A

CR11

U2E

U2A

R41 7500

+5VREF

C46 1UF

+12VC

R23 4750

R22 7500

-5.2V

+5.33V

C42 0.01UF

U6B

CR12

U2D

P/O RP2 4700

-5.2V

CC2

CR6

CC1

CR7

U2C

U2B

P/O RP1 4700

-5.2V

+5VREF

R5 75

-5.2VRET

R17 4.75K

R16 75K

-5.2V

C39 0.01UF

C38 1UF

-5.

-5.2V OVERVO (U6B)

PULSE NON-OVER CIRCU

WARNING

RDOUS VOLTAGES
E PRESENT ON
HESE LINES

WARNING

C10 & C11 REMAIN CHARGED AFTER POWER IS REMOVED. WAIT THREE MINUTES FOR CAPS TO DISCHARGE BEFORE SERVICING THIS CIRCUITRY.

+12VC

+5VREF

VR1-4

SWITCHING CIRCUITRY

C6 1UF
C7 1UF
P/O T5 (PRIMARY)
W1 W2 31T
R3 47
C8 2000
CR2
CR3
MP3 Q1
MP4 Q2
R1 51.1
R2 51.1
4 8T
5
6 1T
P/O T2 (SECONDARY)
P/O T3 (SECONDARY)
T4 60T
CR10
R14 10K
R15 51.1
C19 240
NOTE 4
+12VC
P/O DS1
U4
CR9
R13 1000
FOR U3 & U4 SEE NOTE 2

PRIMARY CIRCUIT CURRENT LIMIT

THERMAL SHUTDOWN

+5VREF
R42 392K
P/O RP3 4700
-2.4VRET
R40 130K
-2.4V
C45 1UF
+.06V
+12VC
U6C
C41 0.01UF
CR16

-2.4 CURRENT LIMIT

P/O RP3 4700

MODULATION CONTROL CIRCUITRY

FOR R19 & R50 SEE NOTE 6

+5V
+12VC
R35 909K
C43 1UF
R36 2000
+5VRET
FOR R37 NOTE 5
R37 31.6K
U6D
CR17
C40 2000
4700 P/O RP3

+5V CURRENT LIMIT

+5VREF
R50 75K
+5V
C35 1UF
-5.2VRET
R17 4.75K
R16 75K
-5.2V
R19 68.1K
R20 4750
C37 75
R30 130K
C34 2000
R18 10K
C32 0.01UF
C20 1UF
R32 7.5K
R28 10K
R31 22.1K
R29 9090
SEE NOTE 1
C36 2000
C39 0.01UF
R33 1000
C38 1UF
-5.2V
R34 1000
VOLT ADJ
R21 2.74K
C22 0.01UF
PWM +5VREF
C21 1UF
RP2 4.7K
[OC]
FF
OSC
U5

PULSE WIDTH MODULATOR

PWM+5VREF
+12VC
P/O DS1
U3
CR8
R11 1000
C18 0.01UF
R12 1000
N C THERMAL SWITCH 105C SW3
MP9

SWITCHING TRANSISTOR BASE DRIVE (PRIMARIES)

+12VC
P/O RP1 4.7K
U2F
U2G
P/O T2
P/O T3
80T
CR5
R7 274
C14 1UF
R9 274
C16 1UF
C17 2000
R10 475
C15 2000
R8 475

+5V OVERVOLTAGE

P/O RP2 4700
CR13
R38 10K
+5V
R39 56.2K
C44 0.01UF
PWM +5VREF
U6A
CR11
U2E
P/O DS1 "OV"
R41 7500
+5VREF
C46 1UF
+12VC
R22 7500
R23 4750
-5.2V
+5.33V
C42 0.01UF
U6B
CR14
CR12
U2A
U2D
P/O RP2 4700
-5.2V

-5.2V OVERVOLTAGE (U6B)

CC2
CR6
CC1
CR7
P/O RP1 4700
U2C
U2B

PULSE NON-OVERLAP CIRCUIT

P6
P1
C29 1UF
NC 1,2
+15V 3,4
OUTPUT TO MOTHERBOARD
+12V 5,6
GND 9-24
-12V 7,8
-5.2V 37-50
-2.4V 31-36
+5V 25-30
+5V 5
-2.4V 4
-5.2V 3
-12V 2
GND 1,8
+12V 6
+15V 7
TEST CONNECTOR
TP2
CC1
CC2

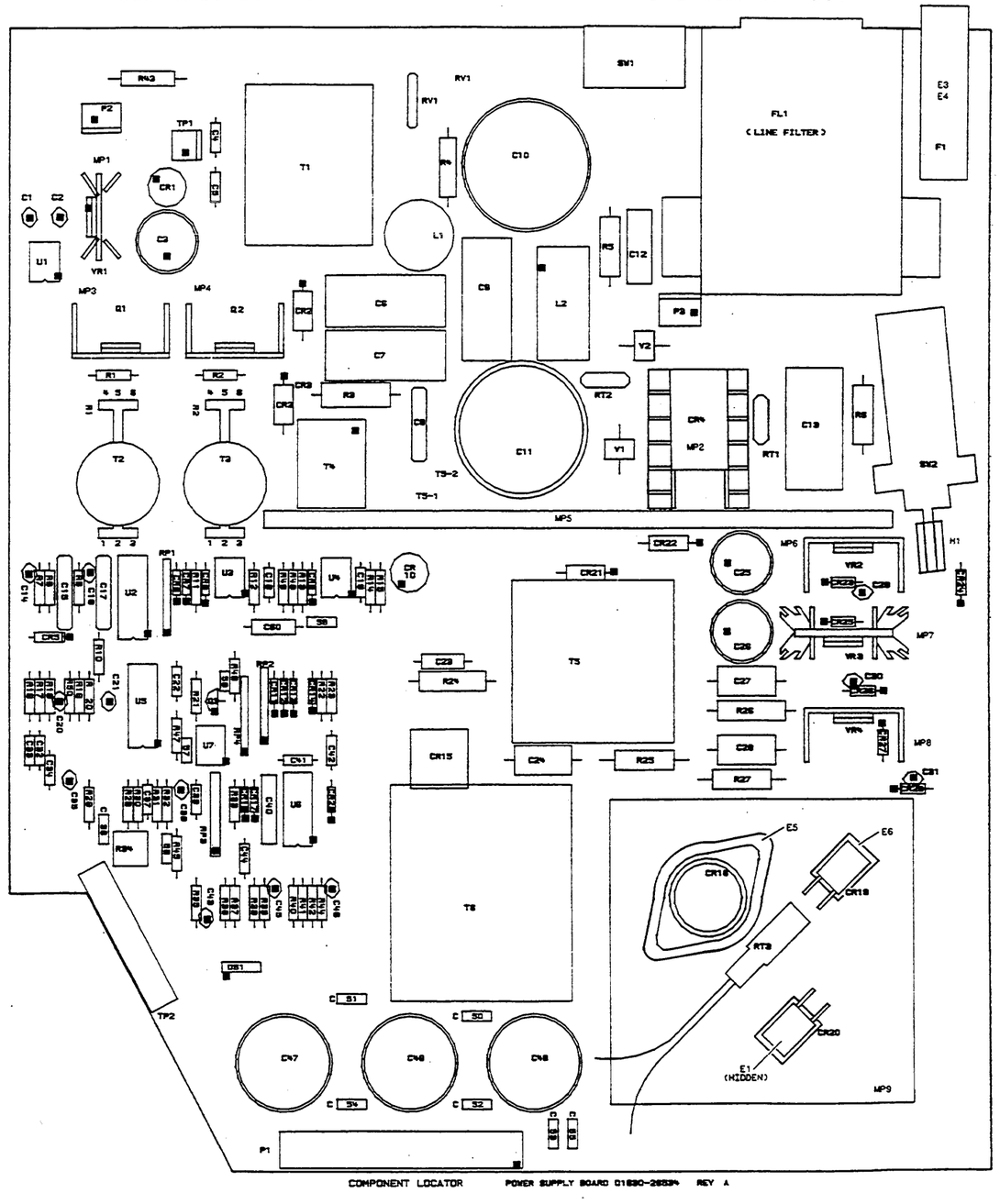
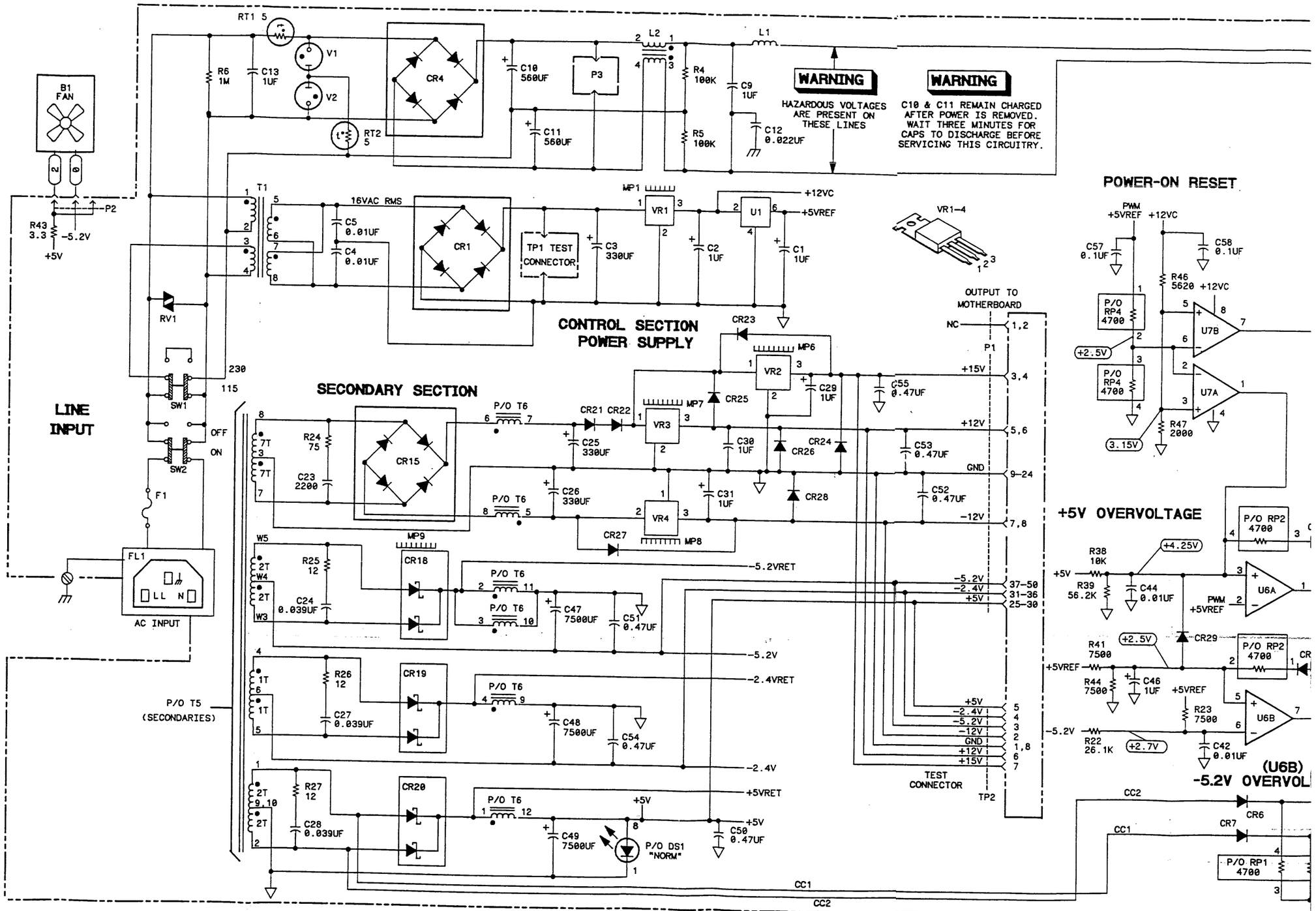


Figure 8A-6. Power Supply Component Locator (01630-66534 and later)



WARNING
HAZARDOUS VOLTAGES ARE PRESENT ON THESE LINES
WARNING
C10 & C11 REMAIN CHARGED AFTER POWER IS REMOVED. WAIT THREE MINUTES FOR CAPS TO DISCHARGE BEFORE SERVICING THIS CIRCUITRY.
LINE INPUT
AC INPUT
CONTROL SECTION POWER SUPPLY
SECONDARY SECTION
POWER-ON RESET
+5V OVERVOLTAGE
(U6B) -5.2V OVERVOL
TP1 TEST CONNECTOR
OUTPUT TO MOTHERBOARD
TEST CONNECTOR
P/O T5 (SECONDARIES)
16VAC RMS
P/O DS1 "NORM"

WARNING

C10 & C11 REMAIN CHARGED AFTER POWER IS REMOVED. WAIT THREE MINUTES FOR CAPS TO DISCHARGE BEFORE SERVICING THIS CIRCUITRY.

VOLTAGES SENT ON LINES

VR1–4

OUTPUT TO MOTHERBOARD

NC 1,2
P1
+15V 3,4
+12V 5,6
GND 9–24
−12V 7,8
−5.2V 37–50
−2.4V 31–36
+5V 25–30

+5V 5
−2.4V 4
−5.2V 3
−12V 2
GND 1,8
+12V 6
+15V 7

C55 0.47UF
C53 0.47UF
C52 0.47UF

TEST CONNECTOR
TP2

POWER-ON RESET

PWM +5VREF +12VC
C57 0.1UF
C58 0.1UF
R46 5620 +12VC
P/O RP4 4700
U7B
U7A
+2.5V
P/O RP4 4700
3.15V
R47 2000

+5V OVERVOLTAGE

P/O RP2 4700
CR13
R38 10K
+4.25V
+5V
R39 56.2K
C44 0.01UF
U6A
PWM +5VREF
CR11
P/O DS1 "OV"
U2E
U2A
CR29
R41 7500
+2.5V
+5VREF
P/O RP2 4700
CR14
R44 7500
C46 1UF
U2D
+5VREF
R23 7500
U6B
CR12
−5.2V
R22 26.1K
+2.7V
C42 0.01UF
P/O RP2 4700
−5.2V
U2C
CC2
CR6
CC1
CR7
U2B
P/O RP1 4700
−5.2V

(U6B) −5.2V OVERVOLTAGE

−2.4 CURRENT LIMIT

+5VREF
R42 392K
P/O RP3 4700
−2.4VRET
R40 130K
C45 1UF
+.06V
+12VC
U6C
−2.4V
P/O RP3 4700
C41 0.01UF
CR16

+5V CURRENT LIMIT

+12VC
+5V
C43 1UF
R35 909K
R36 2000
+5VRET
U6D
+5V
4700 P/O RP3
R37 42.2K
C40 2200
4700 P/O RP3
CR17

SWITCHING CIRCUITRY

C6 1UF
C7 1UF
P/O T5 (PRIMARY)
W1 W2
31T
R3 47
C8 2200
CR2
CR3
MP3 Q1
MP4 Q2
R1 51.1
R2 51.1
4 8T
5
6 1T
P/O T2 (SECONDARY)
P/O T3 (SECONDARY)
1T
T4 50T
CR10

PRIMARY CIRCUIT CURRENT LIMIT

R14 10K
+12VC
U4
R15 42.2
C19 150
C59 0.1UF
P/O DS1
R48 1000
R49 1000
R13 1000
CR9

THERMAL SHUTDOWN

FOR U3 & U4 SEE NOTE 2

PULSE WIDTH MODULATOR

C37 150
R30 64.9K
C34 0.015UF
R18 10K
C32 0.01UF
+5VREF
R19 68.1K
R20 4750
+12VC
[+V]
U5
OSC
FF
[OC]
[GND]
PWM +5VREF
R28 10K
C20 1UF
R29 9090
SEE NOTE 1
R34 1000
VOLT ADJ
R21 2.74K
C22 0.01UF
C21 1UF

SOFT-START

PWM +5VREF
P/O RP4 4700
Q3
P/O RP2 4700

PULSE NON-OVERLAP CIRCUIT

−5.2VRET +5VREF
C35 1UF
R17 4750
R50 75K
R16 75K
−5.2V
C36 0.1UF
R32 7500
R45 4750
C56 0.047 UF
R31 22.1K
C39 0.01UF
R33 1000
C38 1UF
−5.2V

SWITCHING TRANSISTOR BASE DRIVE (PRIMARIES)

+12VC
P/O DS1
U3
PWM+5VREF
CR8
R11 1000
C18 0.01UF
R12 1000
C60 0.22UF
RT3
PWM+5VREF
+12VC
P/O RP1 4.7K
U2F
P/O T2
80T
CR5
R7 274
C14 1UF
+12VC
P/O RP1 4.7K
U2G
P/O T3
80T
R9 274
C16 1UF
C17 2200
R10 475
C15 2200
R8 475

8A-2

S1631090/3-9-88

Schematic 8A-2
Power Supply (01630-66534 and later)

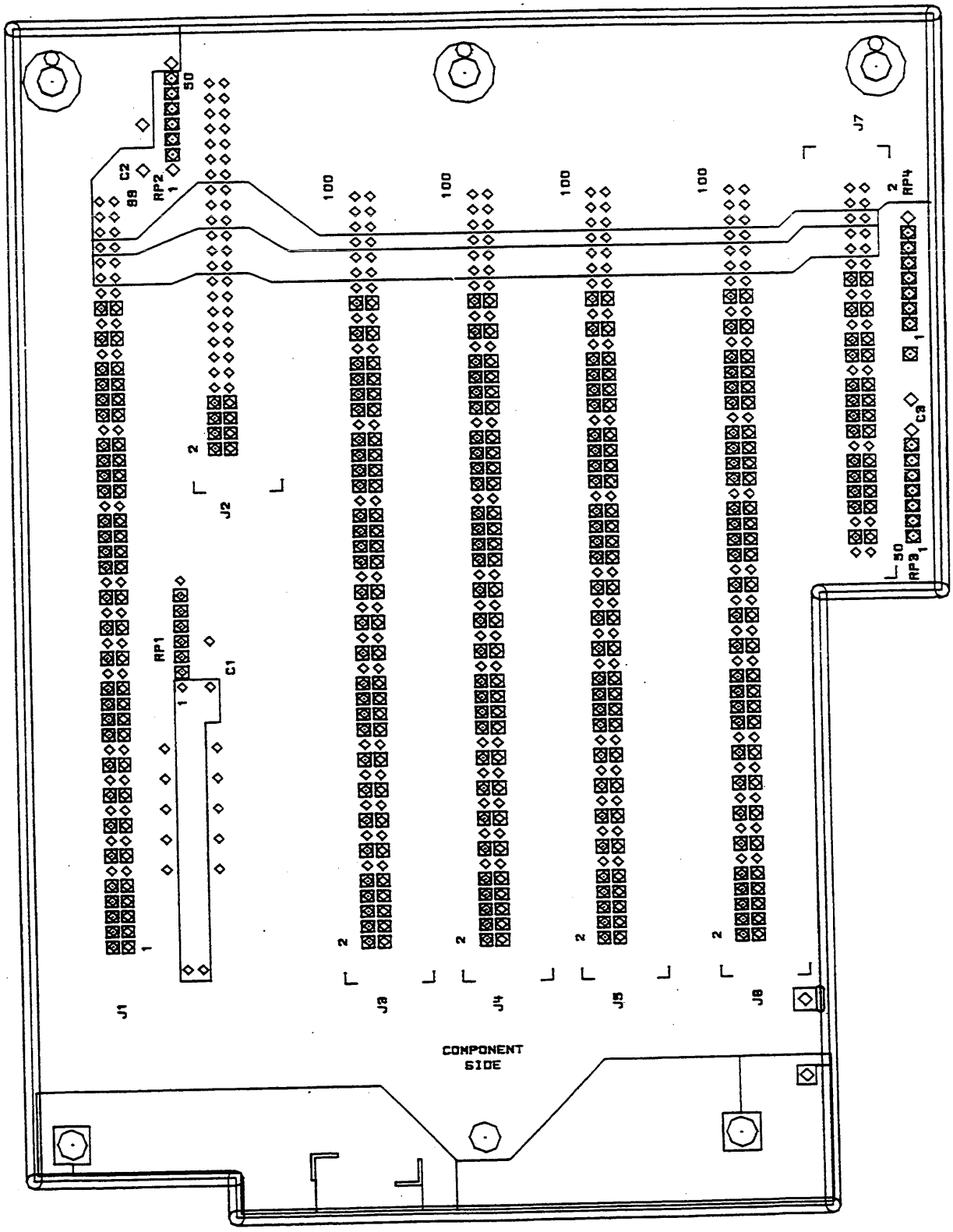


Figure 8A-7. Motherboard Component Locator

Table 8A-3. Motherboard Connections & Signal Distribution.

SIGNAL	J3-J6 PINS	CPU J6	STATE MASTER J5	TIMING MASTER J4	TIMING SLAVE J3	STATE SLAVE J3	TERM. LOC. (NOTE 3)	ANALOG J7	ANALOG J7 PINS
GS4	1	B-7	[C-1]						
THR4	2	[B-7]	C-1						
GS3	3	B-7	[C-1]						
THR3	4	[B-7]	C-1						
GS2	5	B-7	[C-1]						
THR2	6	[B-7]	C-1						
GS0	7	B-7		[D-1]					
THR0	8	[B-7]		D-1					
GS1	9	B-7			[E-1]	[F-1]			
THR1	10	[B-7]			E-1	F-1			
GND	11,12								
NOT USED	13								
NOT USED	14								
GND	15,16								
HGS	17	NC	NC	D-2	[E-1]				
LTS	18	NC	NC	D-2	[E-1]				
GND	19,20								
HSWS	21	NC	[C-7]		E-2	F-3			
HSWM	22	NC	[C-7]	D-4					
GND	23,24								
HSCS	25	NC	[C-6]		E-1	F-3			
HSCM	26	NC	[C-6]	D-1					
GND	27,28								
LDS	29	NC	C-3		[E-1]	[F-2]	C-3		
LDM	30	NC	C-3	[D-1]			C-3		
LCS	31	NC	C-3		[E-1]	[F-2]	C-3		
LCM	32	NC	C-3	[D-1]			C-3		
LBS	33	NC	C-3		[E-1]	[F-2]	C-3		
LBM	34	NC	C-3	[D-1]			C-3		
LAS	35	NC	C-3		[E-1]	[F-2]	C-3		
LAM	36	NC	C-3	[D-1]			C-3		
GND	37,38								
LSTP	39	NC	NC	[D-4]	E-2				
HSQ3	40	B-1	[C-4]				1-3,3-2		
GND	41,42								
LTCK	43	[B-1]		[D-3]	E-2		1-5,3-4		
HTCK	44	[B-1]		[D-3]	E-2		1-4,3-3		
GND	45,46								49,50
HACK	47	[B-1]		[D-3]		F-3	1-7,3-6	G-2	47
LACK	48	[B-1]		[D-3]		F-3	1-6,3-5	G-2	48
GND	49,50								45,46

NOTES: 1) ALL PINS OF CONNECTORS J1 (SERVICE CONNECTOR), AND J3 THRU J6 ARE BUSED TOGETHER, WITH THE EXCEPTION OF THOSE MARKED "NC".

2) X-X (LETTER-NUMBER) INDICATES THE SECTION (BOARD) AND SCHEMATIC THAT A SIGNAL IS FOUND, WITH [ ] INDICATING A SOURCE OF THE SIGNAL.

3) TERMINATION LOCATION SHOWS WHERE A SIGNAL IS PULLED LOW (ECL) WITH X-X (LETTER-#) GIVING SCHEMATIC AND #-# GIVING MOTHERBOARD RP# AND PIN#.

Table 8A-3. Motherboard Connections & Signal Distribution (cont.).

SIGNAL	J3-J6 PINS	CPU J6	STATE MASTER J5	TIMING MASTER J4	TIMING SLAVE J3	STATE SLAVE J3	TERM. LOC. (NOTE 3)	ANALOG J7	ANALOG J7 PINS
HD7	51	B-2	C-8	D-5	E-2	F-5	B-2	G-4	44
HD6	52	↕	↕	↕	↕	↕	↕	↕	43
HD5	53	↕	↕	↕	↕	↕	↕	↕	42
HD4	54	↕	↕	↕	↕	↕	↕	↕	41
HD3	55	↕	↕	↕	↕	↕	↕	↕	40
HD2	56	↕	↕	↕	↕	↕	↕	↕	39
HD1	57	↕	↕	↕	↕	↕	↕	↕	38
HD0	58	B-2	C-8	D-5	E-2	F-5	B-2	G-4	37
GND	59,60								35,36
HA5	61	[B-2]	C-8	D-5	E-2	F-5	B-2	G-4	34
HA4	62	↕	↕	↕	↕	↕	↕	↕	33
HA3	63	↕	↕	↕	↕	↕	↕	↕	32
HA2	64	↕	↕	↕	↕	↕	↕	↕	31
HA1	65	↕	↕	↕	↕	↕	↕	↕	30
HA0	66	[B-2]	C-8	D-5	E-2	F-5	B-2	G-4	29
HR/LW	67	[B-2]	C-8	D-5	E-2			G-4	28
NOT USED	68								27
GND	69,70								25,26
NOT USED	71								
NOT USED	72								
+15	73	B-1							
+15	74	B-1							
+12	75	B-1				F-4		G-2	24
+12	76	B-1				F-4		G-2	23
-12	77	B-1				F-4		G-2	22
-12	78	B-1				F-4		G-2	21
GND	79,80								19,20
LSTB	81	[B-2]	C-8	D-5	E-2	F-3	2-5,4-3	G-4	18
LMCI	82	B-6	[C-4]	[D-2]			2-6,4-2	[G-2]	17
GND	83,84								15,16
HARM	85		[C-4]C-4	[D-1]D-1			2-2,4-5	[G-4]G-4	14
HBNC	86	B-7	[C-4]	[D-2]			2-3,4-4	[G-2]	13
GND	87,88								11,12
+5	89,90	B-1	C-8	D-5	E-1	F-4		G-2	9,10
+5	91,92	↕	↕	↕	↕	↕		↕	7,8
-2.4	93,94	↕	↕	↕	↕	↕		↕	5,6
-5.2	95,96	↕	↕	↕	↕	↕		↕	3,4
-5.2	97,98	↕	↕	↕	↕	↕		G-2	1,2
-5.2	99,100	B-1	C-8	D-5	E-1	F-4			

NOTES: 1) ALL PINS OF CONNECTORS J1 (SERVICE CONNECTOR), AND J3 THRU J6 ARE BUSED TOGETHER, WITH THE EXCEPTION OF THOSE MARKED "NC".

2) X-X (LETTER-NUMBER) INDICATES THE SECTION (BOARD) AND SCHEMATIC THAT A SIGNAL IS FOUND, WITH [ ] INDICATING A SOURCE OF THE SIGNAL.

3) TERMINATION LOCATION SHOWS WHERE A SIGNAL IS PULLED LOW (ECL) WITH X-X (LETTER-#) GIVING SCHEMATIC AND #-# GIVING MOTHERBOARD RP# AND PIN#.

Service Group 8B Table of Contents

Paragraph		Page
8B-1.	Introduction	8B-1
8B-2.	Block Diagram Theory	8B-1
8B-3.	Theory of Operation	8B-7
8B-4.	Control Timing	8B-7
8B-5.	System Timing Controller	8B-7
8B-6.	Control Latches	8B-7
8B-7.	Microprocessing Circuitry	8B-8
8B-8.	MPU Operation	8B-8
8B-9.	MMU Operation	8B-9
8B-10.	Power Up-Master Reset	8B-10
8B-11.	Acquisition Interface	8B-10
8B-12.	Acquisition Addressing	8B-10
8B-13.	Acquisition Data	8B-10
8B-14.	Full-Field Scanning Generation and Graphics MUX	8B-12
8B-15.	Scanning	8B-12
8B-16.	Graphics MUX	8B-12
8B-17.	Waveform Formatter	8B-12
8B-18.	ROM and ROM Selection	8B-12
8B-19.	RAM Timing Control and RAMs	8B-15
8B-20.	RAM Timing Control	8B-15
8B-21.	RAM	8B-15
8B-22.	CRT Control	8B-15
8B-23.	CRT Controller (CRTC) Operation	8B-15
8B-24.	CRTC Interfacing	8B-15
8B-25.	Horizontal and Vertical Sync	8B-16
8B-26.	Display Enable and Cursor Outputs	8B-16
8B-27.	RAM Addressing	8B-16
8B-28.	Raster Addresses	8B-16
8B-29.	Character Generation	8B-16
8B-30.	Character ROM	8B-16
8B-31.	Display Data Shift Register	8B-17
8B-32.	Graphics Output Buffer	8B-17
8B-33.	Display Data Latches	8B-17
8B-34.	Display Control	8B-17
8B-35.	I/O Decoding	8B-18
8B-36.	Macro I/O Decoding	8B-18
8B-37.	Micro I/O Decoding	8B-19
8B-38.	Interrupt Processing	8B-19
8B-39.	HP-Interface Bus (HP-IB) Circuitry	8B-20
8B-40.	MPU to HP-IB Interface	8B-20

Service Group 8B Table of Contents (Cont'd)

Paragraph		Page
8B-41.	HP-IB Interface Lines and Operations	8B-20
8B-42.	HP-IB Transceivers	8B-22
8B-43.	System Status Switches	8B-22
8B-44.	BNC Outputs	8B-22
8B-45.	HP-Interface Loop (HP-IL) Circuitry	8B-22
8B-46.	General Information	8B-22
8B-47.	MPU to HP-IL Interface	8B-23
8B-48.	HP-IL Interface Lines and Operations	8B-23
8B-49.	Probe Reference Voltage Adjust	8B-24
8B-50.	Probe Threshold Selection	8B-24
8B-51.	Additional Information	8B-24
8B-52.	Keyboard Scanning	8B-24
8B-53.	MPU to Keyboard Controller Interface	8B-24
8B-54.	Keyboard Scan Operations	8B-25
8B-55.	Keyboard Switch Pad	8B-26
8B-56.	Display System Operation Verification and Troubleshooting	8B-26
8B-57.	Mnemonics	8B-29

List of Illustrations

Figure		Page
8B-1.	CPU Block Diagram	8B-5
8B-2.	Acquisition Write Timing Waveforms	8B-11
8B-3.	Acquisition Read Timing Waveforms	8B-11
8B-4.	Display Character Area	8B-13
8B-5.	Display Timing Waveforms for One MPU Cycle	8B-14
8B-6.	RAM Timing Waveforms for One MPU Cycle	8B-14
8B-7.	A Typical 9 x 16 Dot Pattern for a Character	8B-17
8B-8.	HP-IB Signal Lines	8B-20
8B-9.	HP-IB Handshake Timing for One Talker and Multiple Listeners	8B-21
8B-10.	Keyboard Switch to Sensor Matrix Address Locations	8B-25

List of Tables

Table		Page
8B-1.	Control Latch Bit Assignments	8B-8
8B-2.	Physical Address-to-Function Allocation	8B-9
8B-3.	Macro I/O Physical Address-to-Function	8B-18
8B-4.	Micro I/O Physical Address-to-Function	8B-19
8B-5.	CPU to Display Driver Cable Pin Assignments	8B-26
8B-6.	Applicable Electrical Specifications	8B-27
8B-7.	Typical Operating Voltages for the CRT	8B-29
8B-8.	Mnemonics	8B-30

List of Schematics

Schematic		Page
8B-1.	System Timing Control, Beeper	8B-35
8B-2.	Master Reset, MPU, MMU	8B-37
8B-3.	Display Control and ROM	8B-39
8B-4.	40MHz Clock, Memory Control	8B-41
8B-5.	CRT Controller, Character ROM, Display Control	8B-43
8B-6.	I/O Decoding, Interrupt Processing	8B-45
8B-7.	HP-IB Control, Threshold Reference and Drivers	8B-47
8B-8.	Keyboard	8B-49

NOTE 1

CPU BOARDS 01630-66503 AND 01630-66512 ORIGINALLY HAVE U6M PIN 25 AS "NC". THESE BOARDS MAY BE MODIFIED TO RUN IN A 1630G AND HAVE PIN 25 JUMPERED TO +5V.

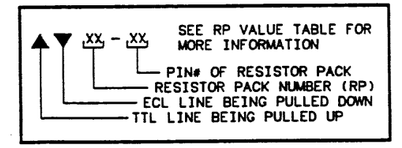
NOTE 2

CPU BOARDS 01630-66503, 66512, 66519, AND 66522 DO NOT HAVE U3P AND U3Q AND THEIR ASSOCIATED CIRCUITRY. U2P IS ALSO DESIGNATED U3P ON THOSE BOARDS.

IC DEVICE POWER CONNECTIONS

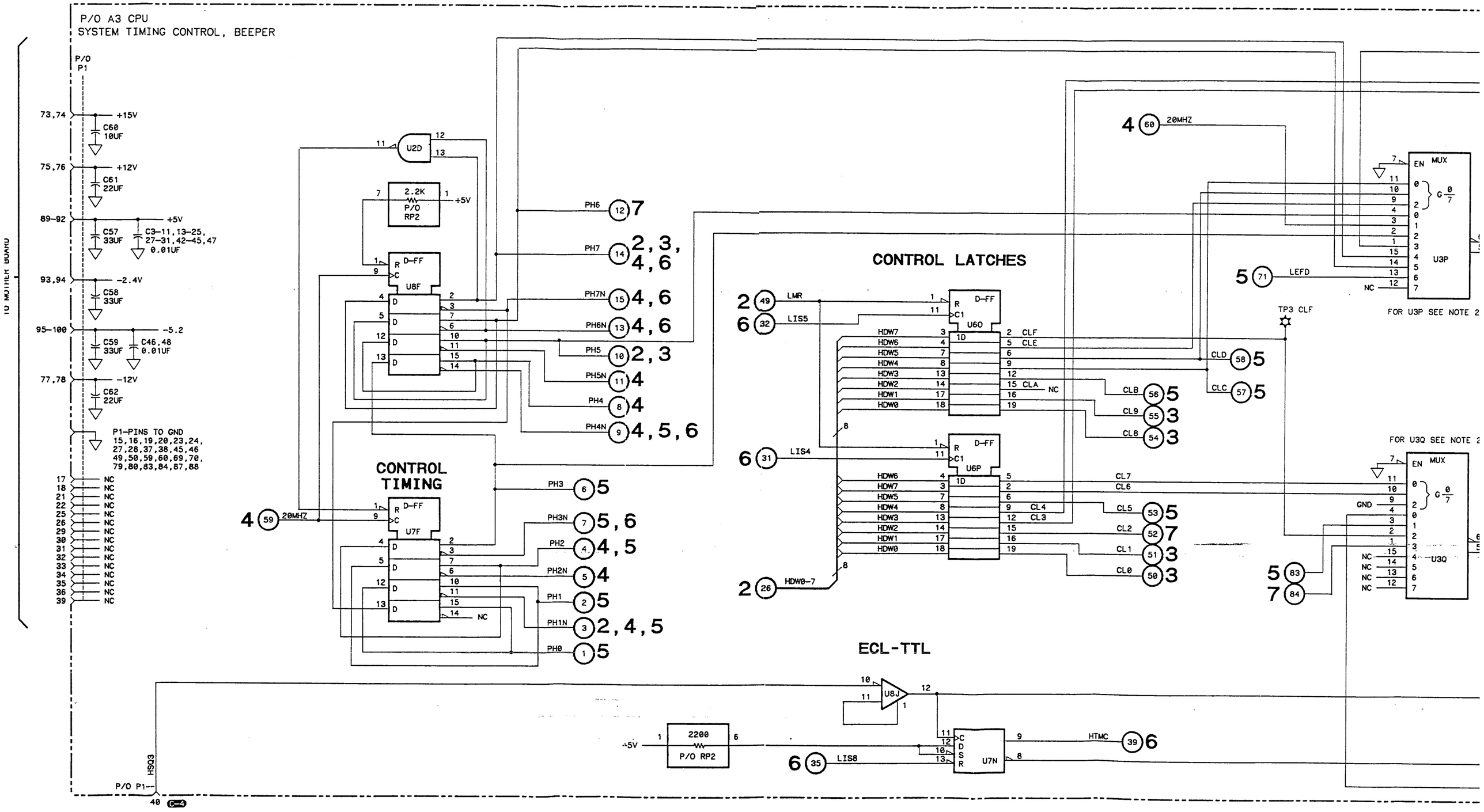
SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U6O,P
+5 GND	14 7	U2D,3E,7N
+5 GND	1 21	U6M
+5 GND	16 8	U7F,8F
+5 -5.2 GND	9 8 16	U7M,8J
+5 -5.2 GND	1 8 16	U9M

RESISTOR PACK DESCRIPTIONS



PARTS ON THIS SCHEMATIC

C3-11,13-25,27-31, 42-48,57-62 LS1 R14,15,31 RP2,4 TP3 U2D,3E,6M,O,P, U7F,M,N,8F,J,9M	UY6Q



P/O A3 CPU
SYSTEM TIMING CONTROL, BEEPER
P/O P1
73,74 +15V C60 10UF
75,76 +12V C61 22UF
89-92 +5V C57 33UF C3-11,13-25, 27-31,42-45,47 0.01UF
93,94 -2.4V C58 33UF
95-100 -5.2 C59 33UF C46,48 0.01UF
77,78 -12V C62 22UF
P1-PINS TO GND 15,16,19,20,23,24, 27,28,37,38,45,46 49,50,59,60,69,70, 79,80,83,84,87,88
TO MOTHER BOARD
CONTROL TIMING
U2D
2.2K P/O RP2
+5V
D-FF U8F
D-FF U7F
20MHZ
PH6 7
PH7 2,3, 4,6
PH7N 4,6
PH6N 4,6
PH5 2,3
PH5N 4
PH4 4
PH4N 4,5,6
PH3 5
PH3N 5,6
PH2 4,5
PH2N 4
PH1 5
PH1N 2,4,5
PH0 5
CONTROL LATCHES
LMR
LIS5
LIS4
HDW0-7
D-FF U6O
D-FF U6P
HDW7 HDW6 HDW5 HDW4 HDW3 HDW2 HDW1 HDW0
CLF CLE CLA NC
CLB 5
CL9 3
CL8 3
CLD 5
CLC 5
CL7 CL6 CL4 CL3
CL5 5
CL2 7
CL1 3
CL0 3
20MHZ
LEFD
TP3 CLF
MUX U3P
FOR U3P SEE NOTE 2
FOR U3Q SEE NOTE 2
MUX U3Q
GND
ECL-TTL
U8J
2200 P/O RP2
+5V
LIS8
U7N
HTMC
HSQ3
P/O P1
C-4

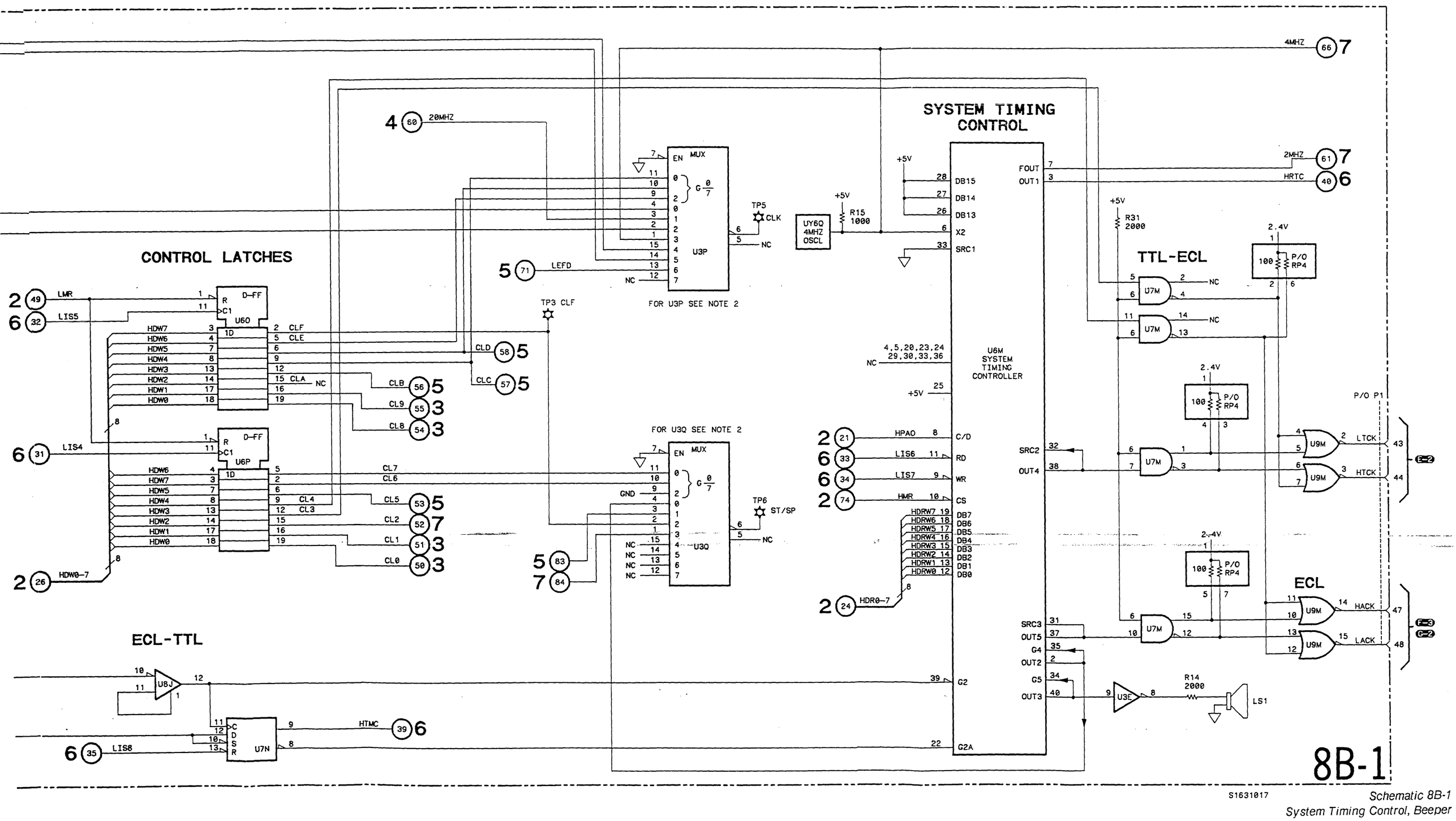
CONTROL LATCHES

SYSTEM TIMING CONTROL

TTL-ECL

ECL-TTL

ECL



S1631017

Schematic 8B-1
System Timing Control, Beeper

SERVICE GROUP 8B
CPU, DISPLAY, AND KEYBOARD

8B-1. INTRODUCTION

This service group contains block and component level theory, service and troubleshooting information necessary to service the CPU and keyboard. Service group 8B is separated into two sections; theory and troubleshooting.

The display system used by the logic analyzer is an OEM assembly and is not serviced by HP. The Display Driver, yoke, and CRT are each given a separate HP part number and should be ordered that way. The DISPLAY SYSTEM OPERATION VERIFICATION AND TROUBLESHOOTING section of this Service Group will aid the service person in determining whether or not the Display System or the CPU system is failing.

Note, the terms MPU and processor will be used throughout this manual in reference to the MC68B09E MICROPROCESSOR used on the CPU board.

8B-2. BLOCK DIAGRAM THEORY (see Figure 8B-1)

The block theory for service group 8B is focused at the CPU board because the control circuitry for the keyboard and display board is located on the CPU board. The order in which each block is described is also the order that each block is functionally described in the detailed theory of operation.

CONTROL TIMING. The control timing section provides the CPU board with fifteen timing waveforms. Each waveform and its complement has a frequency of 1.27 MHz and the delay between each adjacent phase group is 50 nS. For example PH1N and PH1 lead PH2N and PH2 by 50 nS.

SYSTEM TIMING CONTROLLER. The system timing controller (STC) is a processor programmable timer. It also provides a 2 MHz clock for the HP-IL controller, synchronization for a real-time clock, measurement time for the acquisition system, and a signal source for an audio feedback speaker.

CONTROL LATCHES. The processor uses these latches to control and/or enable eleven functions on the CPU board.

MICROPROCESSOR UNIT (MPU). The processor uses the 8-bit bi-directional data bus HDRW0-7 to communicate with and control devices in this system. Addresses A11-15 are used to select tasks from the Memory Management Unit (MMU). Physical Addresses 0-10 (HPA0-10) combine with addresses HPA11-20 from the MMU to form the Physical Address bus. Clocking of the MPU E and Q clock inputs is provided by the Control Timing Section.

MEMORY MANAGEMENT UNIT (MMU). Expanding the 64K addressable space of the processor, write protection, mapping and allocation of memory are some of the functions of the MMU. The MMU, controlled by the processor, outputs the Physical Addresses 11-20.

ACQUISITION ADDRESS INTERFACE. The processor uses this block to convert TTL logic address and control information into ECL logic for the all-ECL acquisition boards.

ACQUISITION DATA INTERFACE. In order for the processor to send data to or from the ECL logic acquisition boards, the data must be converted from TTL-to-ECL, or from ECL-to-TTL. This block also forms the 8-bit write only data bus labeled HDW0-7.

POWER UP MASTER RESET. The purpose of this block is to keep certain key devices on the CPU board OFF while the power supply is turning ON. Different reset logic levels are provided.

FULL-FIELD SCANNING GENERATION AND GRAPHICS MUX. This block provides the X and Y scanning information for RAM when graphics information is required in the full-field

graphics area of the display. Also, RAM refresh is provided during retrace.

WAVEFORM FORMATTER. The purpose of the Waveform Formatter circuitry is to sample state and/or timing data and convert it into waveform information. The data is sampled for a high or low level, an edge, or a glitch. The information or symbols that make a waveform are then displayed in the full-field graphics area via RAM and the graphics buffer.

ROM AND ROM SELECTION. The eight 8K word x 8 bit ROMs used by this system are each selected by an addressable 1 of 8 demultiplexer.

MPU ADDRESS MULTIPLEXER. This block multiplexes the first 16 Physical Addresses into 8 RAM address lines HRAA0-7. This allows the processor to address RAM during the proper processor cycle.

RAM TIMING CONTROL. This block generates the timing signals (LCAS and LRAS) necessary to read and write from RAM. The Address Multiplexer Select (AMS) signal allows one group of devices, either MPU, graphics, or CRT controller, to address RAM at a given time. Also generated is a 20 MHz clock used to clock control timing, the display data shift register and display data latches.

RAM. The CPU board uses eight 64K word x 1 bit dynamic RAMs. RAM is addressed by three groups of devices (MPU, Graphics, or CRTC) during a processor cycle time. The data from the eight RAM data lines (HRAD0-7) is used by the CRT Controller (CRTC), Character ROM, and graphics buffer.

CRT CONTROLLER (CRTC) AND CRT CONTROL MUX. The CRTC is the interface between the Display System and the processor. Controlling CRT scanning, retrace execution, and cursor positioning are some of the functions of the CRTC. Like the MPU, and the full-field scanning generator the CRTC is only allowed to address RAM at the proper time in a processor cycle. This is determined by the ON time of the CRT control multiplexers.

CHARACTER ROM. The Character ROM converts the ASCII code for a given character into the 9 x 16 dot pattern used by this system to display characters. The data output is loaded into the display data shift register where it is serialized and sent to the display.

DISPLAY DATA SHIFT REGISTER AND DISPLAY DATA LATCHES. This block takes parallel display information from the character ROM and the graphics buffer. The information is converted into a serial data stream and mixed with cursor and video brightness information. This data is then captured by the display data latches and supplied as video information to the display driver.

GRAPHICS OUTPUT BUFFER. The graphics output buffer routes graphics information from the waveform formatter (via RAM) into the display data shift register. When scanning of the full-field graphics area is occurring this circuit will be ON and the character ROM will be OFF.

DISPLAY CONTROL. Video brightness, cursor timing, and enabling and disabling of the character ROM and graphics output buffer are the functions of this block.

I/O DECODING. Input/output operations function in two separate levels according the amount of memory reserved to execute an I/O operation; these are macro and micro. A macro operation reserves thirty-two Physical Addresses to execute an I/O operation and a micro operation reserves two or less Physical Addresses. This circuit controls read and write operations of I/O devices.

INTERRUPT PROCESSING. This circuitry is responsible for sampling and masking interrupts. The status of all interrupting devices is available to the processor. The processor sets the priority of each interrupt, masks out lower priority interrupts, and services the interrupt with the highest priority. The priority and masking of each interrupt is determined by firmware.

HP-IB AND SYSTEM STATUS SWITCHES. Communication between separate systems is done over a high speed communications link called HP-IB. The Hewlett-Packard Interface Bus requires a device address, and a talk-only or a controlled status on the bus. The status

is determined by the settings of the system status switches.

BNC OUTPUTS. Two BNC ports are provided for the user. The BNC labeled PORT supplies one of seven signals from the acquisition system on a multiplexed basis. The other labeled ACCESSORY POWER is a regulated +5 volt supply for use by a preprocessor option.

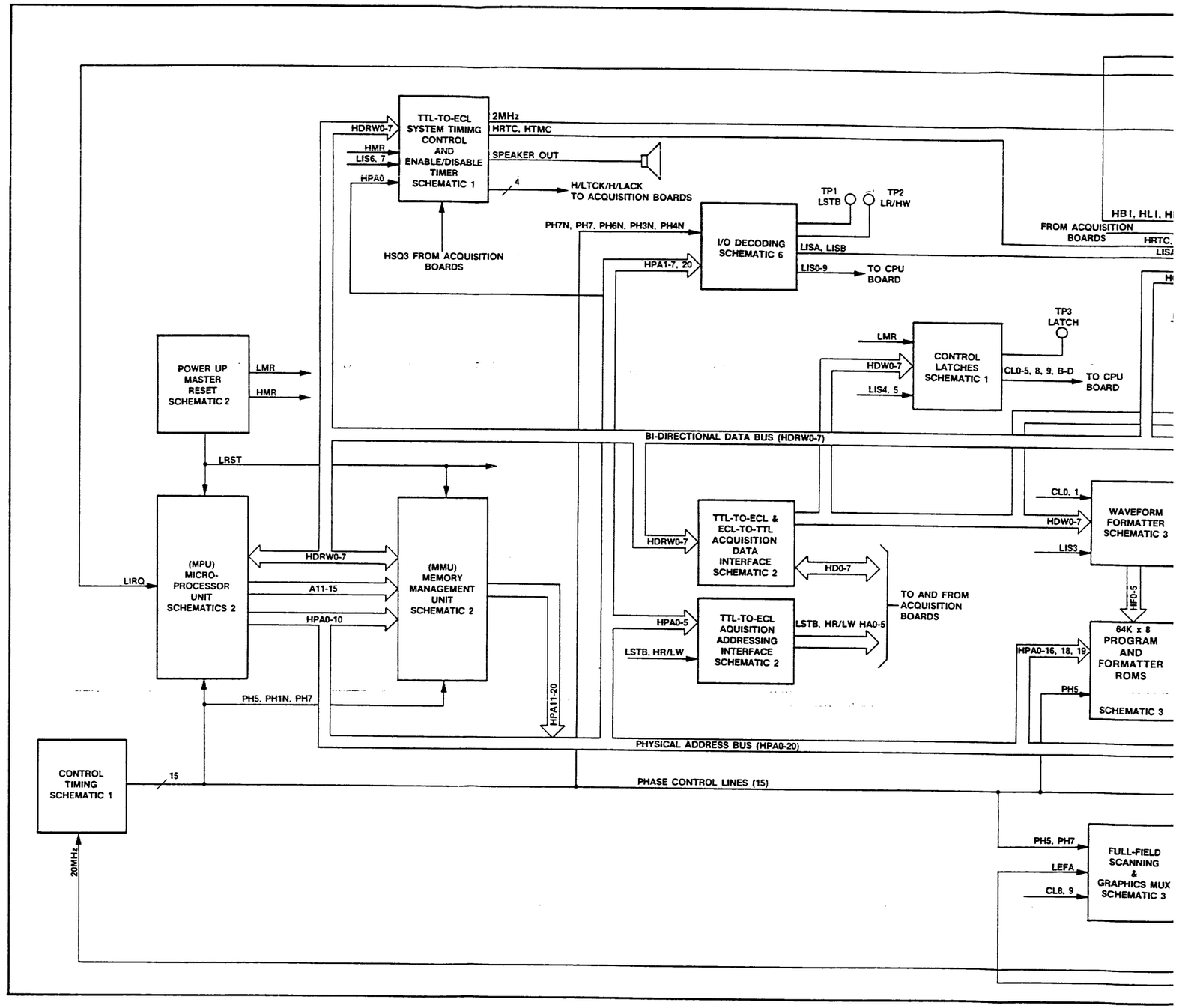
HP-IL. The Hewlett-Packard Interface Loop is used as a low speed form of communication between separate systems. Whether the logic analyzer is HP-IL controlled or not is determined by the settings of the system status switches.

PROBE REFERENCE VOLTAGE ADJUST. User data can be sampled at voltage levels ranging from plus to minus 9.9 volts. This block adjusts the comparator switching point (threshold) of each probe hybrid chip so that data is sampled at the specified voltage threshold. The return ground sense lines adjust the threshold level so that data is sampled with respect to the ground level of the user's system. The processor adjusts the probe reference voltages via the keyboard controller.

KEYBOARD CONTROLLER. Scanning the keyboard and controlling probe reference voltage adjustments is the function of this block. The keyboard controller scans each row and column of the keyboard for a closed switch. When a closed switch is found the processor is sent an interrupt request.

KEYBOARD SWITCH PAD. The keyboard is a switch pad consisting of 38 keys, or switches, wired in a 6 x 8 row/column matrix.

NOTES


TTL-TO-ECL SYSTEM TIMIMG CONTROL AND ENABLE/DISABLE TIMER SCHEMATIC 1
HDRW0-7
HMR
LIS6, 7
HPA0
2MHz
HRTC, HTMC
SPEAKER OUT
H/LTCK/H/LACK TO ACQUISITION BOARDS
HSQ3 FROM ACQUISITION BOARDS
TP1 LSTB
TP2 LR/HW
PH7N, PH7, PH6N, PH3N, PH4N
I/O DECODING SCHEMATIC 6
LISA, LISB
LIS0-9
TO CPU BOARD
HPA1-7, 20
HB1, HL1, H
FROM ACQUISITION BOARDS
HRTC,
LISA
TP3 LATCH
LMR
HDW0-7
LIS4, 5
CONTROL LATCHES SCHEMATIC 1
CL0-5, 8, 9, B-D
TO CPU BOARD
POWER UP MASTER RESET SCHEMATIC 2
LMR
HMR
LRST
BI-DIRECTIONAL DATA BUS (HDRW0-7)
CL0, 1
WAVEFORM FORMATTER SCHEMATIC 3
HDW0-7
LIS3
HF0-5
HDRW0-7
TTL-TO-ECL & ECL-TO-TTL ACQUISITION DATA INTERFACE SCHEMATIC 2
HD0-7
TO AND FROM ACQUISITION BOARDS
HPA0-5
LSTB, HR/LW HA0-5
LSTB, HR/LW
TTL-TO-ECL AQUISITION ADDRESSING INTERFACE SCHEMATIC 2
64K x 8 PROGRAM AND FORMATTER ROMS
HPA0-16, 18, 19
PH5
SCHEMATIC 3
LIRQ
(MPU) MICRO-PROCESSOR UNIT SCHEMATICS 2
HDRW0-7
A11-15
HPA0-10
(MMU) MEMORY MANAGEMENT UNIT SCHEMATIC 2
HPA11-20
PH5, PH1N, PH7
PHYSICAL ADDRESS BUS (HPA0-20)
CONTROL TIMING SCHEMATIC 1
15
PHASE CONTROL LINES (15)
20MHz
PH5, PH7
LEFA
CL8, 9
FULL-FIELD SCANNING & GRAPHICS MUX SCHEMATIC 3

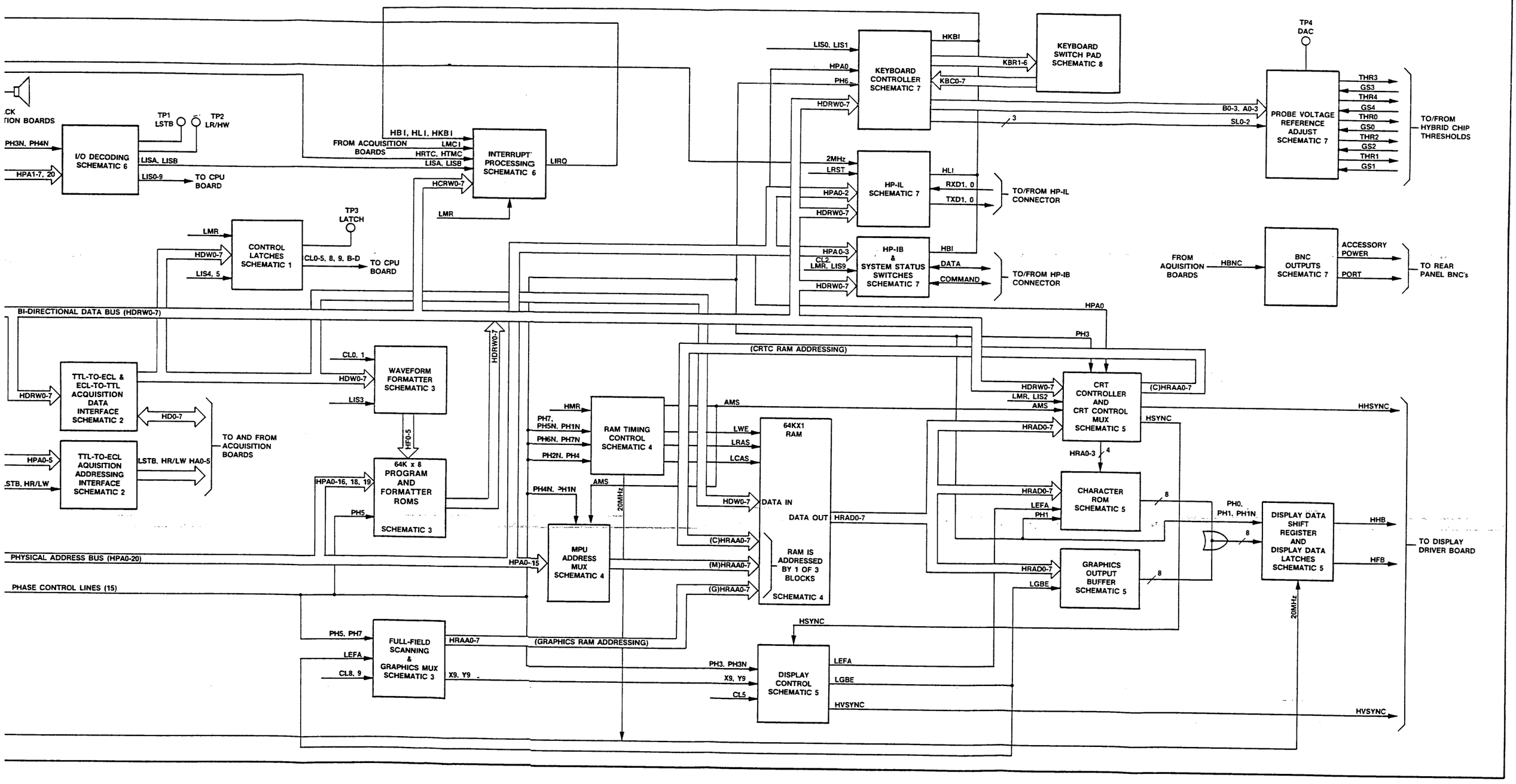


Figure 8B-1. CPU Block Diagram

NOTES

8B-3. THEORY OF OPERATION

The Theory of Operation for this Service Group pertains to the CPU, which includes the interfacing of the keyboard and Display System to the CPU. Refer to the schematic referenced by the secondary heading while reading the Theory of Operation. The theory will begin with the circuitry drawn on the first CPU schematic and continue contiguously to the last.

8B-4. Control Timing (see schematic 8B-1)

The circuit configuration of U7F and U8F is that of an 8-bit twisted-ring shift register. This circuit operates as follows: eight ones and then eight zeros are shifted through the register by a 20 MHz clock. The Q output of each phase is the input for the next phase, thus the output of PH0 is the input of PH1, PH1's output feeds PH2....and PH7N's output feeds back to the PH0 input. Each phase and it's complement are used to control various operations on the CPU board. The frequency of each phase is 1.27 MHz and the delay between adjacent phases is 50 nS. U2D forces this circuit to power up in a twisted-ring configuration.

8B-5. System Timing Controller (see schematic 8B-1)

U6M, a System Timing Controller (STC) chip, is a programmable timer that is configured in the 8-bit mode for reading and writing with the processor. The STC provides the logic analyzer with a 2 MHz clock for HP-IL, interrupt for a real-time clock, a timing measurement clock for the timing board, and a signal source for the piezoelectric speaker LS1.

UY6Q is an external 4 MHz TTL oscillator that drives the STC. FOUT is a continuous 2 MHz clock used by the HP-IL chip. OUT1 is a 20 mS variable width pulse (HRTC) that the processor synchronizes on for the real-time clock display.

The enable/disable timer circuit provides the time count from the first enable to the first disable of a measurement. An interrupt to the processor is generated at the time of the first disable. The time reference is a 32-bit binary counter clocked at 4 MHz by UY6Q.

The operation of the enable/disable timer circuit occurs as follows: Prior to a timing measurement, HSQ3 and LIS8 are low making the G2 and G2A inputs of U6M high. This in turn disables U6M, allowing the MPU to configure U6M and enable the control latch output CL3 of U6P. When the processor is ready, HSQ3 and LIS8 are pulled high making G2 and G2A of U6M low enabling the STC output OUT4 to be ON for the desired measurement time. When a measurement is complete, HSQ3 and LIS8 are pulled low disabling U6M. Then HTMC, an interrupt request, is sent to the processor via the interrupt processing circuit to indicate a measurement was completed. The processor will then interrogate the STC to determine the time it took for a measurement.

U7M is a TTL-to-ECL translator and U9M is an ECL NOR gate. Note, all of the parts on the acquisition boards are high speed emitter-coupled logic (ECL) parts.

8B-6. Control Latches (see schematic 8B-1)

The processor loads control information into U6P and/or U6O with data from the HDW0-7 bus and clocks the desired part via LIS4 and/or LIS5. The resultant outputs are then used to control various system functions. Each control latch bit assignment is given in table 8B-1.

Table 8B-1. Control Latch Bit Assignments

Data Bit	Bit Name	Logic Level	Function
HDW0	CL0 U6P	L	Enables MPU to address ROM 0 instead of W Formatter.
HDW1	CL1 U6P	H	Enables W Formatter to address ROM 0 instead of MPU.
HDW2	CL2 U6P	H	Allows the logic analyzer to be an HP-IB controller.
HDW3	CL3 U6P	H	Enables MPU to drive low speed timing sample clock.
HDW4	CL4 U6P	H	Not Used
HDW5	CL5 U6P	H	Enables graphics display area.
HDW6	CL6 U6P	X	Spare
HDW7	CL7 U6P	X	Spare
HDW0	CL8 U60	*	Graphics Page LSB
HDW1	CL9 U60	*	Graphics Page MSB
HDW2	CLA U60	X	Spare
HDW3	CLB U60	H	Enables HVSYNC (Delays HVSYNC until CRTC is loaded)
HDW4	CLC U60	**	CRT controller (CRTC) page LSB
HDW5	CLD U60	**	CRT controller (CRTC) page MSB
HDW6	CLE U60	X	Spare
HDW7	CLF U60	H/L	Used for signature analysis LATCH test point.

* or ** - The combination of these two lines determine which 16K byte segment of 64K bytes of RAM is displayed.

MSB	LSB	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

8B-7. Microprocessing Circuitry (see schematic 8B-2)

The processor used by the logic analyzer is a MC68B09E microprocessor unit (MPU). The MPU is an 8-bit processor capable of addressing 64K bytes of memory. However, along with the MC68B29 Memory Management Unit (MMU), another 64K bytes of memory is addressable. Table 8B-2 is the Physical Address-to-Function Allocation (memory map).

8B-8. MPU OPERATION. The MPU U6I communicates and controls the system via an 8-bit bi-directional data bus HDRW0-7. The processor addresses the system via 16 output lines. The first 8 address lines (A0-7) are latched by U6J to provide hold considerations and buffering for these lines. The next 3 lines (A8-10) are buffered by P/O U5J. The remaining 5 address lines from U6J are then used as the 7 register select lines (RS0-6) for the MMU U6L. HPA7-10 are also used to address ROM, RAM, and I/O.

The clock inputs to the MPU are Q and E. The 1.27 MHz quadrature clock Q leads the E clock by approximately 200 nS. These clocks are also used by the MMU for synchronization.

The read/write output indicates the direction in which data is being transferred on the HDRW0-7 data bus. When this line is high, data is being read on the bus. When the read/write output is low, the MPU is writing to the bus.

Table 8B-2. Physical Address-to-Function Allocation

Physical Address	Function
000000H 05FFFFH	Not Used
060000H 07FFFFH	I/O
080000H 11FFFFH	Not Used
120000H 13FFFFH	ROM
140000H 15FFFFH	RAM
160000H 1FF7FFH	Not Used
1FF800H 1FFEFFH	ROM
1FFF00H 1FFF7FH	MMU
1FFF80H 1FFFFFH	ROM

The Bus Available (BA) and Bus Status (BS) outputs from the MPU provide the MMU with information about the class of bus operation for each cycle. The following is the MPU state truth table for the BA, BS outputs:

BA	BS	Definition of MPU States
0	0	Normal Running Mode
0	1	Interrupt Acknowledge (LRST or LIRQ)
1	0	SYNC Acknowledge
1	1	HALT or Bus Grant

The NMI, FIRQ, and HALT interrupt inputs to the processor are not used. However, the Interrupt Request line (LIRQ) to the processor is. When an interrupt is detected in the interrupt mask circuitry, the LIRQ line is pulled low. With LIRQ low, the processor then initiates an interrupt sequence, provided the condition code register mask bit (I) is clear.

The LRST input to the processor, when asserted low, will RESET the processor until the LRST line is high. Note, the processor will execute the present bus cycle before going to a RESET state.

8B-9. MMU OPERATION. The Memory Management Unit (MMU) U6L is used to expand the 64K byte addressable space of the processor. Expansion is done by applying the upper five address lines from the processor (A11- 15), along with the contents of a 5-bit task register, to an internal mapping RAM. The MMU outputs ten Physical Address lines (PA11-20) which are combined with HPA0-10 from the processor to form the address bus HPA0-20.

The bi-directional data bus HDRW0-7 is used when the MMU registers are written to or read from. The register and byte of information to be selected is determined by RS0-6. Furthermore, the location of the MMU registers is determined by a low on the Register Access (RA) line, providing the current task number is zero and A11-15 are all ones.

Clocking and resetting of the MMU is synchronous with the processor via the E, Q, and reset inputs. Also, the processor determines read/write status of the MMU via the Low Write/High Read (LW/HR) input.

8B-10. Power-Up Master Reset (see schematic 8B-2)

The purpose of this circuit is to keep some key circuitry on the CPU board OFF while the power supply is turning ON. Upon power up U7P pin 5 is at essentially zero volts and charging through R17,19 and C26, whereas U7P pin 4 is at or near 4.55 volts. This keeps U7P pin 2 and 1 low, holding the reset mode ON. When U7P pin 5 exceeds 4.75 volts, pin 2 will go high, charging C35 for 10 mS. As the voltage on U7P pin 7 exceeds the voltage on pin 6, pin 1 will go high thus removing the reset mode.

The Low Reset line (LRST) is for MOS devices requiring a higher set voltage. The High/Low Master Reset (HMR, LMR) lines are used for other devices requiring a certain reset level. Note that all clocks are turned OFF until the reset mode is removed.

8B-11. Acquisition Interface (see schematic 8B-2)

8B-12. ACQUISITION ADDRESSING. U9I and U9J are TTL-to-ECL translators that convert the HPA0-5, LSTB and HR/LW signals to ECL logic levels. This allows the processor to address and control circuitry on the ECL acquisition boards.

8B-13. ACQUISITION DATA. The processor communicates with the acquisition system via a bi-directional data bus HD0-7. A data read occurs when: there is a high on the High Read/Low Write line (HR/LW), a Low Strobe (LSTB) occurs, and the Enable Data Transfer line (ENDT) is asserted low. With these qualifications met, converted data (ECL-to-TTL) from U8K and U9K, seen at the inputs to U7K, is then read onto the bi-directional data bus HDRW0-7. The processor will do a data write when: there is a low on the HR/LW line, LSTB is asserted, and ENDT is low. Write data is then seen on the outputs of U7L (HDW0-7). This information is then converted to ECL levels by U8L and U9L and used on the acquisition boards. See figure 8B-2 and 8B-3 for the timing waveforms between the acquisition system and the MPU during read/write operations.

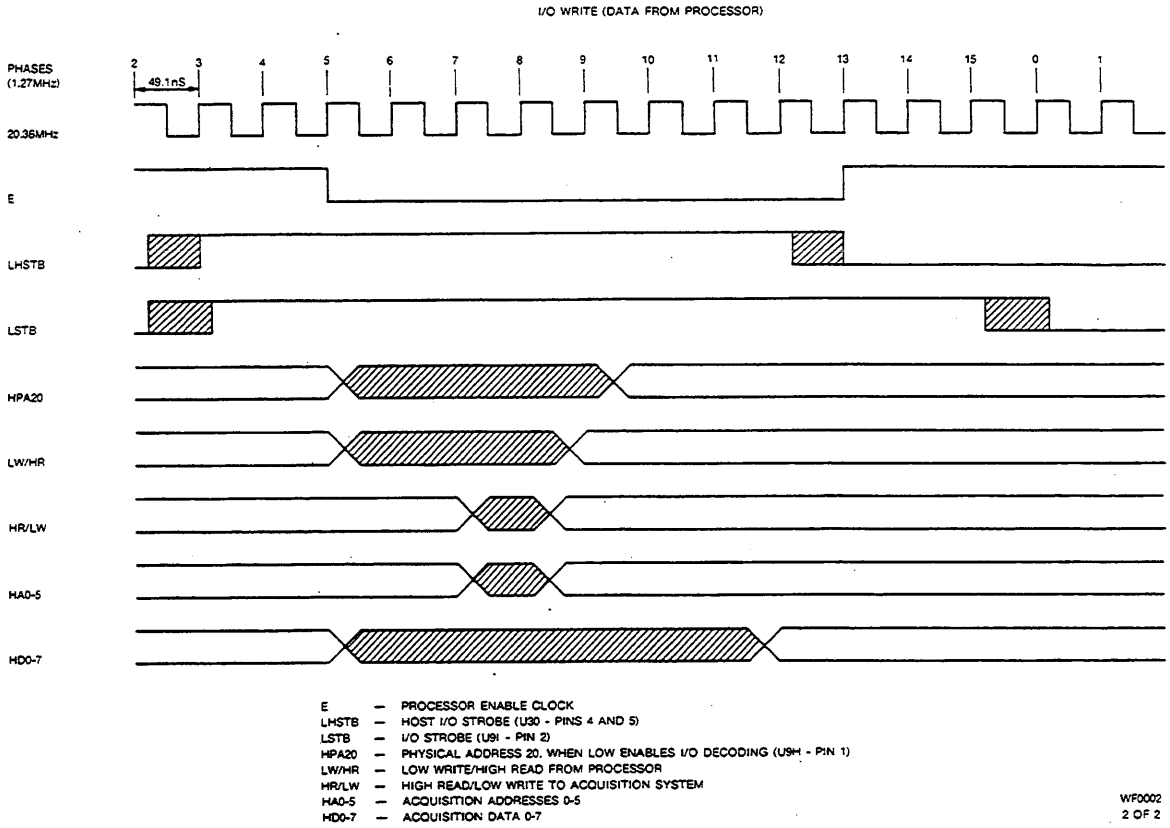


Figure 8B-2. Acquisition Write Timing Waveforms

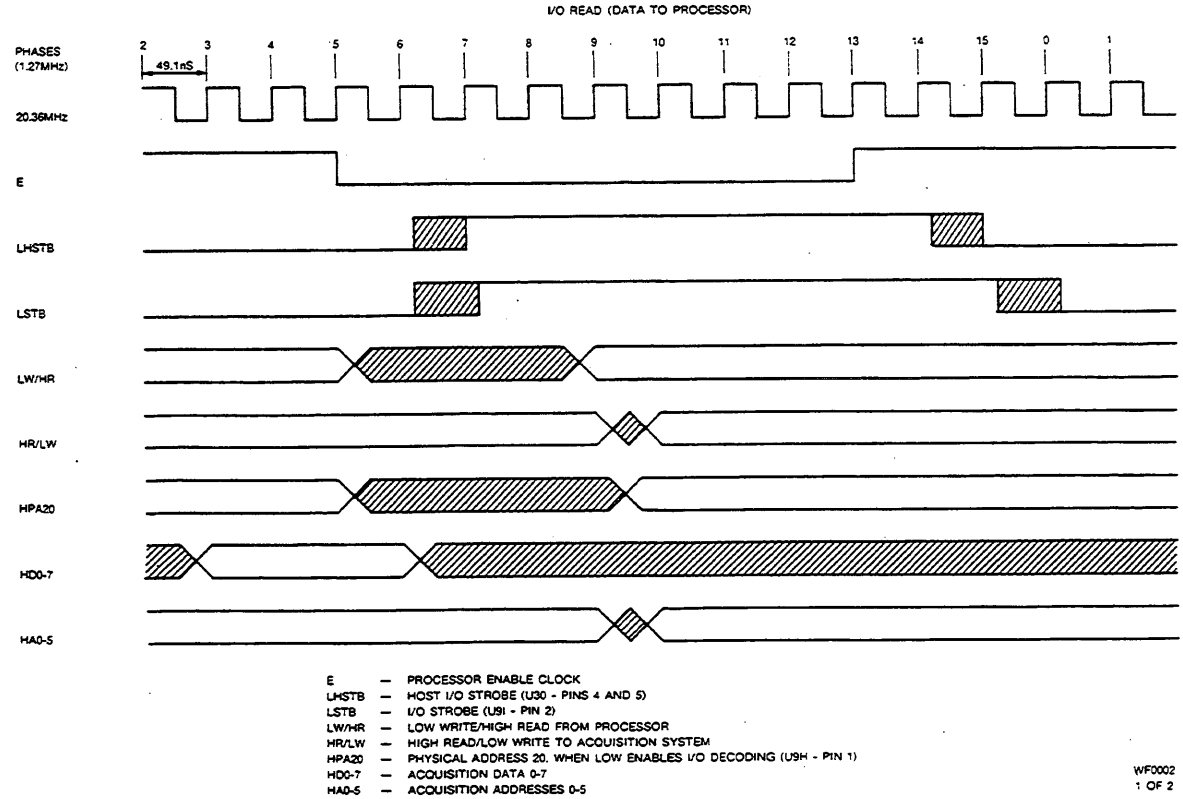


Figure 8B-3. Acquisition Read Timing Waveforms

8B-14. Full-field Scanning Generation and Graphics MUX (see schematic 8B-3)

The full-field scanning generator provides scanning information necessary to display graphics in the 16K bit graphics area shown in figure 8B-4. Display timing waveforms are given in figure 8B-5.

8B-15. SCANNING. Scanning of the full-field graphics display area is done by five binary counters (U3F-A,B, U4F-A,B, and U4G) cascaded together in a ripple carry configuration. U3F is the high speed Y counter that provides the vertical sweep speed and character frequency of 1.27 MHz (PH5), whereas U4F and U4G form the slow speed X counter producing a horizontal frame frequency of 60 Hz.

Y counter U3F is cleared by HCY (the decoded display enable (DE) output of the CRT controller) at the end of a line (every 27.5 uS). The Y8 output, pin 11 of U3F-B, indicates the end of a line and is also used to clock U7A-A.

The X counter U4F is cleared by HCX at the end of a frame, as indicated by the X9 output from U4G. The load X counter (LLX) input to U4G is used to load 07 hex into the counter while low, and count from 07 hex when high. The LLX line is the complement of the high clear X counter (HCX) line.

8B-16. GRAPHICS MUX. The multiplexers, U6F and U5F, are used to generate RAM addresses while in the graphics mode and provide RAM refresh during retrace. These devices are enabled by a low level on the low enable full-field display line (LEFD). The input that is selected is determined by the logic level of the address MUX select line (AMS).

The CL9 and CL8 inputs to U6F determine which 16K byte segment of 64K bytes of RAM is displayed as shown below:

CL8	CL9	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

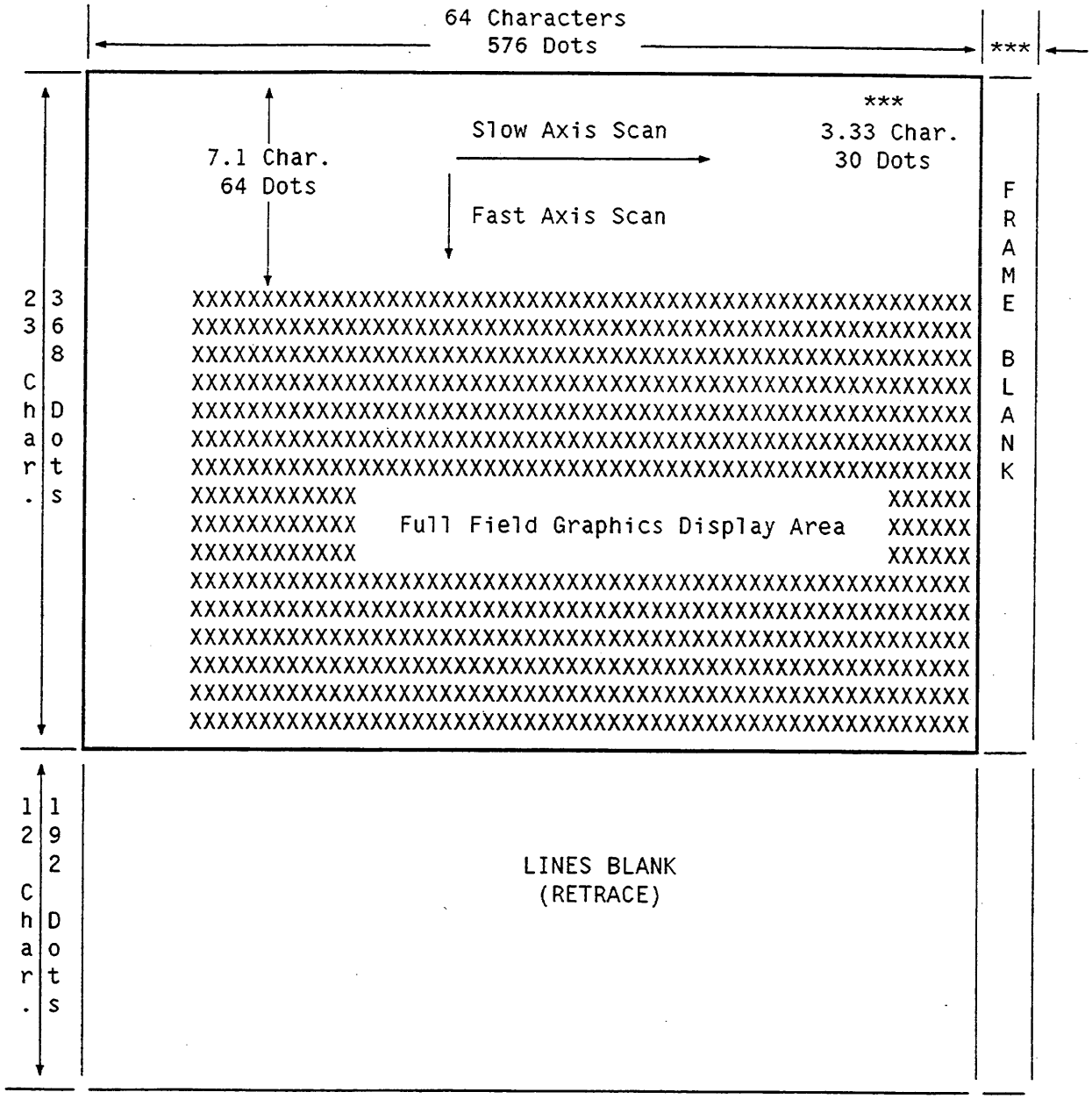
8B-17. Waveform Formatter (see schematic 8B-3)

Basically, the Waveform Formatter (Formatter) is responsible for taking state and/or timing waveform information from the acquisition system and generating waveform display symbols. The hardware portion of the Formatter generates addresses that are referenced to fourteen, 256-byte look-up tables in the Formatter ROM. The Formatter ROM then outputs the proper waveform display symbol either a high or low level, an edge, or a glitch. The Formatter is used to increase the waveform display update rate.

When a waveform display is requested by the user, the processor clocks acquisition data stored in RAM into data latches U5D, U5P and U5Q. The processor then enables multiplexers U4O, U4P, and U4Q with control latch line CL1; at the same time disabling U3N (via CL0) allowing the Waveform Formatter to address the Formatter ROM, U3K. Then, according to: the users choice of magnification (X1, X2, or X>2); number of channels to be processed; glitch or no glitch; the processor will address a look-up table stored in U3K, and set the multiplexers to mask out the non-effective bits. The look-up table chosen then samples the data from the Waveform Formatter (HF0-5 and HPA0,1), and generates the proper waveform display symbols. The processor then puts this display information into RAM where it is later routed through the graphics buffer, U6AZ, and shifted out of the display data shift register, U6B, to the display.

8B-18. ROM and ROM Selection (see schematic 8B-3)

U4N, a 1 of 8 addressable demultiplexer, is used to enable one of eight 8K word x 8-bit program ROMs for addressing. U7I and U8D determine if U4N is selected and the combination of HPA13-15 select which ROM is enabled.



Dot Rate:	20.36 MHz
Dot Time:	49.1 ns
Character Rate:	1.27 MHz
Character Time:	785.8 ns
Line Rate:	36.36 KHz
Line Time:	27.503 us
Line Blank Time:	9.43 us
Frame Rate:	60.0 Hz
Frame Blank Time:	825 us

For more information see table 8B-6.

Figure 8B-4. Display Character Area

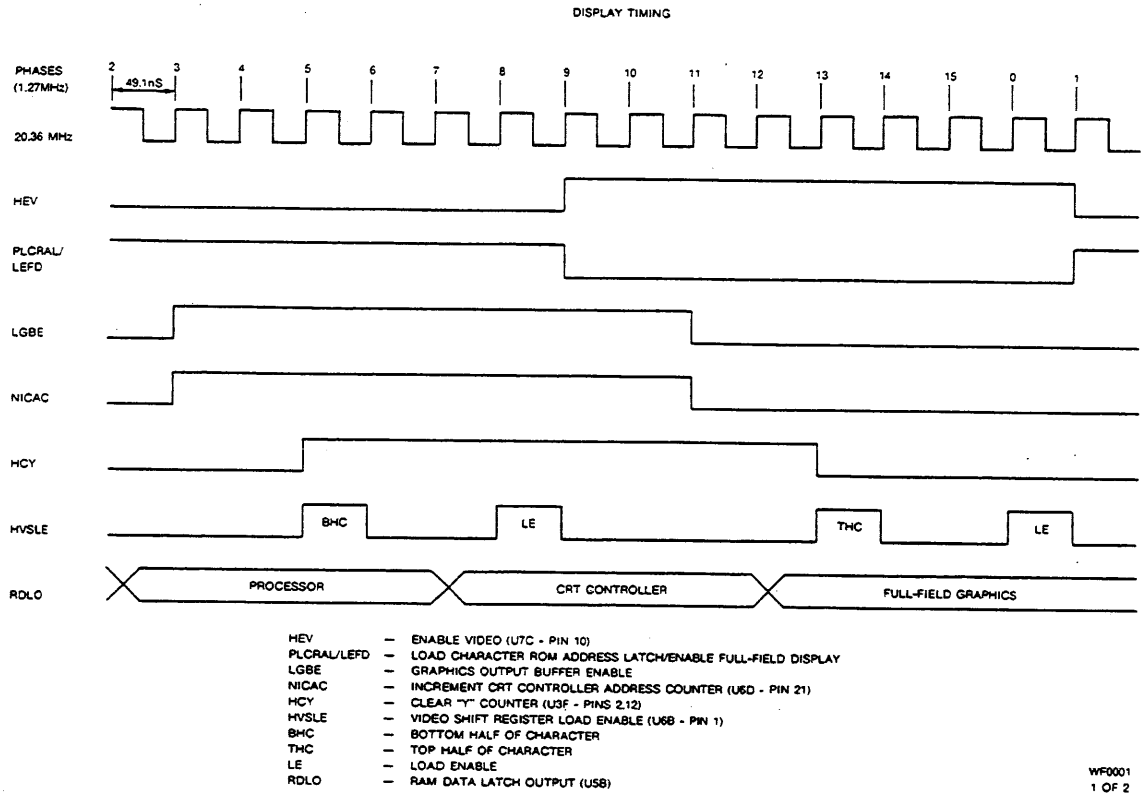


Figure 8B-5. Display Timing Waveform For One MPU Cycle

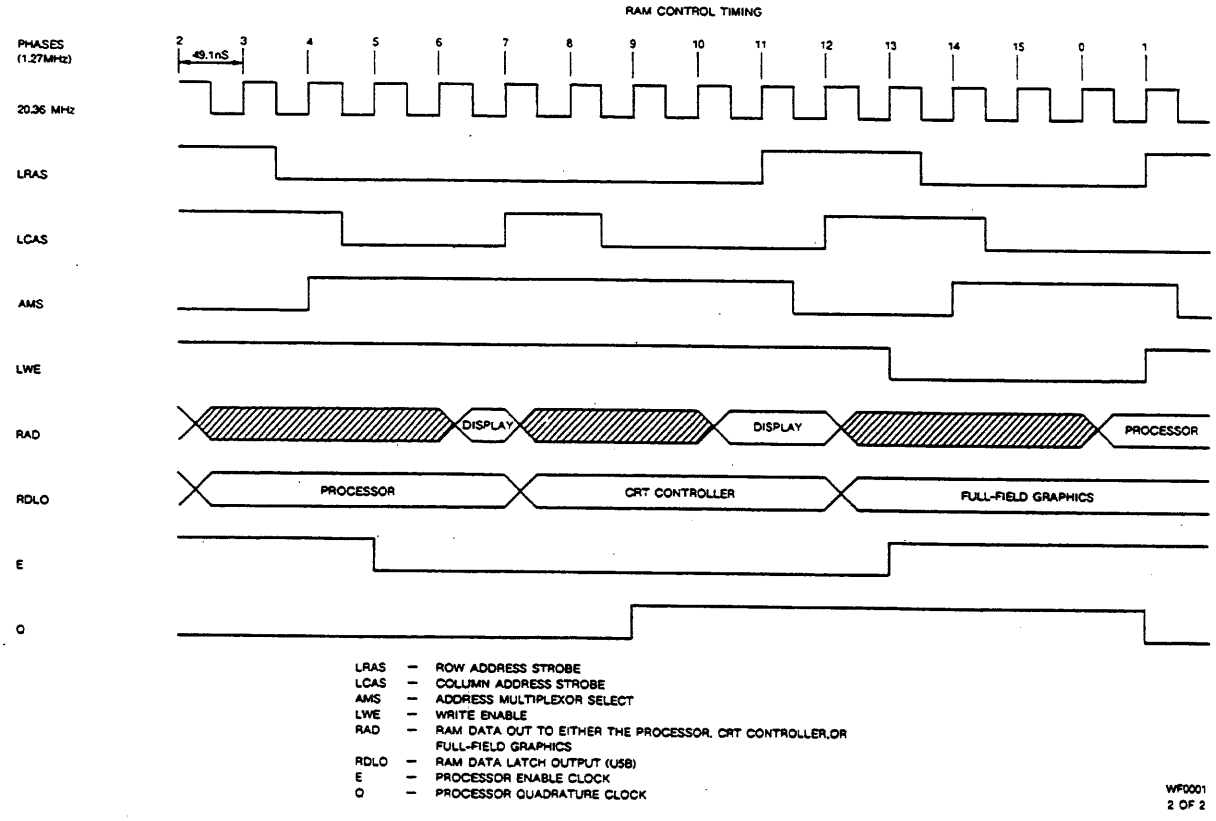


Figure 8B-6. RAM Timing Waveforms For One MPU Cycle

8B-19. RAM Timing Control and RAMs (see schematic 8B-4)

8B-20. RAM TIMING CONTROL. This circuitry is responsible for creating the R and Column Address Strobes (RAS and CAS) needed for RAM data transfers. LRAS and LCAS, generated by the gating action of U2E, U2C, U2B, and U2A, are needed during read, write, and page mode read cycles of RAM. Figure 8B-6 shows the timing relationships of these signals.

The Address Multiplexer Select (AMS) signal lags LRAS by 25 nS and is used to enable the right group of RAM address multiplexers (MPU, graphics or CRTC) at the proper time during a processor cycle time. The 20 MHz output of U2A, used to clock the control timing circuit and U2C, is half the frequency of the master clock UY1D.

8B-21. RAM. The CPU board uses eight 64K word x 1 bit dynamic RAMs. The RAMs require three external control signals LRAS, LCAS and LWE in order to insure proper data transfers. RAM is controlled by three different cycles; read, write, and page mode read. Note, the page mode read pulse is embedded in the LCAS waveform and is used while in the graphics mode when two page reads from RAM are needed. The LWE signal controls read/write operations. See figure 8B-6 for these timing waveform relationships.

Outputting data from RAM occurs as follows: When LCAS is high, the data-out lines from the RAM go to the high impedance state. Note that as LCAS goes high, RAM data latch U5B outputs previously stored data. When LCAS is low the inputs to U5B will be OFF and data will be output from RAM.

RAM refresh is done during a memory cycle at each of the 128 contiguous row addresses within a 2 mS time interval.

8B-22. CRT Control (see schematic 8B-5)

This system uses the vertical scanning method to display information. With this type of scanning, the electron beam scans from top to bottom and from left to right. After each vertical scan the beam is moved horizontally to display another 23 characters. The non-interlace mode is the type of raster scanning used. This means that one field per frame is scanned before the electron beam is returned to the top left hand corner of the display.

For resolution the characters generated on a frame must be continually repeated in order to display them on the CRT. The character code stored in ROM and loaded into RAM is in ASCII and must be converted for use on the CRT. Since ASCII characters cannot be directly displayed, a character ROM (U6C) is used to convert the ASCII codes into the 9 x 16 dot pattern used to generate characters. See figure 8B-7 for a typical dot pattern for a character.

8B-23. CRT Controller (CRTC) Operation (see schematic 8B-5)

The CRTC is the interface between the MPU and the display system. The CRTC U6C contains nineteen programmable registers. These registers are initialized by the processor via the HDRW0-7 data bus. The MPU configures the CRTC to generate horizontal and vertical sync, raster addresses for the character ROM, a display enable signal, and a cursor asserted signal. However, there are several control inputs whose signals contribute to the initialization process. These are described in the following paragraphs.

8B-24. CRTC INTERFACING. The bi-directional data bus D0-7 is used for data transfers between the MPU and one of the internal registers of the CRTC. The high read/low write (HR/LW) line is used to determine whether a register is written to or read from. The register selected is determined by the state of HPA0 that is tied to the register select (RS) line. When HPA0 is low the address register is selected. When HPA0 is high, one of the data registers can be accessed. The enable (E) input is used to clock data to and from the data input/output buffers. The processor controls the E input with LIS2 which is the read/write CRTC line.

The clock (CLK) input is used mainly to synchronize the horizontal sync registers. The clock rate input is equal to the character rate of 1.27 MHz.

The low master reset (LMR) line is tied to the reset input of the CRTC. When a low level is on this line, the CRTC is forced into the following state:

a. The display operation stops and all CRTC counters are cleared.
b. All outputs go low.
c. The control registers remain unchanged and unaffected.

8B-25. HORIZONTAL AND VERTICAL SYNC. The sync signals are generated by the CRTC timing registers. The horizontal registers are programmed in character time (785.79 nS) units with respect to the left-most displayed character. Note that the horizontal sync (HSYNC) signal from the CRTC is NANDed with the control latch bit B (CLB) signals. CLB will go high when the processor is finished initializing the CRTC. The HSYNC signal then becomes the vertical sync (HVSYNC) for the display driver board. The CRT's vertical sync timing registers are programmed in character line time (27.5 uS) and are referenced to the top character position. Note that the vertical sync (VSYNC) signal from the CRTC becomes the horizontal sync (HHSYNC) signal for the display driver board.

8B-26. DISPLAY ENABLE AND CURSOR OUTPUTS. Display enable (DE) is an active high output that indicates that addressing in the active display area is being provided by the CRTC. The cursor (CUR) output signal is determined by the initialization of the CRTC cursor registers. CUR is an active high signal that is exclusive-ORed with HRAD7 to provide inverse/non-inverse display blinking on a character.

8B-27. RAM ADDRESSING. The 14 memory addresses, MA0-13, from the CRTC are multiplexed together by U6E and U5E and used to address a 16K byte segment of dynamic RAM. The combination of the CLD and CLC inputs to U6E determine which 16K byte segment of RAM is available to the CRTC.

CLD	CLC	kilo byte segment
0	0	0-16
0	1	16-32
1	0	32-48
1	1	48-64

8B-28. RASTER ADDRESSES. The CRTC provides 4 outputs, RA0-3, to be used by the character ROM U6C as the column address (1 of 9) for a character. In other words, RA0-3 position the Character ROM so that the correct character dots are displayed in the correct location on the raster.

8B-29. CHARACTER GENERATION (see schematic 8B-5).

The circuitry responsible for the final processing of a character is the Character ROM, graphics output buffer, the display data shift register, display control circuitry, and the display data latches.

8B-30. CHARACTER ROM. The 121-bit Character ROM address consists of a 7-bit binary ASCII code (HCRA 0-6) that represents a standard symbol, i.e., a letter, number, or a symbol. Also, a column address (HRA0-3) that corresponds to the dot column that is to be output, and a timing qualifier, PH1. When character ROM U6C is enabled by LRE and the low output of U8D pin 6, the proper 8 dot segment for a given character is output to the display data shift register. A dot represents one logical bit.

The dot matrix size for each character is 9 dots wide by 16 dots high. The following is an example of how a single character is displayed on the CRT. Note that there are 23 characters to a character column on the raster (refer to figure 8B-4). The output dot sequence for a character is in 8 dot segments from top to bottom, left to right. The character ROM outputs the first 8 bits to the shift register U6B.

When U6B serializes these, another 8 bits is loaded. Then the character ROM is given a new dot column address and the dot output routine is repeated. This is done 9 times for each character. Thus, the 9 x 16 character dot pattern. Note that a high from U6C is equal to a dot being on. See figure 8B-7 for a typical dot pattern.

8B-31. DISPLAY DATA SHIFT REGISTER. This device is responsible for converting parallel display information into a serial data stream. U6B can be configured for either shift left or parallel loading operations. This is determined by the level on pin 1.

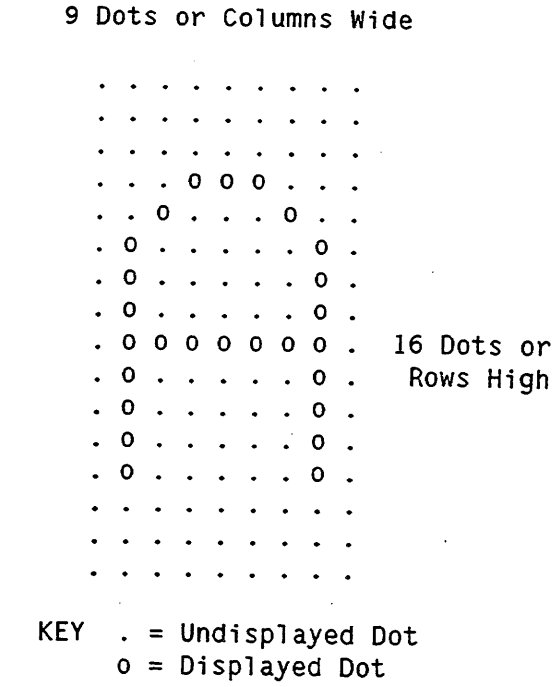


Figure 8B-7. A Typical 9 x 16 Dot Pattern for a Character.

8B-32. GRAPHICS OUTPUT BUFFER. While in the graphics mode the Character ROM is disabled and U6A is enabled. Graphics information is then loaded into U6B and displayed in the full-field graphics display area.

8B-33. DISPLAY DATA LATCHES. The display data latches U8C-A,B provide the video data to the display driver board. These latches are clocked at 20 MHz making a 50 nS dot rate, whereas the combination of the outputs of U7B-A,B determine the brilliance of the video displayed. The following is the output of U8C-A,B which is the truth table for video information.

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

8B-34. DISPLAY CONTROL. This circuitry is responsible for controlling display operations. For instance, the outputs of U7A and U9D-B control which device group access RAM and which devices are ON or OFF during a fast axis retrace. U7C provides timing for the cursor and enables the video brightness circuitry, U7B-A,B. Also, this circuitry enables and disables the character ROM, full-field scanning generator, and graphics buffer during the proper time in a processor cycle.

8B-35. I/O Decoding (see schematic 8B-6)

The Input/Output decoding circuitry is separated into two levels of decoding; macro and micro. I/O operations are enabled by a low level on the HPA20 address line from the MMU. Each level of decoding is outlined in the following.

8B-36. MACRO I/O DECODING. Macro decoder U30 is a 1 of 8 addressable demultiplexer. U3O is used to select, or enable, an I/O device that requires more than 2 Physical Addresses to perform a specific I/O function, i.e., read or write operations. Macro I/O is memory mapped into a 256 word space as shown in table 8B-3. Each macro I/O function, when selected by U3O, is given 32 words of ROM space. However, the acquisition system is given a total of 64 words, two outputs from U3O which are ORed together by U7I-A to form Low Strobe (LSTB).

Table 8B-3. Macro I/O Physical Address-to-Function

Physical Address	I/O Function	Strobe Mnemonic
06XX00H	Acquisition Sys.	LSTB
06XX40H	Micro I/O	
06XX60H	HP-IL Write	LHLW
06XX80H	HP-IL Write	LHLR
06XXA0H	HP-IB	LHBS
06XXC0H	Spare	
06XXE0H	Not used	LSS

8B-37. MICRO I/O DECODING. Micro decoders U5N and U6N are 1 of 8 addressable demultiplexers. U5N and U6N are used to select, or enable, an I/O operation and/or device that requires 2 Physical Addresses or less to perform an I/O operation. The I/O strobe line to function is given in table 8B-4.

Table 8B-4. Micro I/O Physical Address-to-Function

Physical Address	I/O Function	Strobe Mnemonic
06XX40H	Keyboard Read Data	LIS0
06XX41H	Keyboard Read Status	LIS0
06XX42H	Keyboard Write Data	LIS1
06XX43H	Keyboard Write Status	LIS1
06XX44H	Read/Write CRTC	LIS2
06XX46H	Write Formatter	LIS3
06XX48H	Write Control Latch U6P	LIS4
06XX4AH	Write Control Latch U6O	LIS5
06XX4CH	Read Counter U6M	LIS6
06XX4EH	Write Counter U6M	LIS7
06XX50H	Reset Enable/Disable Timer FF	LIS8
06XX52H	Read HP-IB Address	LIS9
06XX54H	Read Interrupt Status	LISA
06XX56H	Write Interrupt Mask	LISB
06XX58H	Spare	LISC
06XX5AH	Spare	LISD
06XX5CH	Spare	LISE
06XX5EH	Spare	LISF

8B-38. Interrupt Processing (see schematic 8B-6)

When an interrupt is generated by a device, a high will be sensed at the inputs to the interrupt mask and the read interrupt status buffer U1M. The interrupting device(s) is determined by the output of U1M. Each interrupt is given a specific firmware priority so that if two interrupts occur simultaneously, one will be serviced before the other. Interrupt priority is done by masking out the lower priority interrupts with a zero, from U1L, on the other input of their respective interrupt mask NAND gate. The highest priority interrupt is given a one (thus, making the low interrupt request (LIRQ) line low to the processor). The processor will then service the interrupt, clear the device's interrupt request line, read the interrupt status buffer, and change the interrupt mask to sample the next highest priority interrupt.

8B-39. HP-Interface Bus (HP-IB) Circuitry (see schematic 8B-7)

The Hewlett-Packard Interface Bus transfers data and commands between systems via 16 signal lines. The interface functions for each system component are performed within the component so only passive cabling is needed to connect systems. The cables connect all instruments, controllers, and other components of the system in parallel. The following is a description of the inputs to the HP-IB controller, and the outputs as they relate to interface operations.

8B-40. MPU TO HP-IB INTERFACE. HP-IB controller U2G communicates via thirteen memory mapped registers. Six of the registers are read from, and seven are written to. The registers are used to pass control data to, and status information from, a system component. HPA2-0, connected to the register select (RS2-0) lines, are used to select a particular register. A low on the chip enable line (CE) indicates that the processor is doing either a read or write from the selected register. Note that each combination of RS2-0 can indicate one of two different registers depending on whether a read or write operation is occurring. For example, a write operation with RS2-0 = 110 indicates a Parallel Poll register access, but a read to the same location indicates a Command Pass Through register access.

Reading or writing to a register is indicated by the level of HPA3. A high indicates an MPU read and the Data Bus In (DBIN) line will be asserted. When low, the Write Enable line (WE) is asserted and the MPU will write to a register. Data transfers are via the bi-directional data lines HDRW0-7 attached to the D0-7 lines of U2G.

8B-41. HP-IB INTERFACE LINES AND OPERATIONS. The eight data I/O lines (DIO1-8) are reserved for the transfer of data and other messages in a byte-serial, bit-parallel manner. Data and message transfer is asynchronous and is coordinated by three handshake lines: Data Valid (DAV), Not Ready For Data (NRFD), and Not Data Accepted (NDAC). The other five lines are for management of bus activity. See figure 8B-8 for HP-IB signal lines.

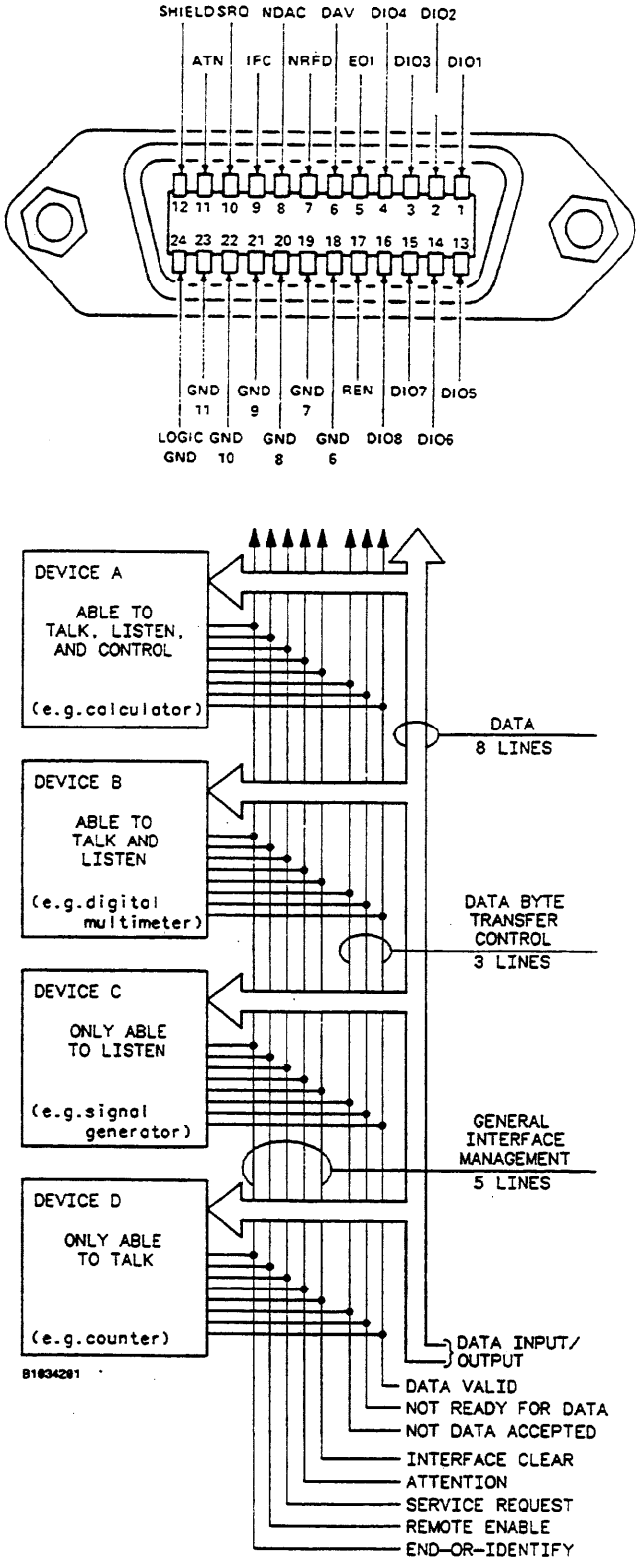


Figure 8B-8. HP-IB Signal Lines

Devices connected to the bus may be talkers, listeners, or controllers. The controlling device dictates the role of each of the other devices on the bus by setting the ATN (attention) line true (low true) and sending talk or listen addresses on the data lines.

The MPU reads the rear panel switches to determine its device bus address and loads this into the HP-IB controller. While the ATN line is true, all devices must listen to the data lines. When the ATN line is false, only devices that have been addressed will actively send or receive data; all others ignore the data lines.

Several listeners can be active simultaneously but only one talker can be active at a time.

Whenever a talk address is put on the data lines (while ATN is true), all other talkers are automatically unaddressed.

Information is transmitted on the data lines under sequential control of the three handshake lines (DAV, NRFD and NDAC). No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices to receive the same message byte concurrently. For HP-IB handshake timing, see figure 8B-9.

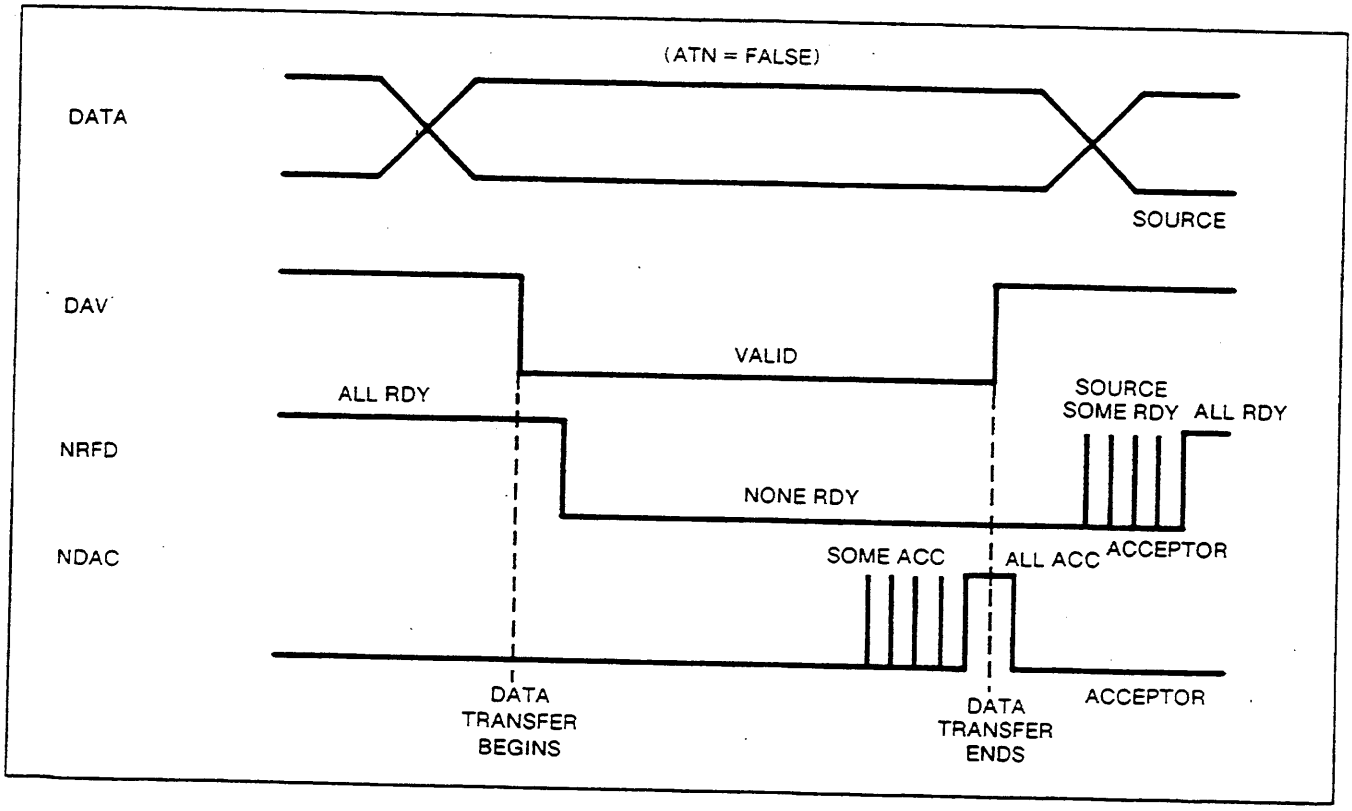


Figure 8B-9. HP-IB Handshake Timing For One Talker And Multiple Listeners

The ATN line is one of the five management lines. When ATN is true, addresses and universal commands are transmitted on only seven of the data lines using ASCII codes. When ATN is false, any code of 8 bits or less understood by both talker and listener(s) may be used. The Interface Clear (IFC) line places the interface system in a known quiescent state via the abort message. The Remote Enable (REN) line is used with the remote, local and clear lockout/set local messages to select either local or remote control of each device. Any active device can set the Service Request (SRQ) line true. This indicates to the

MPU that the device on the bus wants attention. The End Or Identify (EOI) line is used by a device to indicate the end of a multiple-byte transfer sequence. When the controlling device sets both the ATN and EOI lines true, each device capable of a parallel poll indicates its current status on the DIO line assigned to it.

The Interrupt (INT) line indicates an interrupt request when low. This signal is then inverted by U3P-B and routed to the interrupt mask where the MPU branches to a subroutine to service this interrupt.

8B-42. HP-IB TRANSCEIVERS. All of the input/output signals from the HP-IB controller are routed through two octal bus management transceivers U1I, and U1H. These devices are controlled by CONT (controller), TE (talk enable), and CL2 (system controller). U1I controls the direction of command and data transfer signals. The direction of the command signals ATN, SRQ and EOI is determined by the CONT line, but IFC, and REN are directed by CL2. Data transfer signals NRFD, NDAC, and DAV are controlled by TE. The direction of data flow through U1H is determined by ATN or EOI, while TE controls whether U1H is tri-stated or in the open-collector (enabled) mode.

8B-43. System Status Switches (see schematic 8B-7)

SW1, an 8 switch dip package, is mainly used to configure the analyzer on a system bus, i.e., HP-IB and HP-IL. Switch 6 of 8 is used to access a self test (ST) routine for testing some of the functions of the logic analyzer. See Section 3 (Operation) for configuring the analyzer for HP-IB and HP-IL operations and Section 4 (Performance Tests) for initiating ST.

Switches 1 through 5 of 8 are used to select an address on the HP-IB interface bus. The combination of switches 7 and 8 select HP-IB talk only, HP-IB controlled, HP-IL controlled.

During power-on, the processor reads the status of SW1 by enabling U1E via LIS9. Then according to the switch settings the processor will either initiate self test (ST), write the HP-IB address and status into the HP-IB controller, or indicate to the HP-IL controller whether or not it is to be controlled by an outside device.

NOTE

The processor samples the setting of the system status switches ONLY during turn-on. Changing SW1 to "1" after turn-on will not initiate SELF TEST. Cycling the power OFF/ON will reset the switch status. After ST is executed, however, the ST switch may be set to a "0" allowing the System Specification menu to be displayed without cycling power.

8B-44. BNC Outputs (see schematic 8B-7)

The rear panel BNC labeled PORT is used to supply the following seven signals from the acquisition system on a multiplexed basis. The other BNC labeled ACCESSORY POWER provides a regulated + 5 volt power supply for use by a preprocessor option.

Signal to BNC

a. Pulse on State Trace Point
b. High until State Trace Point
c. Low until State Trace Point
d. High on last Sequence
e. Constant High
f. Constant Low
g. High on Timing Pattern

8B-45. HP-Interface Loop (HP-IL) Circuitry (see schematic 8B-7)

8B-46. GENERAL INFORMATION. HP-IL is a bit-serial, uni-directional loop. Information is re-transmitted by each device; each device supplies only enough power to drive the message on to the next device. Also, HP-IL protocol provides for excellent error detection (meaning that commands and data make a complete circuit of the loop.) The originating device receives the information back after all other loop devices have received and transmitted it. By comparing returning

information with what was sent out, errors along the loop are automatically detected.

HP-IL is capable of transmission speeds of up to 5,000 bytes per second. This speed is equivalent to about one printed page per second.

Three different roles are defined for HP-IL devices: Controller, talker and listener. Any device not assigned one of these roles is inactive. The controller is the one device in the loop that can designate the roles of devices and control the loop's operation. The system controller is the device that controls and initiates loop communication. It can transfer control to another device, which then becomes the controller on the loop (the active controller). Likewise, an active controller can transfer control to another device.

In order to distinguish between devices in the loop, each device must have an address (a number from 1 to 30). The controller uses the addresses to specify and control the devices. Even though each HP-IL device has a built-in address, the system controller always assigns new sequential addresses to each loop member. These addresses begin with address one for the device that follows the controller. Each device then stores its assigned address internally.

Information is in two categories: commands and data. Each piece of information, a command or data, is initiated by a device and sent around the loop. Each subsequent device, in turn, receives the information and either sends the information to the next device, or processes the information and then sends the information on to the next device.

8B-47. MPU TO HP-IL INTERFACE. The HP-IL controller U2O is used to interface the analyzer to devices that work at relatively low data rates, i.e., a digital cassette drive. U2O serves the purpose of converting signals back and forth from HP-IL to the MPU. The processor communicates with U2O through memory or I/O read and write cycles. The HP-IL chip has a Chip Select line (CS) and three address lines (RS0-2) to permit data transfers to and from eight internal registers. Note that some of the register bits are read-only, or write-only while some have bits that are both.

A write operation occurs when Low HP-IL Write (LHLW) from the macro decoder goes low, then the register selected by RS0-2 will be written to by the processor via the HDRW0-7 data bus. Read operations operate the same as a write operation except the Low HP-IL Read (LHLR) line will be asserted low.

The 2 MHz clock from the system timing controller provides the clock for the HP-IL chip. A low reset (LRST) from the power up master reset circuit will shut off the internal oscillator allowing the processor to initialize the chip.

8B-48. HP-IL INTERFACE LINES AND OPERATIONS. The signals from the previous device come into the receive data inputs RXD0 and RXD1 through a small pulse transformer in UT1 which provides a voltage step-up and isolates this device from the loop. R3 and R6 from the receiver inputs provide the proper load for the loop.

Each of the transmitter outputs TXD0 and TXD1 pass through a low-pass filter and impedance matching network consisting of C2, R5 and C1, R4. The signals then go through a pulse transformer which steps down the voltage to the proper loop level and isolates this device. Zener diodes CR1-4 are provided for transient suppression.

Whenever one or more of the interrupt bits together with the corresponding enable bit in the interrupt register is high, the interrupt request line HLI will be low. This signal is then inverted by U3P and seen in the interrupt mask. The MPU will respond, clearing or masking the bit, and IRQ will return to its normal high state. Unless the interrupt flag bit is cleared or masked, no further interrupts can occur since the interrupt line will remain in its low state.

8B-49. Probe Reference Voltage Adjust (see schematic 8B-7)

The thresholds (THR0-4) for each pod are reference power supplies that specify the comparator switching points on the pod hybrid chip. Each of the five processor programmable supplies consist of a sample/hold circuit selected by U7O, and adjusted by U9N, a programmable DAC. Data can be specified in ranges of plus to minus 9.9 volts in 0.1 volt increments.

8B-50. PROBE THRESHOLD SELECTION. The following is a brief example of this circuit's operation for selecting one probe threshold: The user can request a specific threshold for sampling data on each pod, either TTL, ECL, or a level equal to or less than ± 9.9 volts (this system defaults to TTL sample levels). After a threshold is selected the processor will program U9N (via U9E), a digital-to-analog converter (DAC) for a current level proportional to the threshold. This current level is then converted by U8O to a voltage level proportional to the required threshold. A probe threshold driver is selected by U7O. The selected reference threshold level is then used by the pod hybrid chip. The probe threshold driver will hold a reference level until it is refreshed or updated.

8B-51. ADDITIONAL INFORMATION. The DAC is configured for write only operation. The processor writes information into the DAC via the keyboard controller U9E. When BD is high, write information is presented to the DAC, and a probe threshold driver is selected by U7O (via the scan line outputs SL0-2 of U9E). Then, when BD goes low it is delayed in the voltage reference circuitry. When U7P pin 13 goes low, the DAC latches the data on its input, converts it, and presents it to U7O. When U7P pin 14 goes high, the selected probe threshold driver samples the converted data. Then, in 100 mV increments, a reference voltage (THR0-4) proportional to the user threshold sample voltage is output. The reference voltage is refreshed or updated every keyboard scan time. A keyboard scan time is 5 mS or every time BD goes low.

The ground sense lines, GS0-4, compensate for the difference in ground levels between systems. For example, if the voltage on GS0 was able to form a voltage drop across R4 of UR9P then the voltage on THR0 would increase proportionally. This insures that data is being sampled at the user selected threshold level with respect to the users system ground.

The Voltage Reference circuit provides a precision +5 volt supply for the DAC and a voltage reference (VR) for U7P in the Power-Up Master Reset circuit.

8B-52. Keyboard Scanning (see schematic 8B-7)

The keyboard controller, U9E, is used to scan the keyboard and control probe reference voltage adjustments. U9E is programmed and controlled by the processor for each of these functions. The following will describe the keyboard scanning functions of U9E.

8B-53. MPU TO KEYBOARD CONTROLLER INTERFACE. The I/O control section of U9E uses four signals to control data flow to and from several internal registers and buffers via the HDRW0-7 data bus. With chip select (CS) tied, low bi-directional data flow is always enabled. A high on the A0 line indicates that the information going in or out to the MPU is command or status. whereas a low means the information transferred is data. When LIS0 is low, data or status is read (RD) into U9E. When LIS1 is low, data or status is written (WR) into U9E.

The 1.27 MHz PH6 signal ties to the clock (CLK) input of U9E. By programming U9E, this frequency is divided internally to 100 KHz which yields a 5 ms keyboard scan time or a 200/sec scan rate.

The Reset Line (RST) is tied to the power up master reset circuit via the High Master Reset line (HMR).

8B-54. KEYBOARD SCAN OPERATIONS. The keyboard controller uses the sensor matrix mode for scanning the keyboard. This means that each switch is given a specific sensor matrix location in an 8 bit x 8 bit sensor RAM on U9E. Thus, the sensor RAM keeps an image of the state of the switches in the sensor matrix. In this mode debouncing of the switches is not done. However, the advantage is that the MPU can determine how long a switch is depressed. The interrupt request line (HKBI) will go high, and stay high at the end of a sensor matrix scan if a location has changed value.

The following is an example of a sensor matrix scan: Scanning the rows of the sensor matrix, or keyboard, is done with the combination of the encoded scan lines, SL0-2. These lines will count from zero to seven in binary enabling U9F, a 1 of 8 demultiplexer. U9F will low select the proper row (KBR1-6) of switches that corresponds to the proper row, or byte, in the sensor RAM matrix. Then, while each row is asserted, each column (KBC0-7) in the sensor matrix is sampled and loaded into their respective bit locations in the sensor RAM. If a low was sensed on a column line, then the intersection of that row and column indicates a switch closed in the sensor matrix. The IRQ line will then go high indicating to the processor that a switch was pressed. The processor will service the interrupt and IRQ will go low. See figure 8B-10 for the keyboard switch to sensor matrix address locations.

BYTE ROWS ↓ BIT COLUMNS

	KBC7	KBC6	KBC5	KBC4	KBC3	KBC2	KBC1	KBC0
KBR0	row not used							
KBR1		CHART	WFORM	LIST	TRACE	FORMAT	SYS.	CURSOR ↑
KBR2				F	E	D	[ ] NEXT	CURSOR →
KBR3		RUN	C	B	A	[ ] PREV	CURSOR ↓	CURSOR ←
KBR4		STOP	9	8	7	CHS		ROLL ↓
KBR5		PRINT	6	5	4	DON'T CARE	ROLL ↑	
KBR6	BLUE	3	2	1	0	CLR ENTRY	INSERT	
KBR7	row not used							

NOTES

a. Keys do not exist for blank spaces above
b. KBC0-7 = Keyboard column 0-7
c. KBR0-7 = Keyboard row 0-7

Figure 8B-10. Keyboard Switch to Sensor Matrix Address Locations

8B-55. Keyboard Switch Pad (see schematic 8B-8)

The keyboard is a 6 x 8 matrix consisting of 6 rows labeled KBR1-6 that are enabled one at a time, and 8 columns (KBC0-7) that are sampled each row time for a closed switch. The 38 keys used are single-pole single-throw switches. The keyboard interfaces with the keyboard controller, U9E, on the CPU board.

8B-56. DISPLAY SYSTEM OPERATION VERIFICATION & TROUBLESHOOTING

The following procedure and information is used to determine if the CPU, Display Driver, or CRT is faulty. The first section determines if the CPU board is bad, the second determines if the CRT or Display Driver is faulty.

CPU INTERFACE OPERATION VERIFICATION

NOTE

The following procedure assumes that there is NO video information being displayed on the CRT.

a. Turn OFF the logic analyzer.

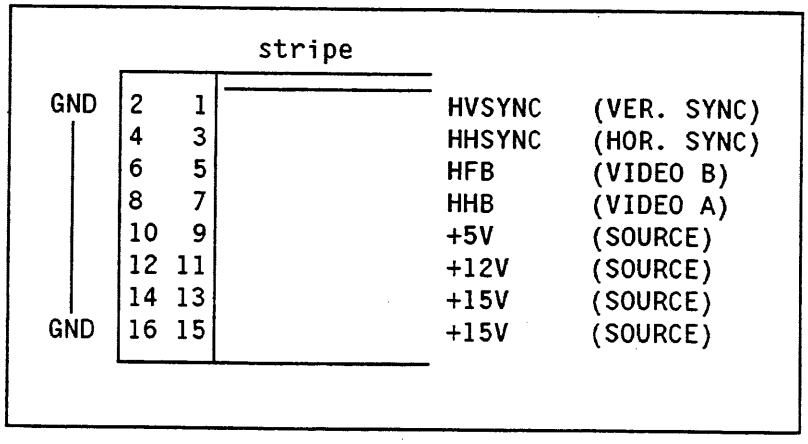
b. Remove the two plastic standoffs and loosen the screw that secures the top cover. Remove cover. For more information refer to the installation and removal procedures in Section II.

c. At the Display Driver board disconnect the 16-pin ribbon cable (W2) going to the CPU board.

d. See table 8B-5 for cable pin assignments. Probe these pins while referencing tables 8B-5 and 8B-6.

e. See table 8B-6 for applicable electrical specifications if problems exist.

Table 8B-5. CPU To Display Driver Cable Pin Assignments



VIEW FROM PIN SIDE

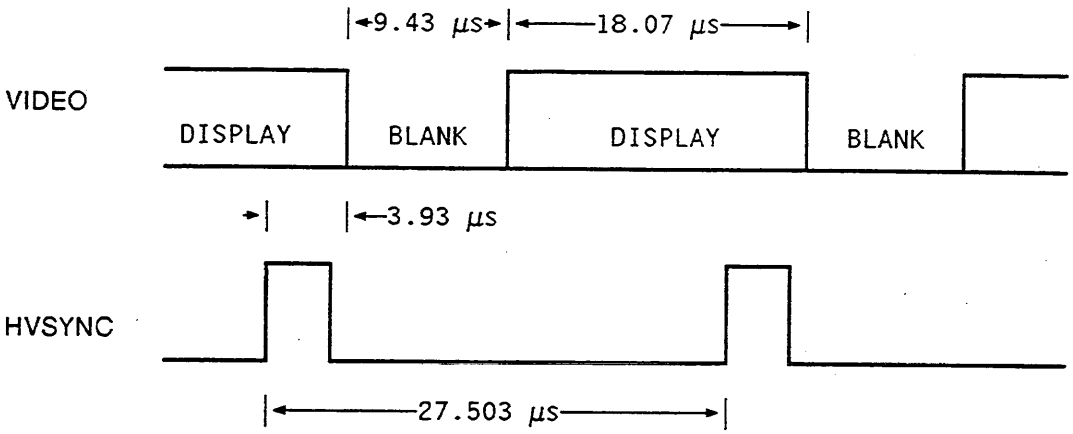
Table 8B-6. Applicable Electrical Specifications

Vertical Sync. (fast axis)

a. Single-ended TTL input: HVSYNC

b. Sync signal timing characteristics.

Pulse width and position relative to the video. Timing is indicated below:



c. Scan direction is top to bottom.

Horizontal Sync. (slow axis)

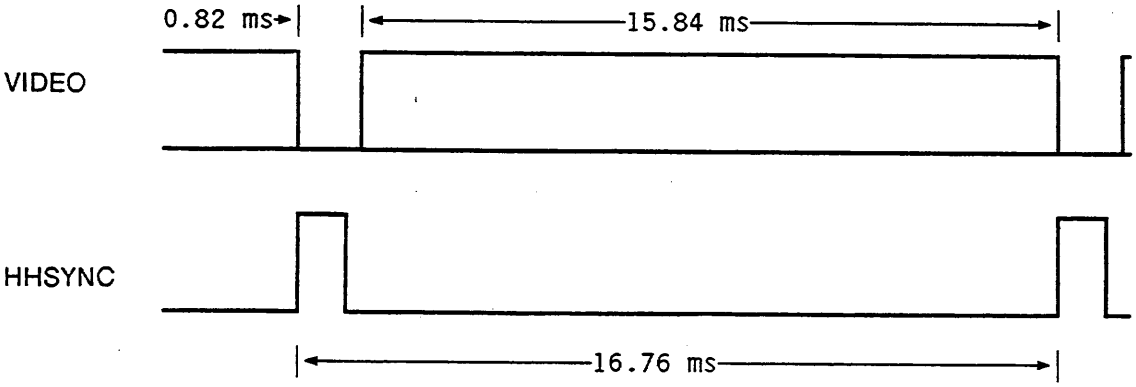
a. Single-ended input: HHSYNC

1. Low level signal is less than or equal to 0.4 volts.

2. High level signal is 5.0 volts ± 5%.

b. Sync signal timing characteristics.

Pulse width and position relative to the video. Timing is indicated below:



c. Scan direction is left to right.

Table 8B-6. Applicable Electrical Specifications (cont'd)

Video information

a. Single-ended TTL inputs

1. Half-bright: HHB
2. Full-bright: HFB

b. Truth Table

HFB	HHB	Video Output
0	0	OFF
0	1	Half-Bright
1	0	Full-Bright
1	1	Full-Bright

c. Dot period is 49.1ns

Power Supplies

a. +5 volts ±5%

b. +12 volts ±5%; Imax is 0.085 Amps
(+12 volts used only for CRT filament)

c. +15 volts ±5%; Imax is .8 Amps average
1.5 Amps peak
.65 Amps typical

(+15 volts used for horizontal and vertical deflection)

DISPLAY DRIVER OPERATION VERIFICATION

The following procedure will help determine if the Display Driver or the CRT is faulty.

a. Verify that the 16 inputs from the CPU board meet the specifications given in table 8B-5 and 8B-6.

b. If there is correct video information on the CRT, perform the Display System Adjustments procedure given in Section V (Adjustments). If any display adjustment cannot be performed, check the typical operating voltages for the CRT given in the table 8B-7. Use a HIGH VOLTAGE PROBE for these measurements.

c. If the voltages to the CRT are correct, the Display Driver is bad and should be replaced.

d. If there is incorrect video information on the CRT, check the display generation circuitry on the CPU board, i.e., CRT Controller, Character ROM, etc.

e. If there is NO video information on the CRT and the typical operating voltages for the CRT (see table 8B-7) are correct, then the CRT and Display Driver are suspect.

Table 8B-7. Typical Operating Voltages For The CRT

NOTE
Unless otherwise specified, voltage values are positive with respect to Grid 1*.

NAME	CRT BASE PIN #	CRT BASE CONNECTOR WIRE COLOR	TYPICAL OPERATING VOLTAGES
Grid 4	7	blue wire	0 to 400 Vdc
Grid 2	6	red wire	500-800 Vdc; Typ. 700 Vdc
Grid 1	5	not connected	
Heater	4	black wire	0 V
Heater	3	brown wire	12 Vdc; 13.2 Vdc Max.
Cathode	2	yellow wire	48-82 V
Grid 1 *	1	green wire	0 V
Anode		red post accelerator lead	8-12 KVdc; Typ. 10 KVdc

8B-57. MNEMONICS.

Signals on the CPU board have been assigned mnemonics in alphabetical order that describe the active state and function of the signal (see table 8-1 Logic Symbols). A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. A "H" prefix indicates that the function is active in the "high" state; a "L" prefix indicates that the function is active in the "low" state. Table 8B-8 is a listing of the mnemonics used on the schematics.

Table 8B-8. Mnemonics

Mnemonic	Description
20MHZ	20 MHz clock used to derive the 1.27 MHz clock rates of the control timing circuit. This signal also determines the dot rate for character generation.
2MHZ	2 MHz clock from the system timing controller for use by the HP-IB control chip.
4MHZ	4 MHz clock from the system timing controller for use by the HP-IB control chip.
AMS	Address MUX Select. AMS selects which group of RAM address multiplexers control the RAM address lines during an MPU cycle. Multiplexers isolate each functional group (MPU, CRTC, or Graphics) from the RAM address bus HRAA0-7.
ATN	Attention. Ties to HP-IB ATN line via transceiver. Defines type of data on the data bus (addresses/commands or data).
CL0-CLD	Control Latch 0-D. Used by the MPU to control various system functions. See table 8B-1 for the Control Latch Bit assignments.
D0-7	Data outputs from the Character ROM and graphics output buffer to the display data shift register.
DAV	Data Valid. Ties to the HP-IB DAV line via transceiver chip. Indicates availability and validity of data on the data bus.
DIO1-8	Data I/O Bits 1-8. Connected to HP-IB I/O lines via transceiver.
ENDT	Enable Data Transfer. When high, allows data to be written to the acquisition system. When low, allows data to be read from the acquisition system.
EOI	End Of Identify. Bi-directional line that ties to the HP-IB EOI line via transceiver. Indicates end of data transfer or identifies initiation of polling operation.
GS0-4	Ground Sense 0-4. Return ground sense lines adjust the threshold level so that data is sampled with respect to the user's system ground.
HA0-5	Address 0-5. ECL level address lines from the CPU system to the acquisition system.
HACK	Address clock. Used to clock slave and analog boards. May be driven by Timing Master board.
HBI	HP-IB Interrupt to the processor via interrupt mask.
HBNC	Signal from the acquisition system to the rear panel BNC labeled PORT
HCRA0-7	Character ROM Address 0-7. ASCII code from RAM via ROM.

Table 8B-8. Mnemonics (Cont'd)

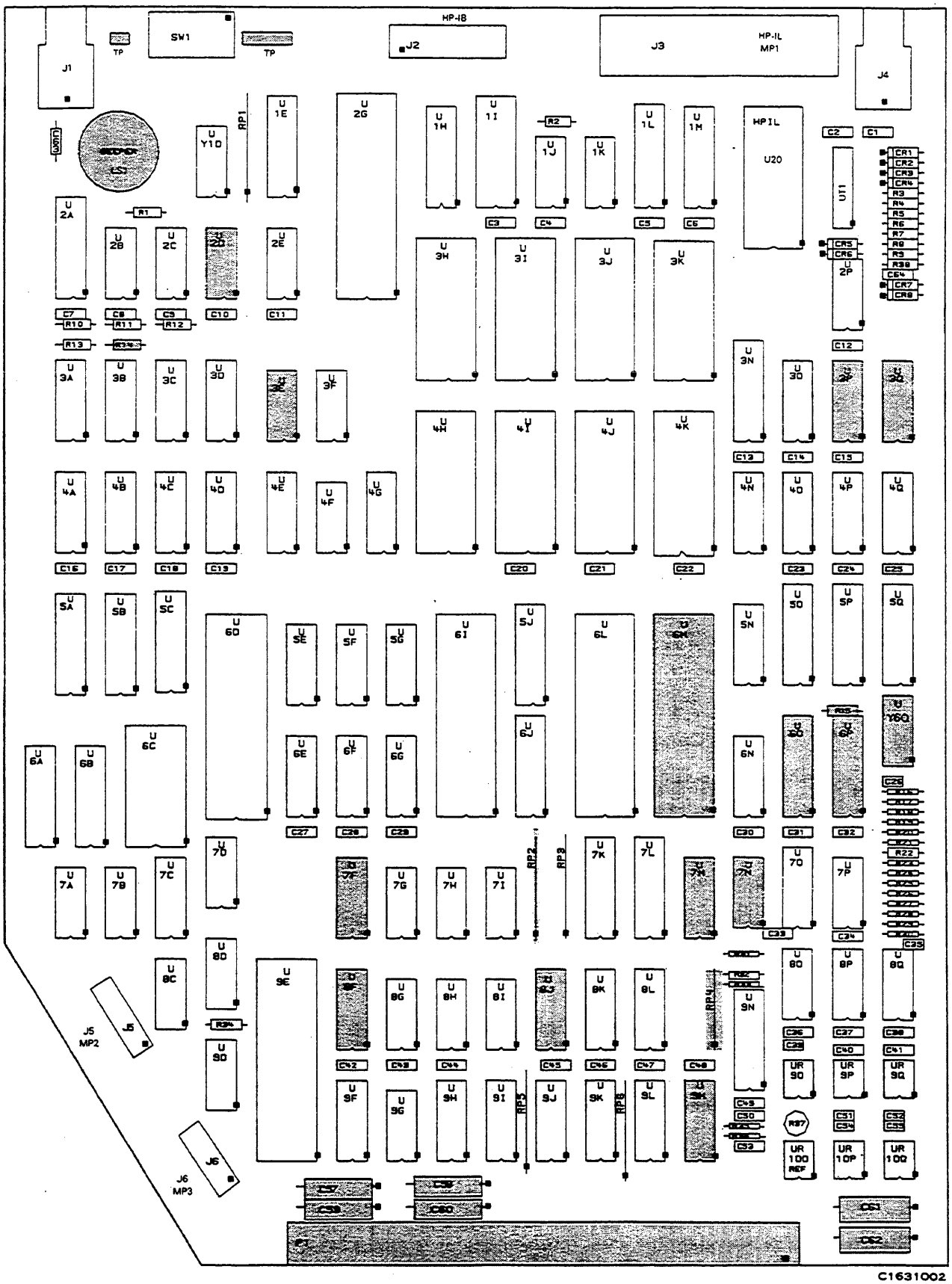
Mnemonic	Description
HCX	Clear X. This signal clears the X counter at the end of a frame.
HCY	Clear Y. This signal clears the Y counter at the end of a line.
HD0-7	Data 0-7. ECL level bi-directional data lines to/from the CPU system and the acquisition system.
HDR0-7	Data Read 0-7. Data read from the acquisition system.
HDRW0-7	Data Read/Write 0-7. Bi-directional CPU system data bus.
HDW0-7	Data Write 0-7. Write only data from the processor.
HF0-5	Formatter 0-5. Waveform information from the waveform formatter used to address the formatter ROM.
HFB	Full Bright. The combination of this signal and the HHB signal determines the brilliance of the video displayed.
HHB	Half Bright. The combination of this signal and the HFB signal determines the brilliance of the video displayed.
HHSYNC	Horizontal Sync. Used by the display driver.
HKBI	Keyboard Interrupt to processor via interrupt mask indicating a key was pressed.
HLI	HP-IL Interrupt to the processor via the interrupt mask.
HMR	High Master Reset. This signal will be high until the +5 volt supply exceeds approximately 4.75 volts.
HPA0-20	Physical Address 0-20. This is the CPU systems Physical address bus.
HRA0-3	Raster Addresses 0-3. Used by Character ROM as column address for characters.
HRAA0-7 (C,G,M)	RAM Address 0-7. Only one of three functional groups are allowed to address RAM at a given time. The functional groups are: CRTC, Graphics, or MPU. See figure 8B-4 for timing waveforms.
HRAD0-7	RAM Data 0-7.
HR/LW	High Read/Low Write. ECL read/write control signal to acquisition system.
HRTC	Real Time Clock. This signal is an interrupt from the system timing controller. The processor syncs on this interrupt for a real time clock display.
HR/WL	High Read/Write Low. Signal from the I/O decoding circuitry to the CRT Controller.

Table 8B-8. Mnemonics (Cont'd)

Mnemonic	Description
HTCK	High Timing Clock. ECL timing clock for under 5 MHz.
HTMC	Timing Measurement Complete. Indicates a measurement has been completed and that acquisition memory can be read by the processor.
HVSYNC	Vertical Sync. Used by the display driver.
IFC	Interface Clear. Ties to the HP-IB IFC line via transceiver. Places I/O system into known quiescent (idle) state.
KBC0-7	Keyboard Column 0-7. Return sense lines to the keyboard controller.
KBR1-6	Keyboard Row 1-6. Keyboard stimulus lines from the keyboard controller.
LACK	Complement of HACK.
LCAS	Column Address Strobe. Needed for RAM data transfers.
LCRE	Character ROM Enable.
LCS0-7	Chip Select 0-7. Selects which ROM is being addressed.
LECB	Enable CRTC Buffer. When low, the CRTC buffer is enabled allowing RAM to supply data to the CRT Controller (CRTC). When high, the processor supplies data to the CRTC.
LEFD	Enable Full-field Display. When low, this signal disables addressing of the Character ROM and enables the graphics address multiplexers. This allows scanning of the full-field graphics area.
LGBE	Graphics Buffer Enable. When asserted, the graphics information is loaded into the display data shift register.
LHBS	HP-IB I/O Strobe. HP-IB chip enable from the macro decoder.
LHLR	HP-IL Read. Processor controls HP-IL read operations via the macro decoder.
LHLW	HP-IL Write. Processor controls HP-IL write operations via the macro decoder.
LIRQ	Interrupt Request. Signal from the interrupt mask to the processor.
LIS0-9	I/O Strobe 0-9. Signals from the micro decoder used for read\write operations. See table 8B-4, micro I/O physical address-to-function.
LLX	Load X Counter. When low the X counter is loaded with 07 hex.
LMCI	Measurement Complete Interrupt. Interrupt to processor via interrupt mask.
LMR	Low Master Reset. This signal will be low until the +5 volt supply exceeds approx. 4.75 volts.

Table 8B-8. Mnemonics (Cont'd)

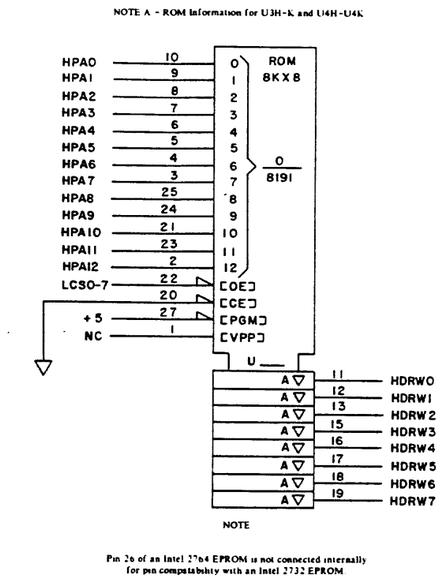
Mnemonic	Description
LRA	Register Access. Indicates that the MMUs registers are being accessed by the processor.
LRAS	Row Address Strobe. Needed for RAM data transfers.
LR/HW	Low Read/High Write. Control signal from the I/O decoding circuitry used to form HR/LW.
LRST	Low Reset. Signal will be low until +5 volt supply exceeds approx. 4.75 volts.
LSTB	Low Strobe. ECL level control signal to the acquisition system that is used with HR/LW to indicate a data transfer.
LTCK	Low Timing Clock. ECL timing clock for under 5 MHz.
LWE	Write Enable. When asserted, allows data to be written into RAM.
LW/HR	Low Write/High Read. Indicates the direction in which data is being transferred on the HDRW0-7 data bus.
MA0-13	Memory Address 0-13. Used for RAM refreshing.
NDAC	Not Data Accepted. HP-IB handshake line indicating acceptance of data by all devices.
HRFD	Not Ready For Data. HP-IB handshake line indicating that devices are ready to accept data.
PH0-PH7	Phase 0-7. Each phase is a 1.27 MHz signal from the control timing circuit. Adjacent phases are separated by 50 mS.
PH1N-7N	Phase 1-7 Not. Complement of the PH0-7 signals.
REN	Remote Enable. Ties to HP-IB REN via transceiver. Enables alternate devices to provide programming data.
RXD0-1	Receive Data 0-1. HP-IL return data from the previous device.
SRQ	Service Request. Ties to the HP-IB SRQ line via transceiver. Indicates a need for service; causes an interrupt of the current sequence to the processor.
THR0-4	Threshold 0-4. Adjustable sample threshold for the pod hybrid chip comparator.
TXD0-1	Transmit Data 0-1. HP-IL transmit information to the next device.
VR	Voltage Reference. A precision +5.00 volt reference supply.
X0-9	X coordinates for the full-field graphics display area.
Y4-9	Y coordinates for the full-field graphics display area.



Component Locator for Schematic 8B-1

NOTE 1

ROM INFORMATION FOR U3H-K AND U4H-K



NOTE

Pin 26 of an Intel 27b4 EPROM is not connected internally for pin compatability with an Intel 2732 EPROM.

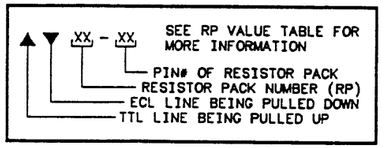
NOTE 2

U2P IS DESIGNATED AS U3P ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5V GND	14 7	U3E, 3F, 3P, 4F, U7I, 8D
+5V GND	28 14	U3H, 3I, 3J, 3K, U4H-K
+5V GND	20 10	U3N, 5O-Q
+5V GND	16 8	U4G, 4N, 4O-Q, 5F U6F

RESISTOR PACK DESCRIPTIONS



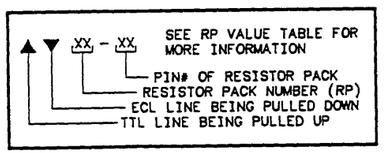
PARTS ON THIS SCHEMATIC

RP2 U3E, F, H-K, N, P, U4F-K, 4N, 4O-Q, 5F U5O-Q, 6F, 7I, 8D	

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5V GND	14 7	U3E,3F,3P,4F, U7I,8D
+5V GND	28 14	U3H,3I,3J,3K, U4H-K
+5V GND	20 10	U3N,5O-Q
+5V GND	16 8	U4G,4N,4O-Q,5F U6F

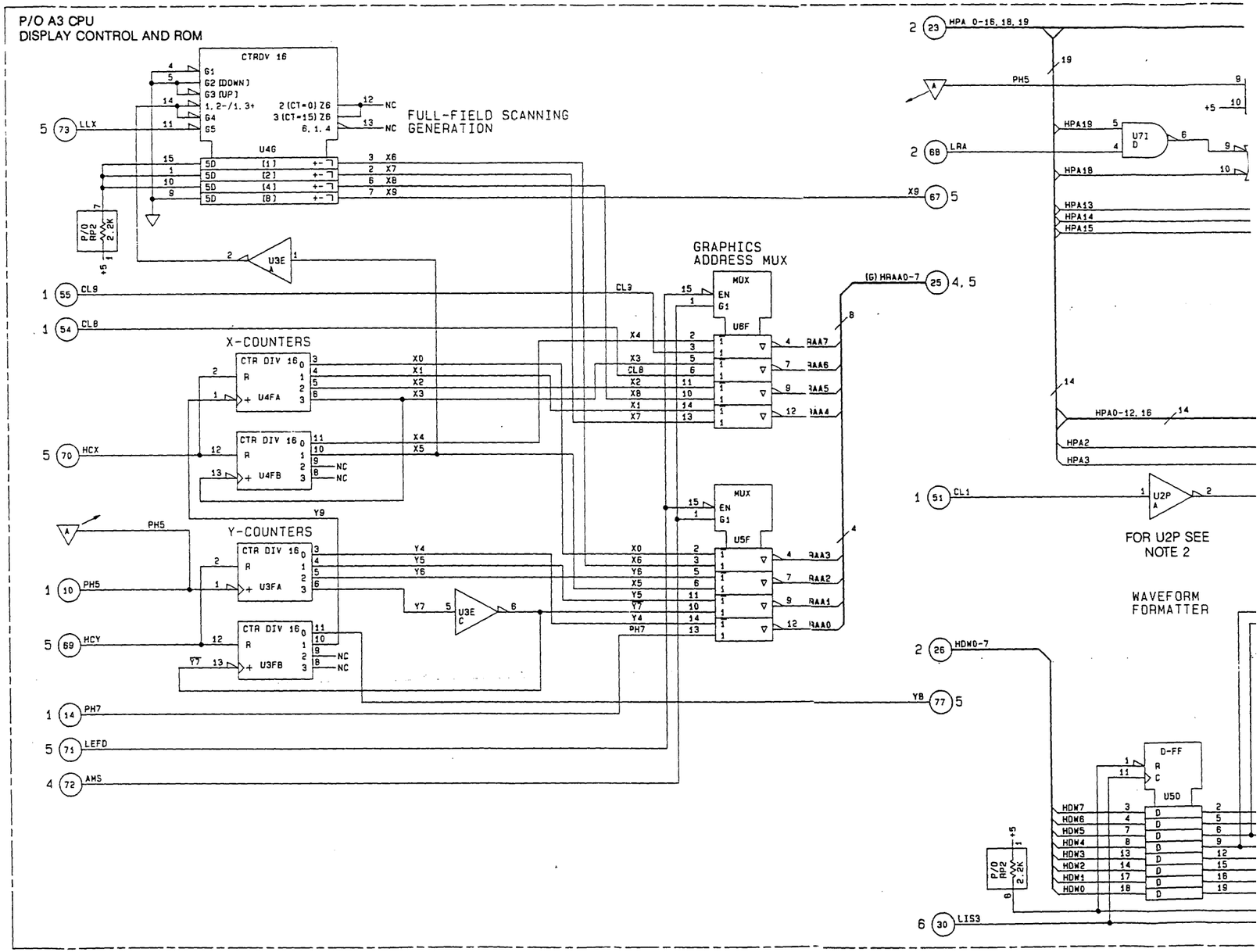
RESISTOR PACK DESCRIPTIONS



PARTS ON THIS SCHEMATIC

RP2 U3E,F,H-K,N,P, U4F-K,4N,4O-Q,5F U5O-Q,6F,7I,8D	

P/O A3 CPU
DISPLAY CONTROL AND ROM



NOTE
ROMS U3H, I, J AND U4H-U4K SHARE THE SAME ADDRESS AND DATA LINES. SEE NOTE 1 FOR ROM INFORMATION.

ROM SELECTOR

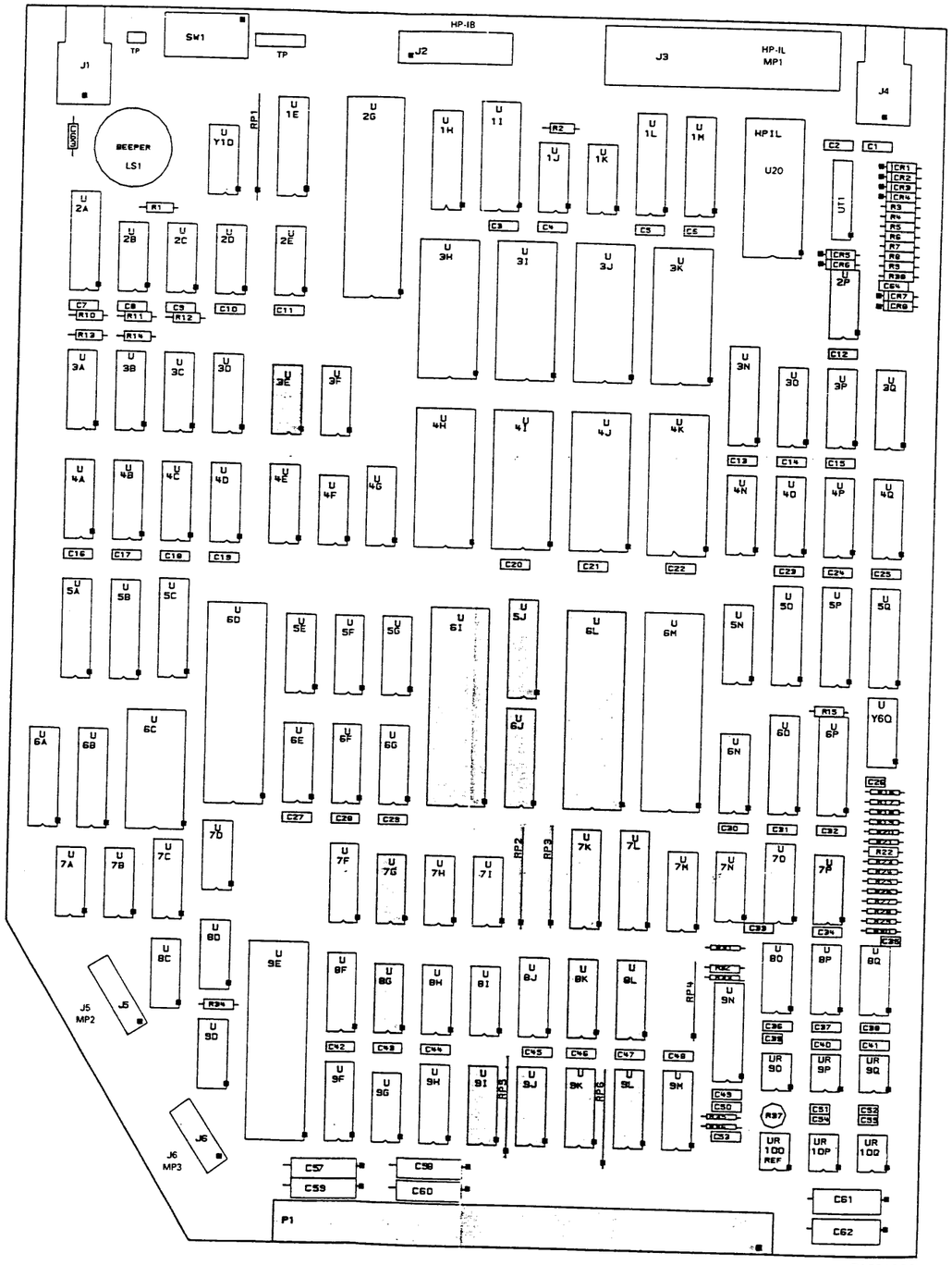
PROGRAM ROMS

FORMATTER ROM

FOR U2P SEE NOTE 2

WAVEFORM FORMATTER

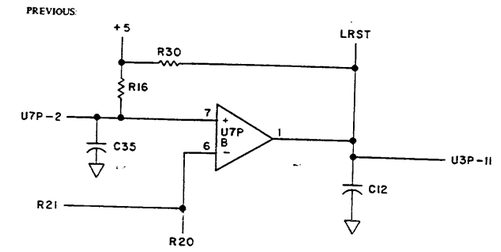
SEE NOTE A



Component Locator for Schematic 8B-2

NOTE 1

FOR CPU BOARD 01630-66503 THE FOLLOWING CIRCUIT CHANGES SHOULD BE MADE. IN THE CONNECTION TO U3P PIN 11. SEE NOTE 3 ALSO.



NOTE 2:

Two value combinations are used for C35 and R16.

If C35 is .1μF, then R16 is 100KΩ
If C35 is 1μF, then R16 is 10KΩ

For reliability reasons, C35 was changed to a .1μF METAL POLY type. R16 was changed to maintain the circuit time constant.

There is no serial prefix or serial number tracking on this change. See the Parts List, Section 7, and Service Note 1630A/D/G 1631A/D-1.

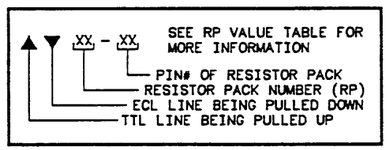
NOTE 3.

U2P IS DESIGNATED AS U3P ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5V GND	20 10	U5J,6J,7K, U7L
+5V GND	14 7	U3E,3P,7G,8G
+5V GND	7 1	U6I
+5V GND	22 1	U6L
+12V GND	3 12	U7P
+5V -5.2V GND	9 8 16	U8K,8L,9I,9J, U9K,L

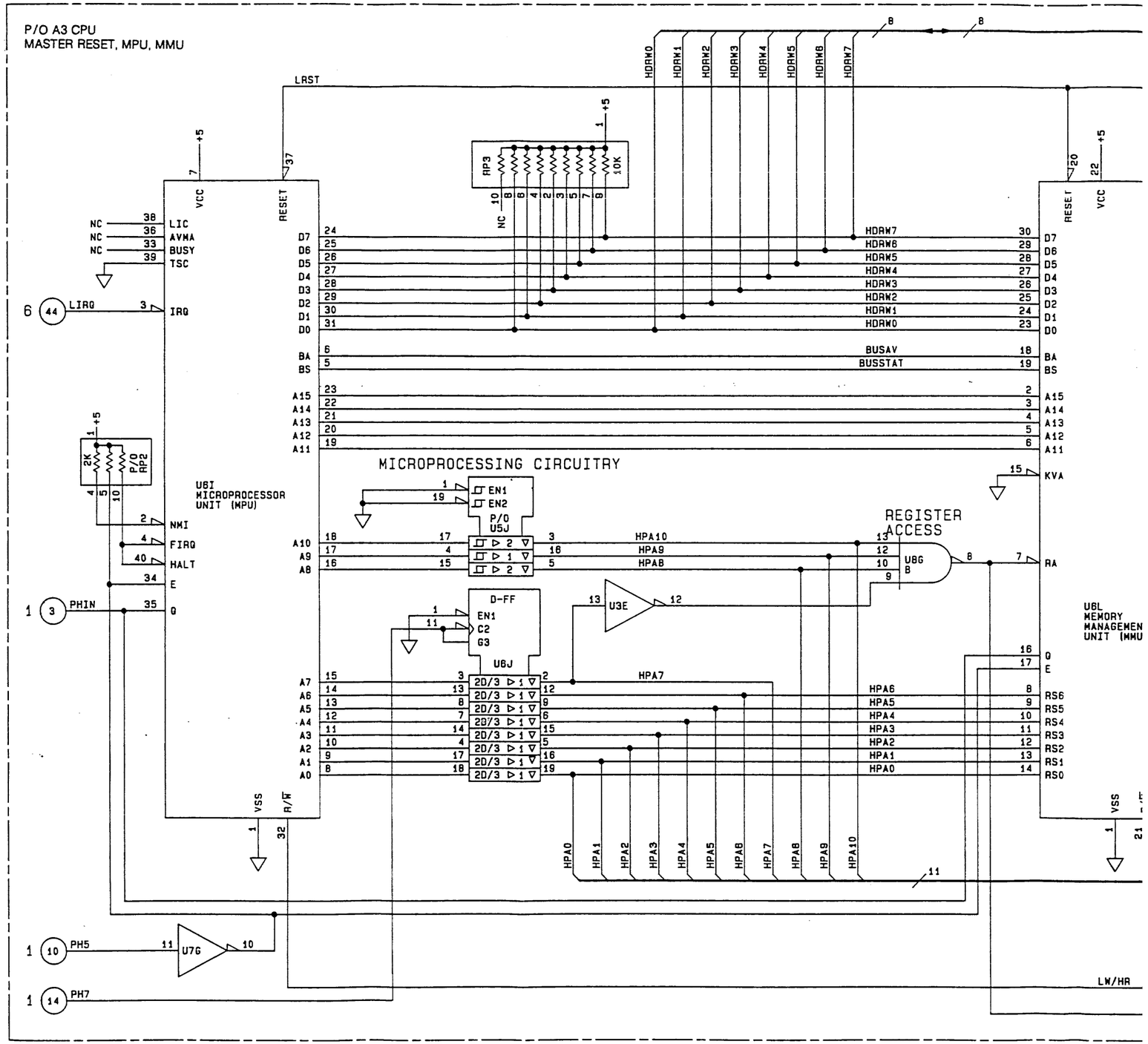
RESISTOR PACK DESCRIPTIONS

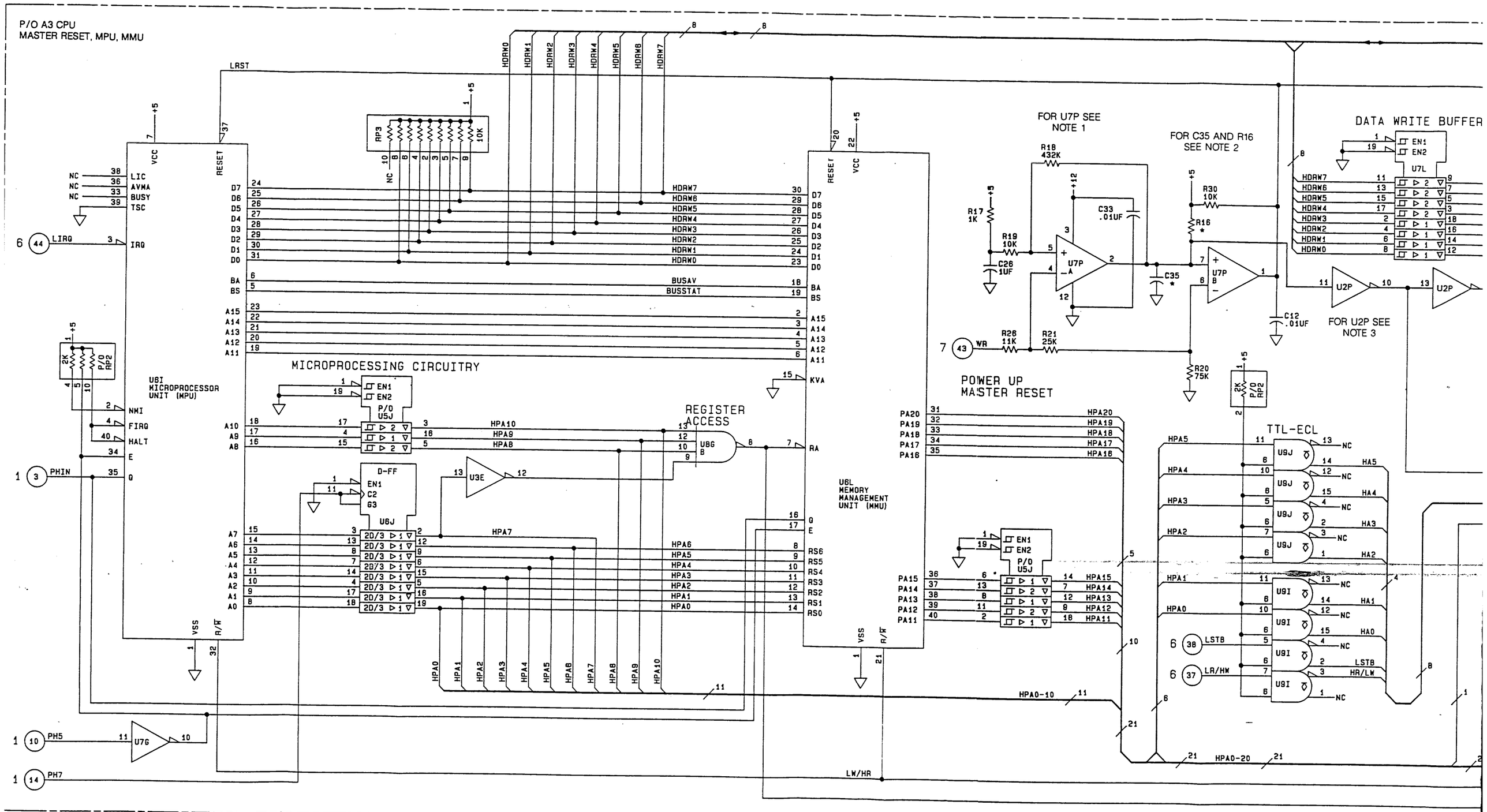


PARTS ON THIS SCHEMATIC

C12,26,33,35 R16-21,26,30 RP2,3,5,6 U3E,P,5J,6I,J U6L,7G,K,L,P, U8G,K,L,9I-L	

P/O A3 CPU
MASTER RESET, MPU, MMU




P/O A3 CPU
MASTER RESET, MPU, MMU
LRST
U6I
MICROPROCESSOR
UNIT (MPU)
MICROPROCESSING CIRCUITRY
REGISTER
ACCESS
U6L
MEMORY
MANAGEMENT
UNIT (MMU)
POWER UP
MASTER RESET
FOR U7P SEE
NOTE 1
FOR C35 AND R16
SEE NOTE 2
FOR U2P SEE
NOTE 3
DATA WRITE BUFFER
TTL-ECL
LIRQ
PHIN
PH5
PH7
LW/HR
HPA0-10
HPA0-20
LSTB
LR/HW
HR/LW

FOR U7P SEE NOTE 1

FOR C35 AND R16 SEE NOTE 2

FOR U2P SEE NOTE 3

POWER UP MASTER RESET

DATA WRITE BUFFER

DATA WRITE TTL-ECL

DATA READ

DATA READ BUFFER

DATA

ACQUISITION DATA

TTL-ECL

ECL ACQUISITION INTERFACE

ADDRESS AND CONTROL

HDW0-7 (26) 1, 3, 4

LWR (49) 1, 5, 6, 7

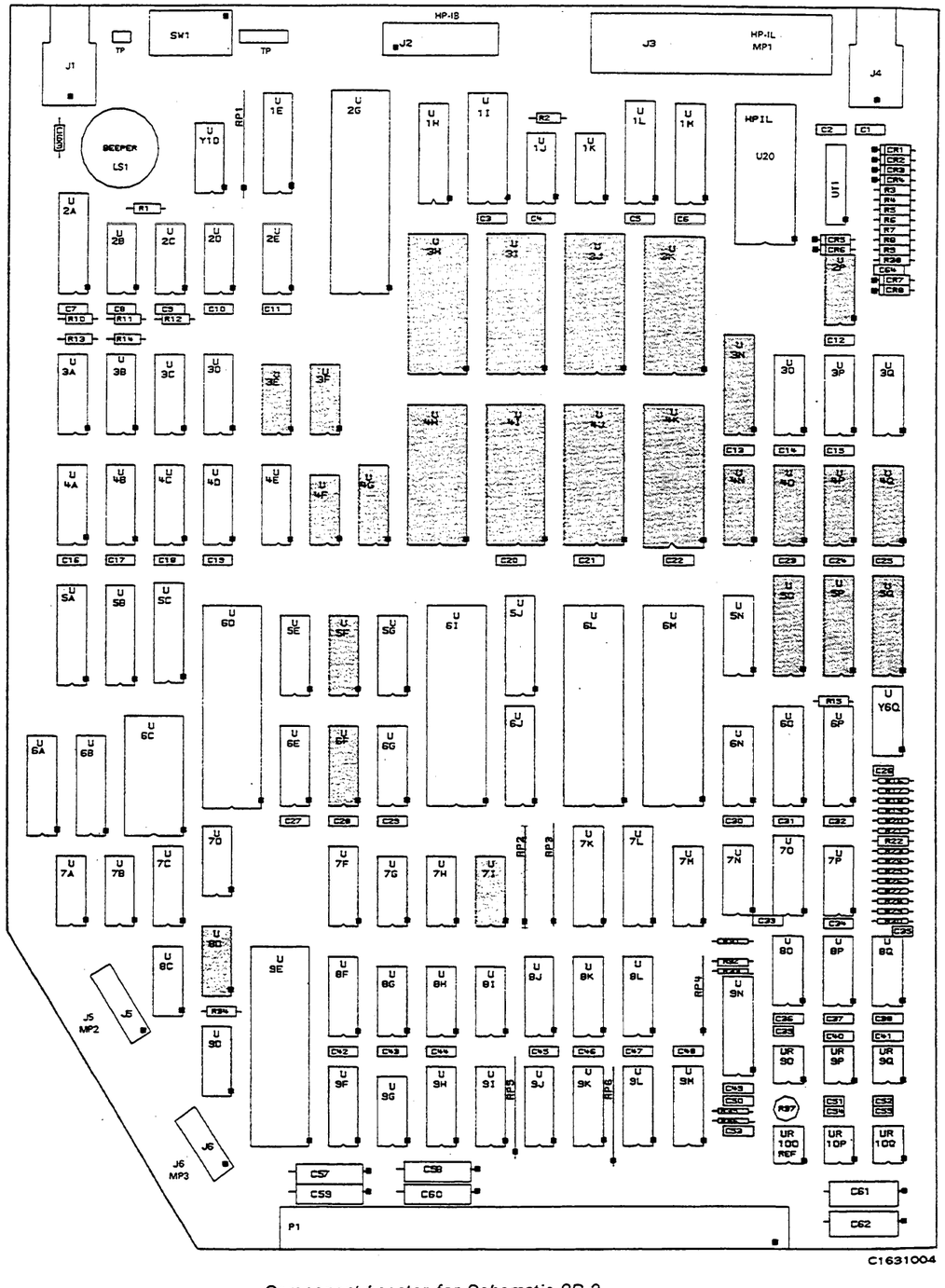
HWR (74) 1, 4, 7

HDR0-7 (24) 1, 3, 5, 6, 7

HPA0-16, 18, 19 (23) 3

LW/HR (41) 4, 6

LRA (88) 3

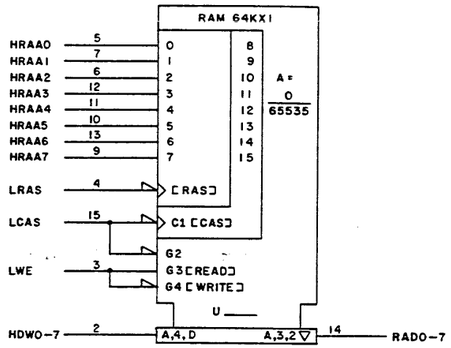


Component Locator for Schematic 8B-3

Component Locator for Schematic 8B-4

NOTE 1

RAM INFORMATION FOR U3A-D AND U4A-D



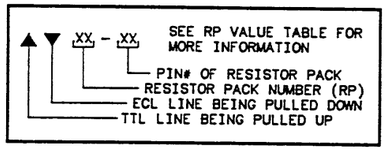
NOTE 2

THIS CONNECTION IS NOT MADE ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

IC DEVICE POWER CONNECTIONS

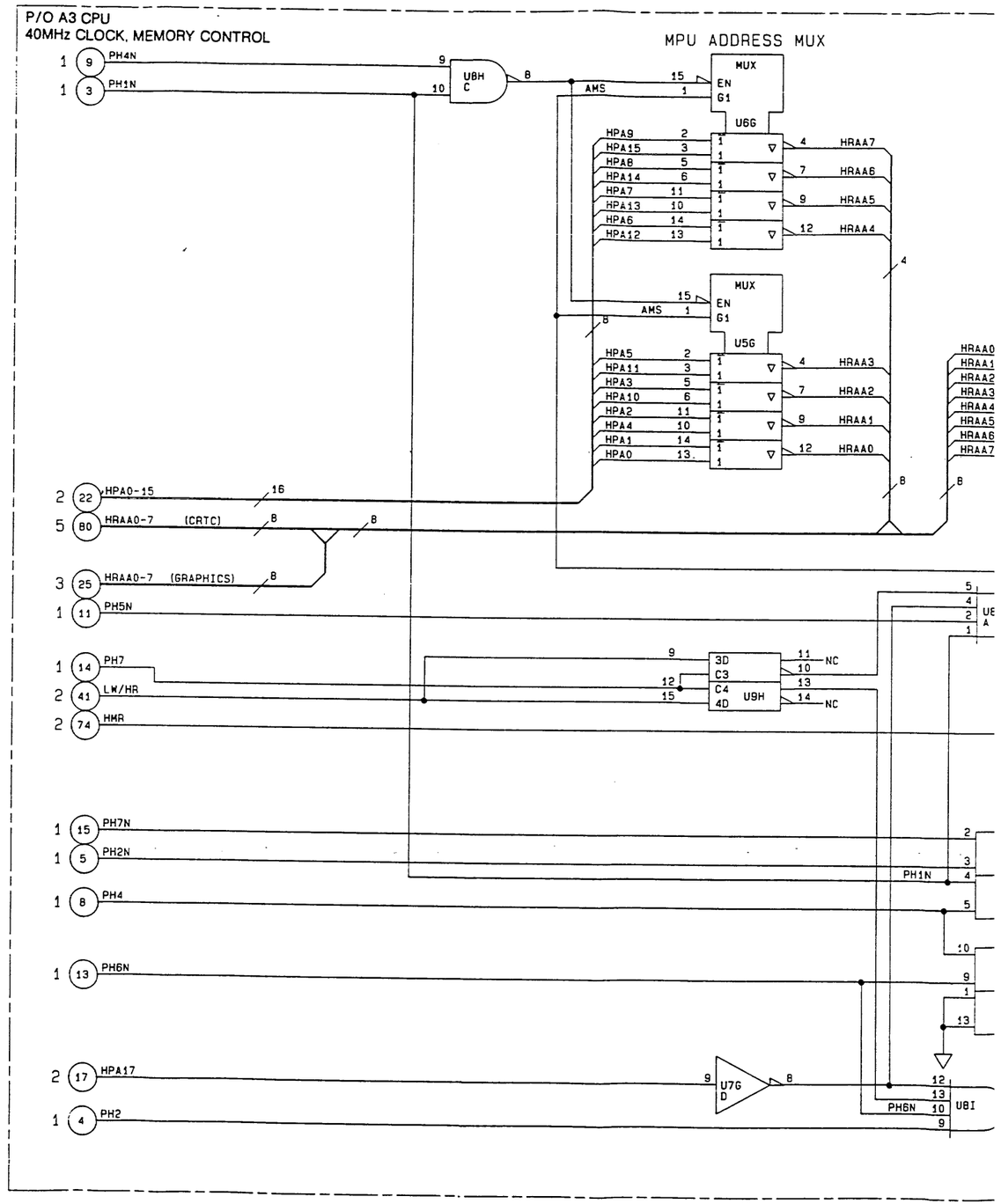
SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U2A,5B
+5 GND	14 7	U2B-E,7G,8G-I
+5 GND	16 8	U5G,6G,9H
+5 GND	8 16	U3A-D,4A-D

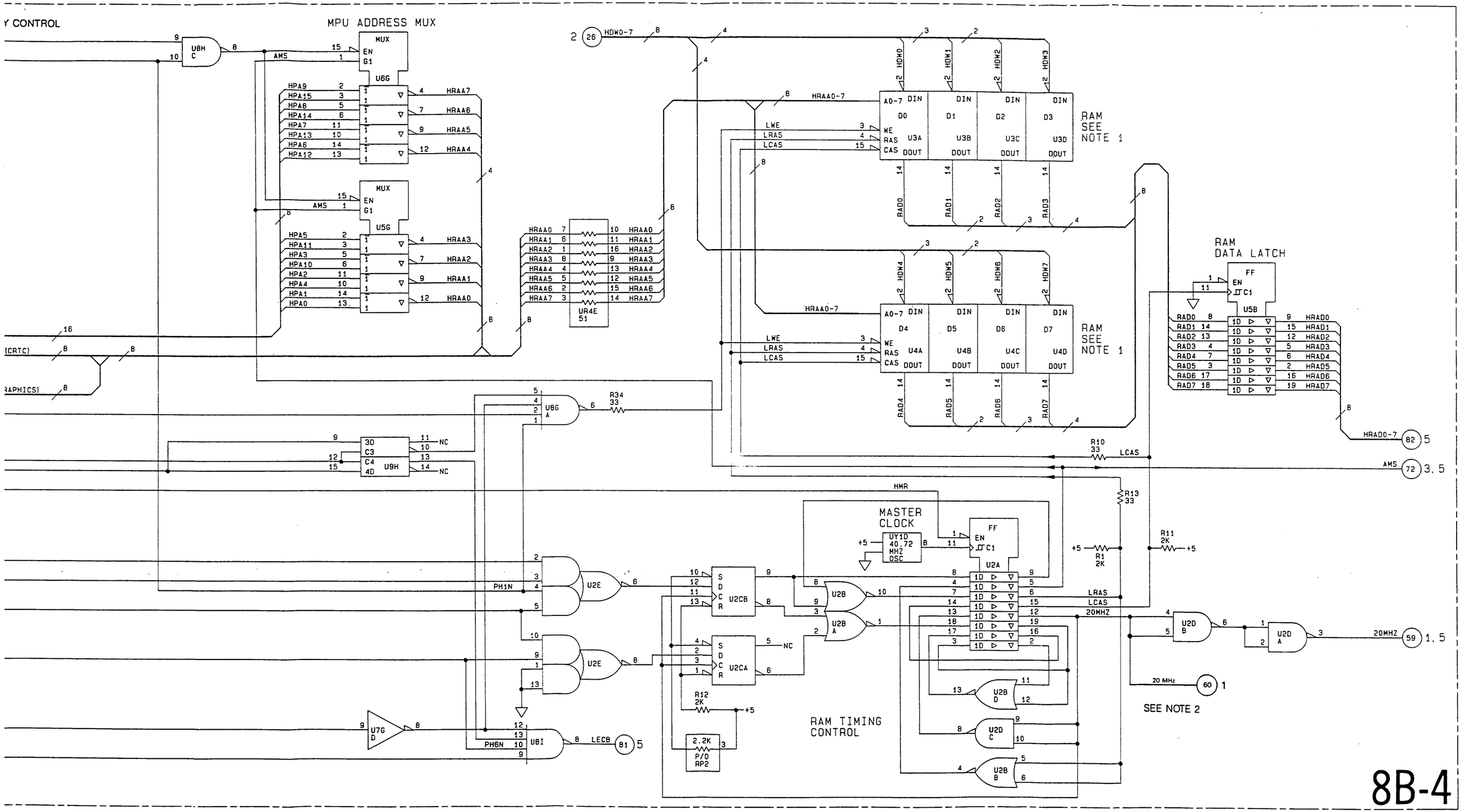
RESISTOR PACK DESCRIPTIONS



PARTS ON THIS SCHEMATIC

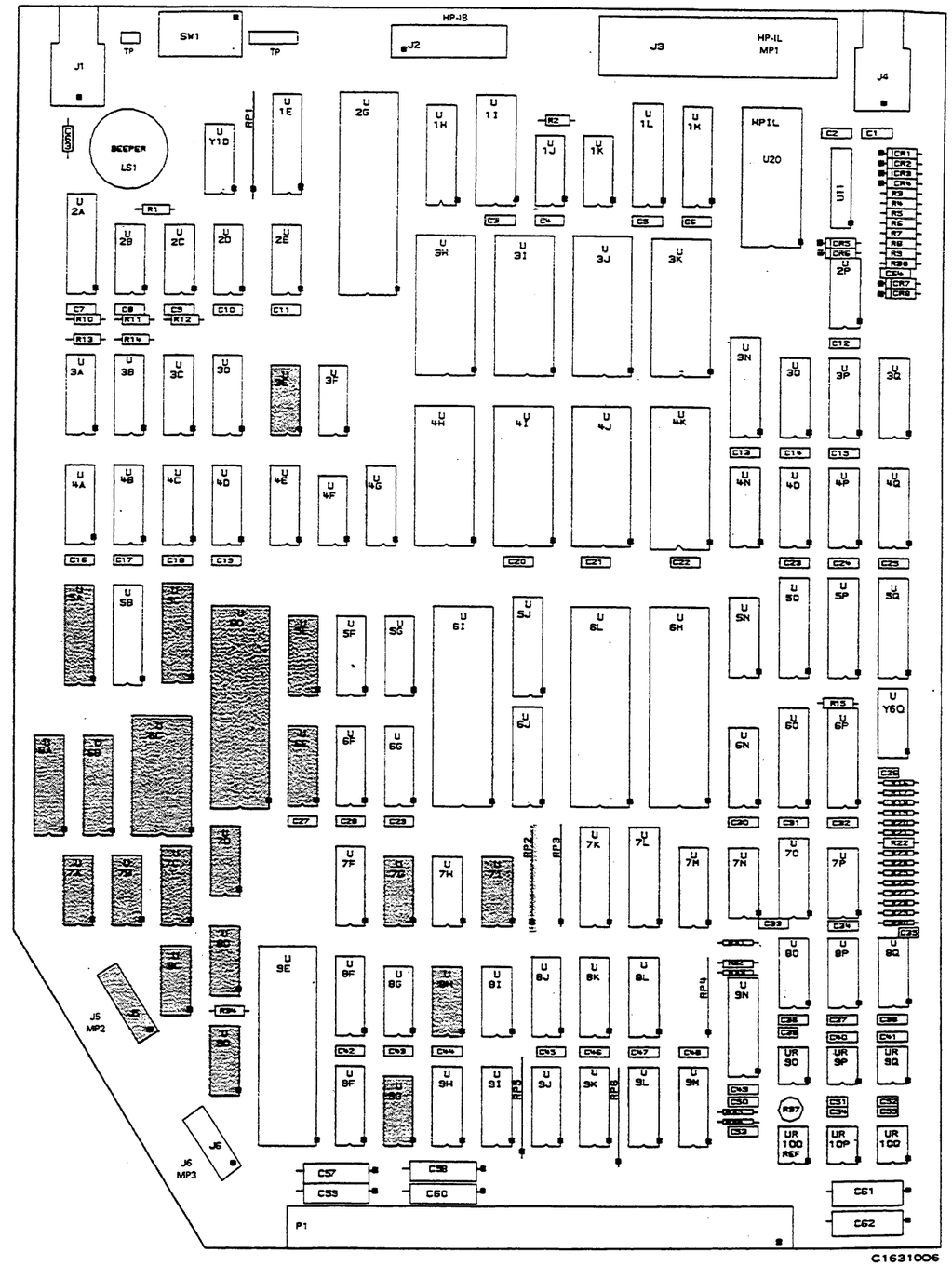
R1,10-13,34 RP2 U2A-E,3A-D,4A-D, U5B,G,6G,7G, U8G-I,9H UR4E AND UY1D	





8B-4

Schematic 8B-4
40MHz Clock, Memory Control
8B-41



Component Locator for Schematic 8B-5

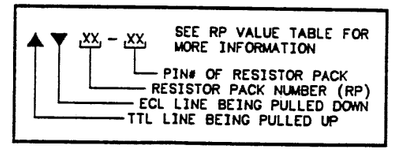
NOTE 1

CONNECTION TO SCHEMATIC 1 IS NOT MADE ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5 GND	14 7	U3E,7A,B,D,G,I, U8C,D,H,9D,G
+5 GND	20 10	U5A,C,6A,B
+5 GND	16 8	U5E,6E,7C
+5 GND	24 12	U8C
+5 GND	20 1	U8D

RESISTOR PACK DESCRIPTIONS



PARTS ON THIS SCHEMATIC	
J5 RP2 U3E,5A,C,E,6A-E, U7A-D,G,I,8C,D,H, U9D,G	

P/O A3 CPU
CRT CONTROLLER, CHARACTER ROM,
DISPLAY CONTROL

CRT CONTROL

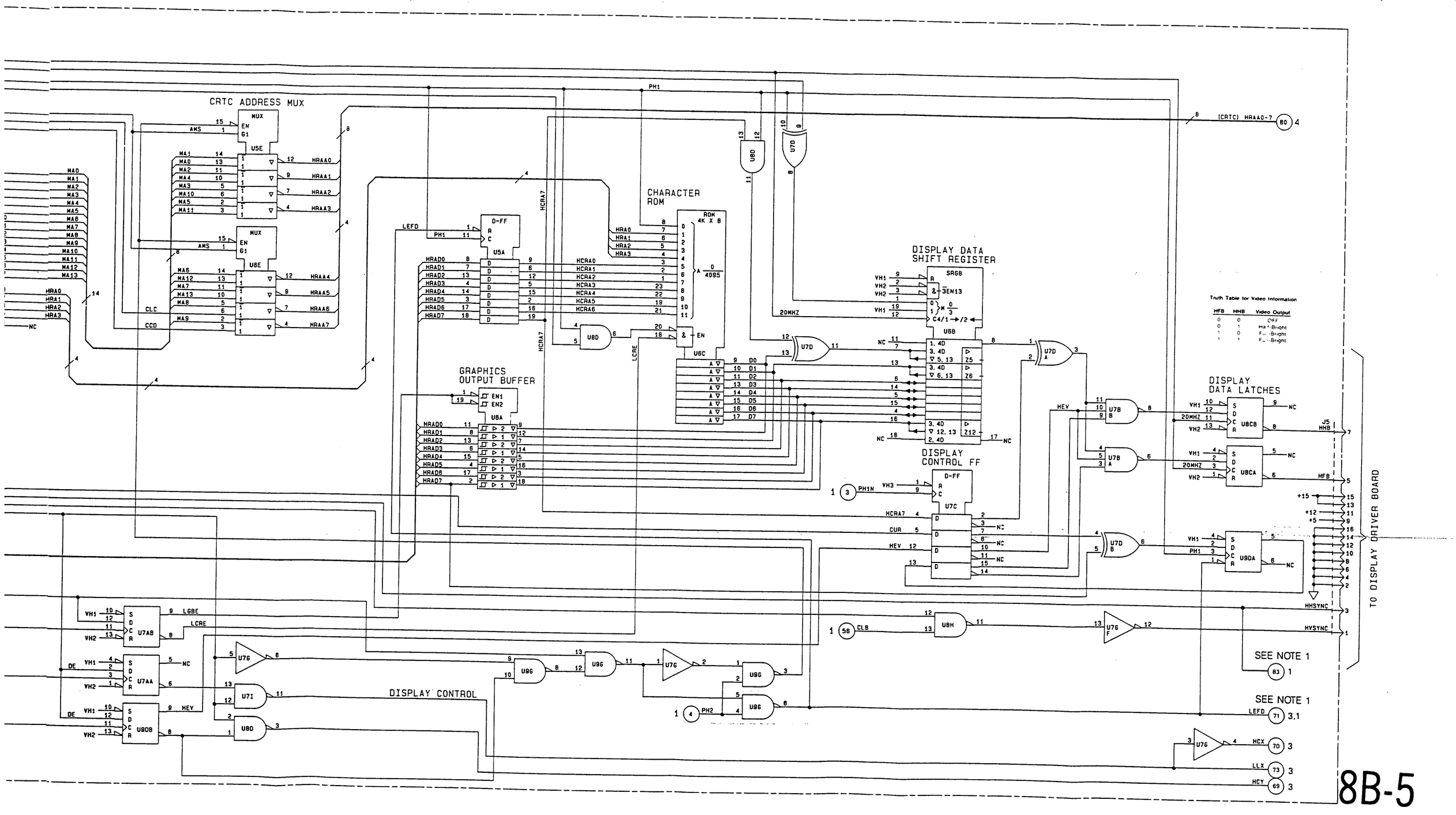
U8D
CRT
CONTROLLER

CRTC ADDRESS MUX

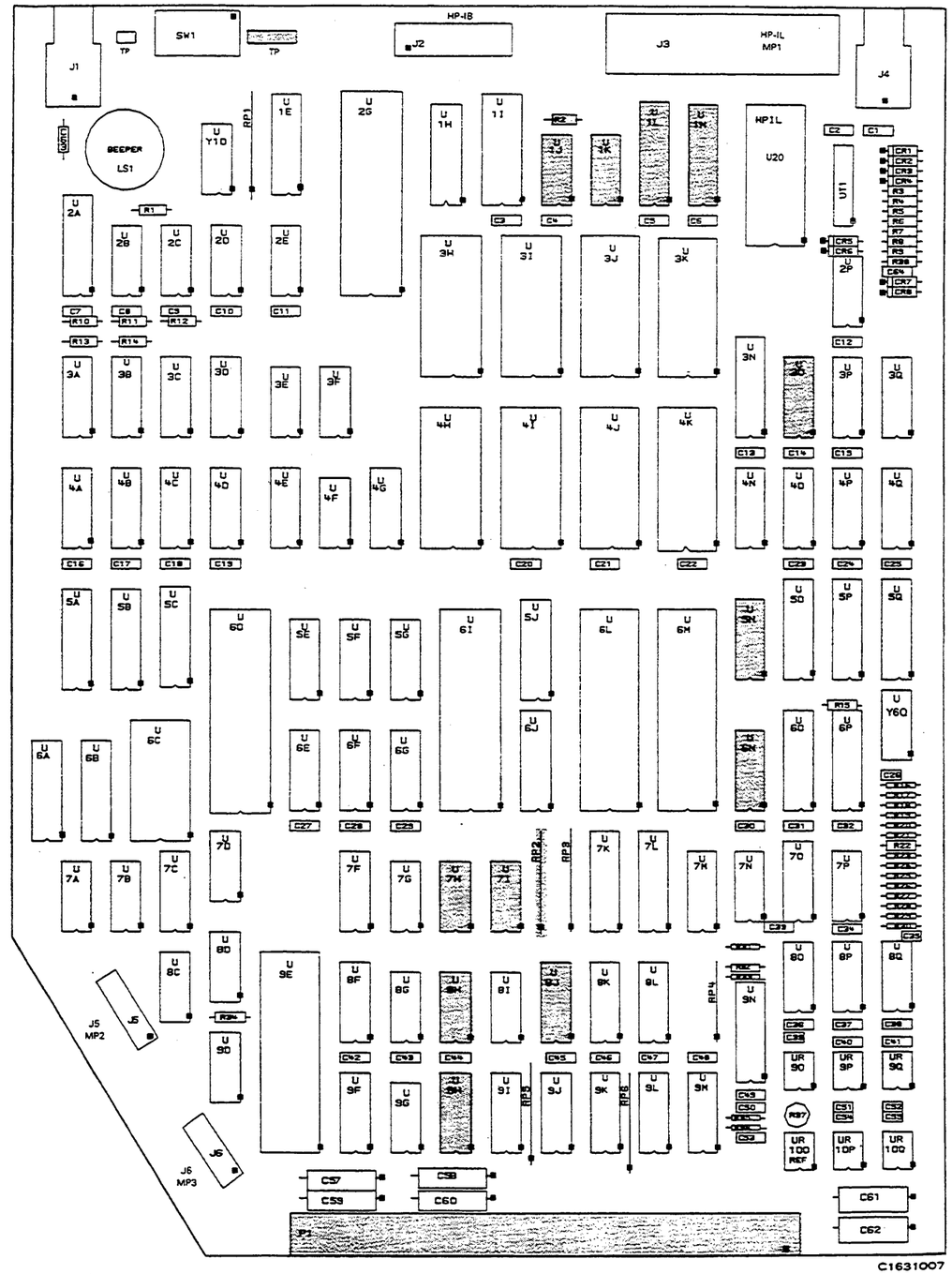
CHARACTER
ROM

GRAPHICS
OUTPUT BUFFER

DISPLAY CONTROL



Schematic 8B-5
CRT Controller, Character ROM, Display, Keyboard

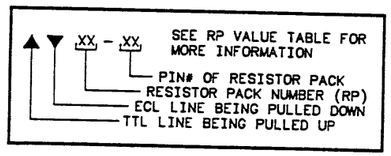


Component Locator for Schematic 8B-6

IC DEVICE POWER CONNECTIONS

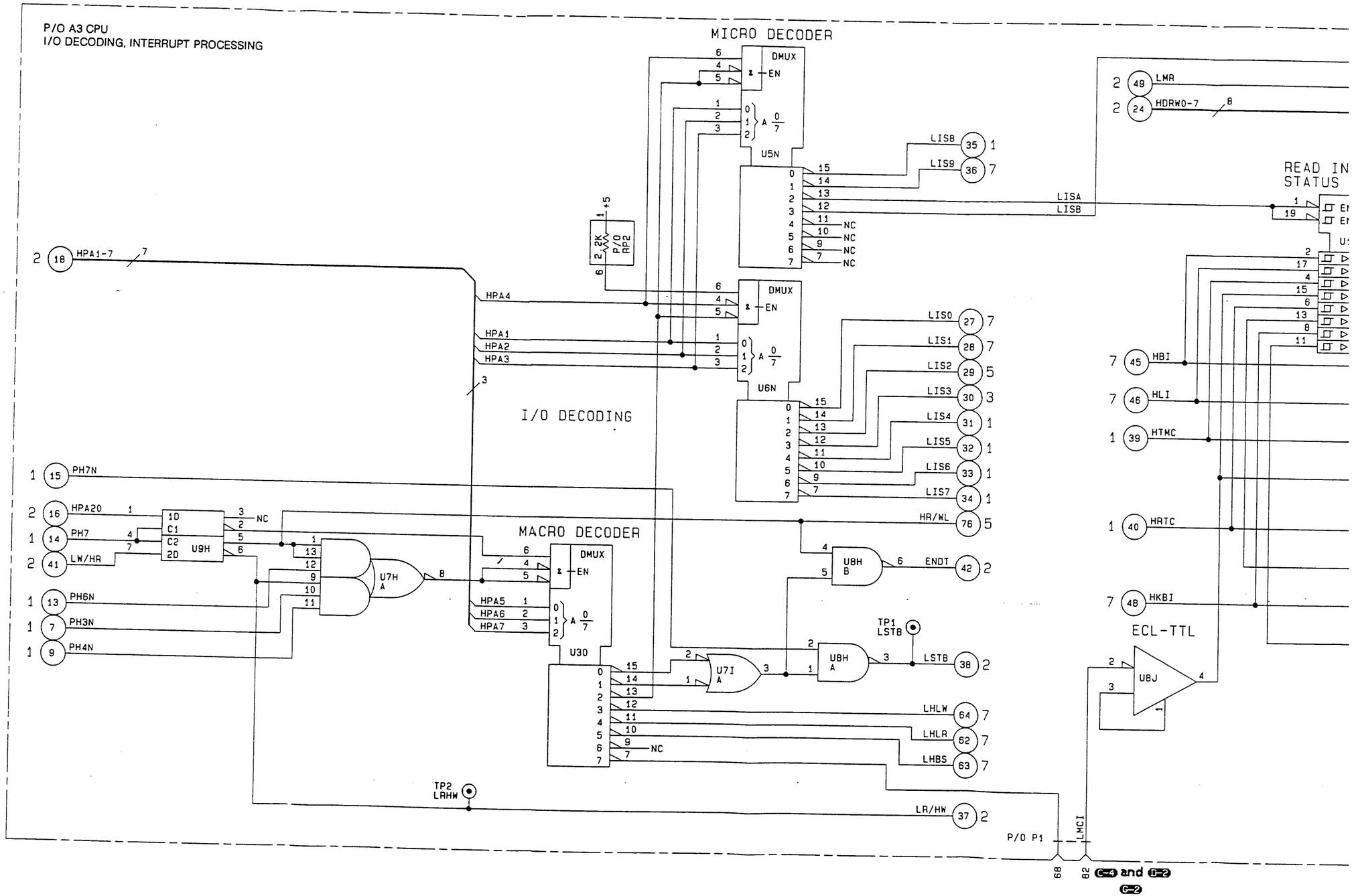
SUPPLY	PIN NO.	IC GROUP
+5 GND	14 7	U1J,K,7H,I,8H
+5 GND	20 10	U1L,1M
+5 GND	16 8	U30,5N,6N,9H
+5 -5.2 GND	9 8 16	U8J

RESISTOR PACK DESCRIPTIONS

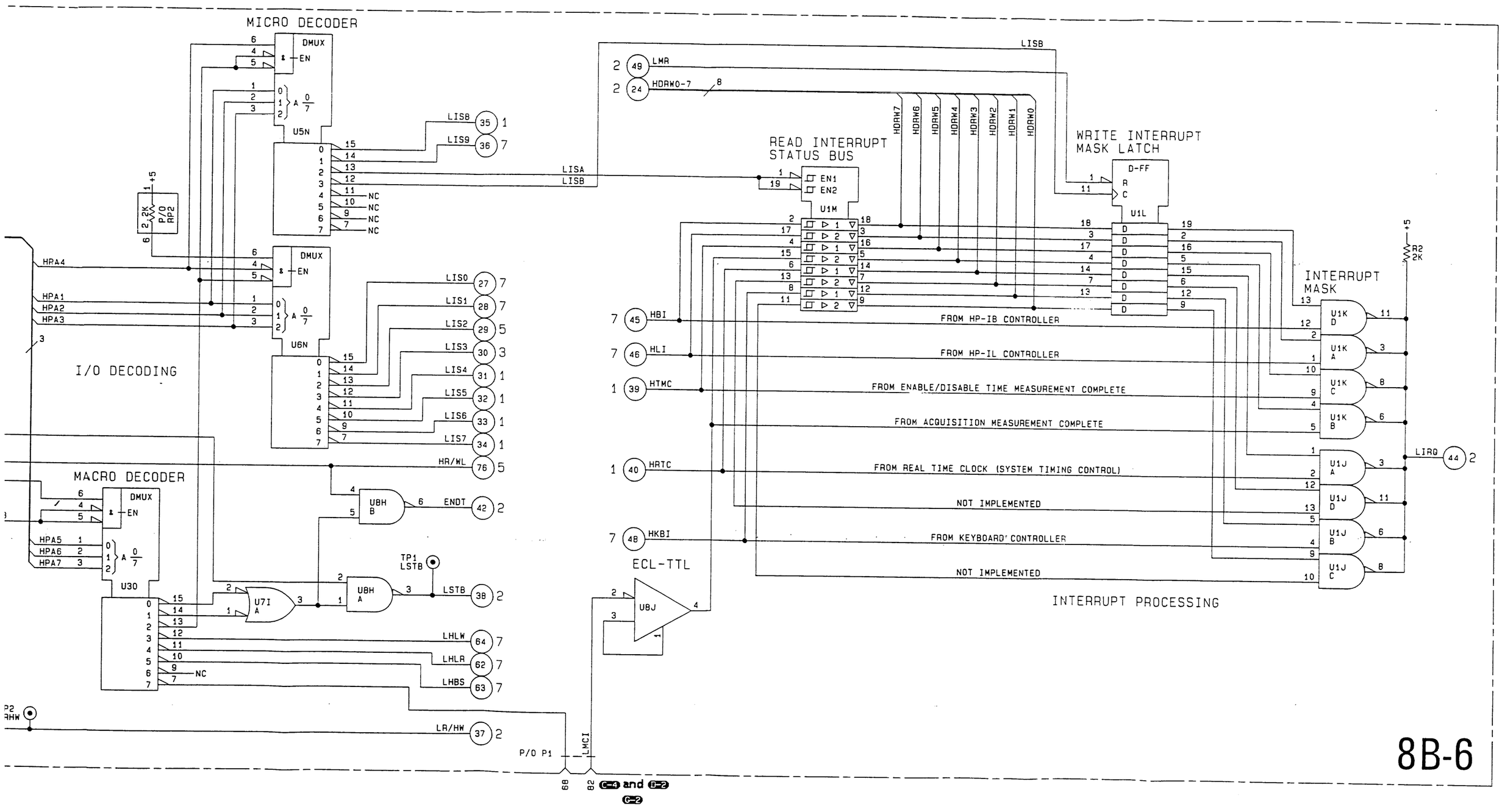


PARTS ON THIS SCHEMATIC

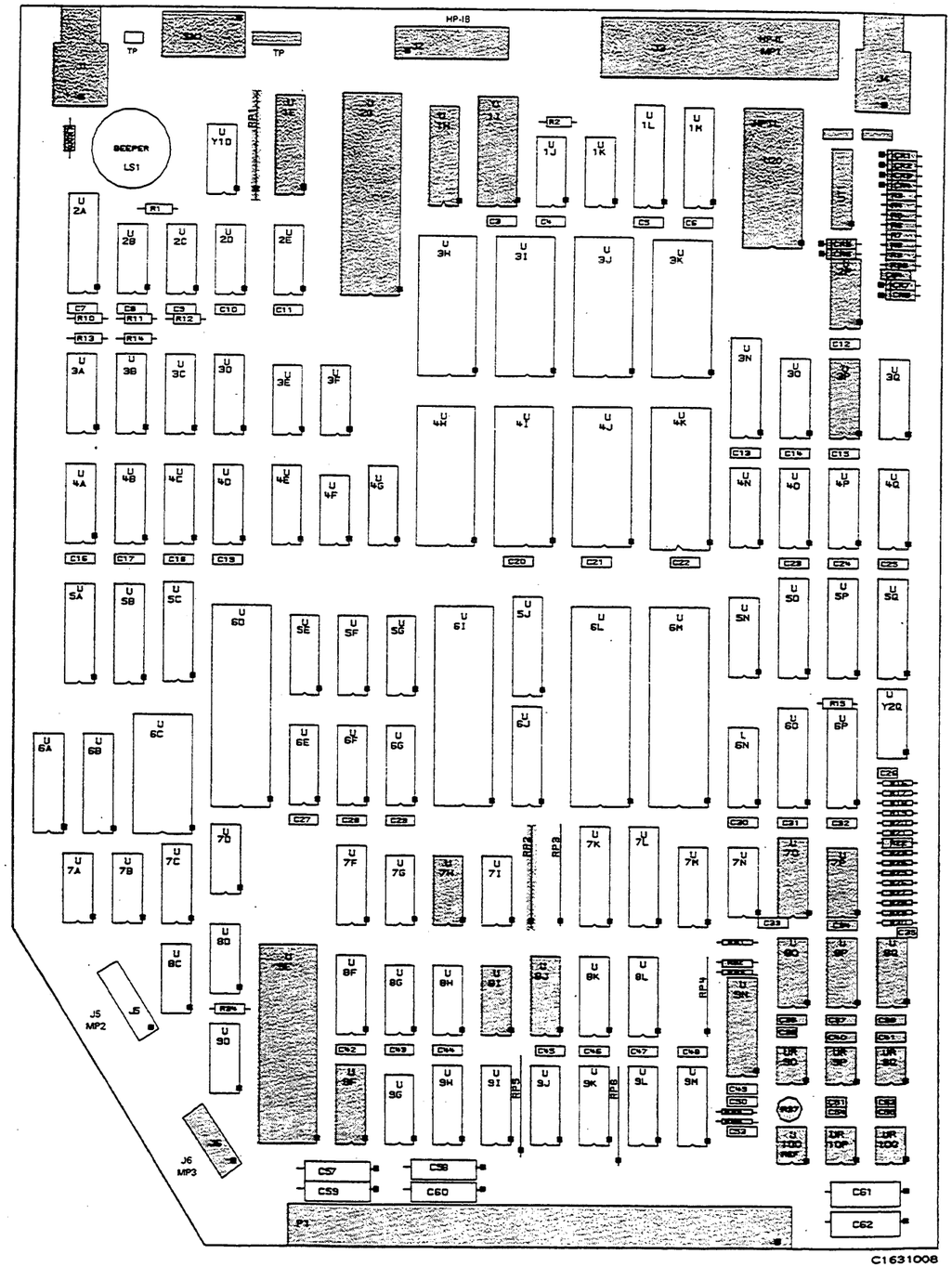
R2 RP2 TP1,2 U1J-M,30,5N,6N, U7H,I,8H,J,9H	



C-4 and D-2
C-2

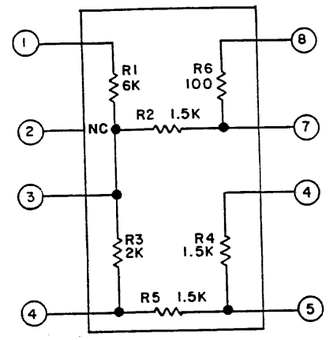


Schematic 8B-6
I/O Decoding, Interrupt Processing
8B-45



Component Locator for Schematic 8B-7

NOTE 1: DIAGRAM FOR UR9O-Q, UR10P,Q



NOTE 2

U2P IS DESIGNATED AS U3P ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

NOTE 3

SOME HP-IL OUTPUT CIRCUITRY IS LOCATED ON SMALL SUB-BOARDS ON SOME CPU BOARDS. C64, CR5-7, AND R38 WERE ADDED TO THE 01630-66512 AND LATER BOARDS.

NOTE 4

THIS CONNECTION IS NOT MADE ON PC BOARDS 01630-66503, 66512, 66519, AND 66522.

NOTE 5

THIS PULL-UP DOES NOT EXIST ON CPU BOARD 01630-66503.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
+5 GND	20 10	U1E,1H
+5 GND	14 7	U3P,7H,8I
+5 −5.2 GND	9 8 16	U8J
+12 −12 GND	20 17 10	U9N
+5 GND	22 11	U1I
+5 GND	40 20	U2G,9E
+12 −12 GND	13 3 14	U70
+12 GND	3 12	U7P
+12 −12	4 11	U80,8P,8Q
+5 GND	16 8	U9F
+12 GND	2 4	U100

PARTS ON THIS SCHEMATIC

C1,2,32,34,36−41, 49−56 CR1−4 J1−4,6 P/O P1 R3−9,22−25,27−29, 32,33,35−37 RP1,2 SW1	TP4 UR9D,9O,9Q,10P,10Q UT1 U1E,H,I,2G,O,3P, U7H,O,P,8I,J, U8O−Q,9E,F,N, U10O

P/O A3 CPU
HP-IB CONTROL, THRESHOLD REFERENCE
AND DRIVERS

HP-IB CIRCUITRY

SYSTEM STATUS SWITCHES

SWITCH STATUS BUFFER

1=OPEN
0=CLOSED

SW1

U26 HP-IB CONTROLLER

HP-IB TRANSCEIVERS

DATA

COMMANDS

FOR U2P SEE NOTE 2

FOR U2P SEE NOTE 2

TO / FROM KEYBOARD

J8

KBR1 KBR2 KBR3 KBR4 KBR5 KBR6 KBC7 KBC6 KBC5 KBC4 KBC3 KBC2 KBC1 KBC0

P/O J1

P/O J4

C63 0.1UF

BNC OUTPUTS

P/O P1

ECL-TTL

KEYBOARD SCANNING

ROW DMUX

SEE NOTE 4

USE KEYBOARD CONTROLLER

U20 HP-IL CONTROL

SEE NOTE 5

SEE NOTE 2

FOR HP-IL OUTPUT CIRCUITRY SEE NOTE 3

INPUT

OUTPUT

UT1

U1OO VOLTAGE REGULATOR

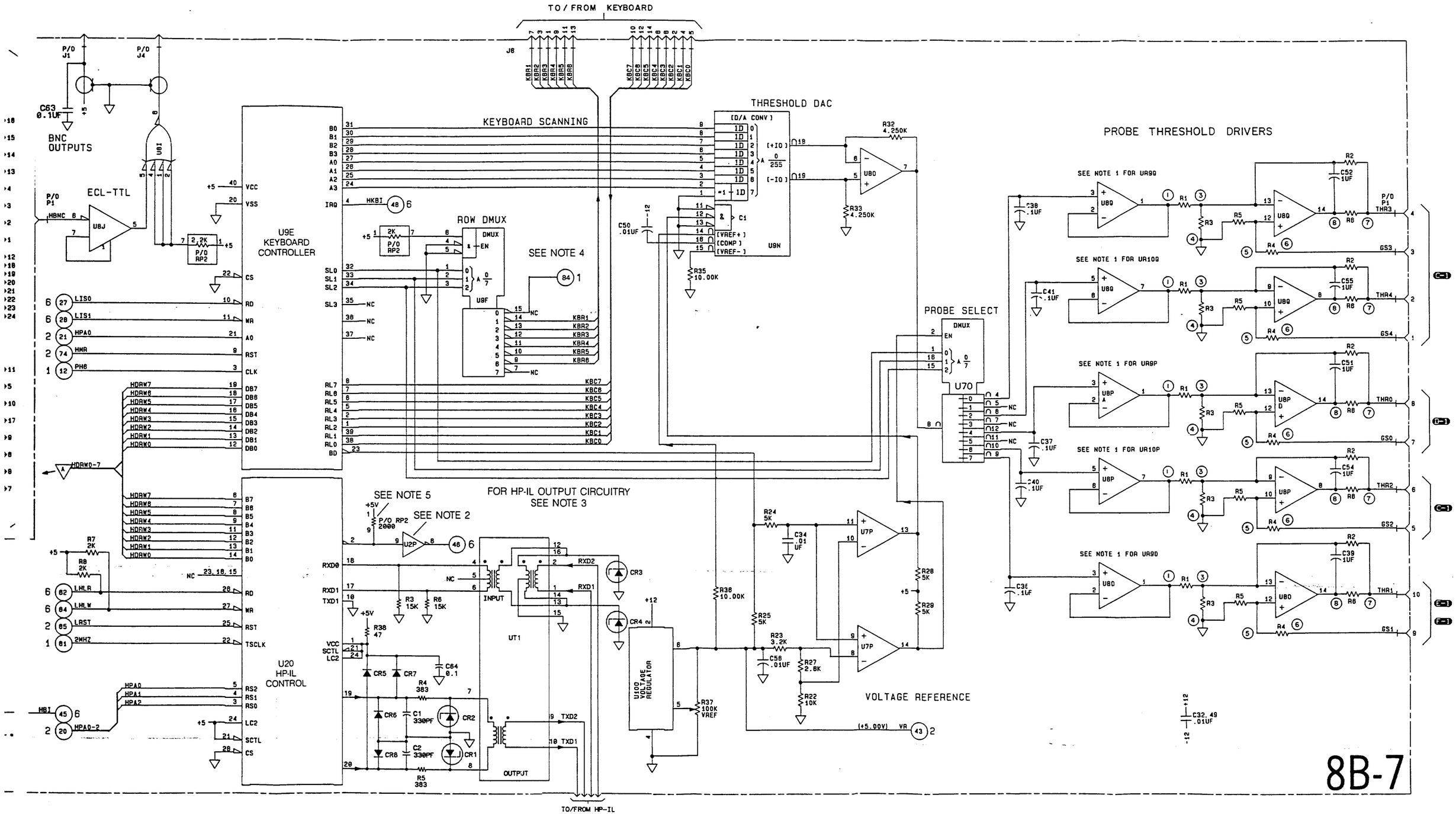
C50 .01UF

R35 10.00K

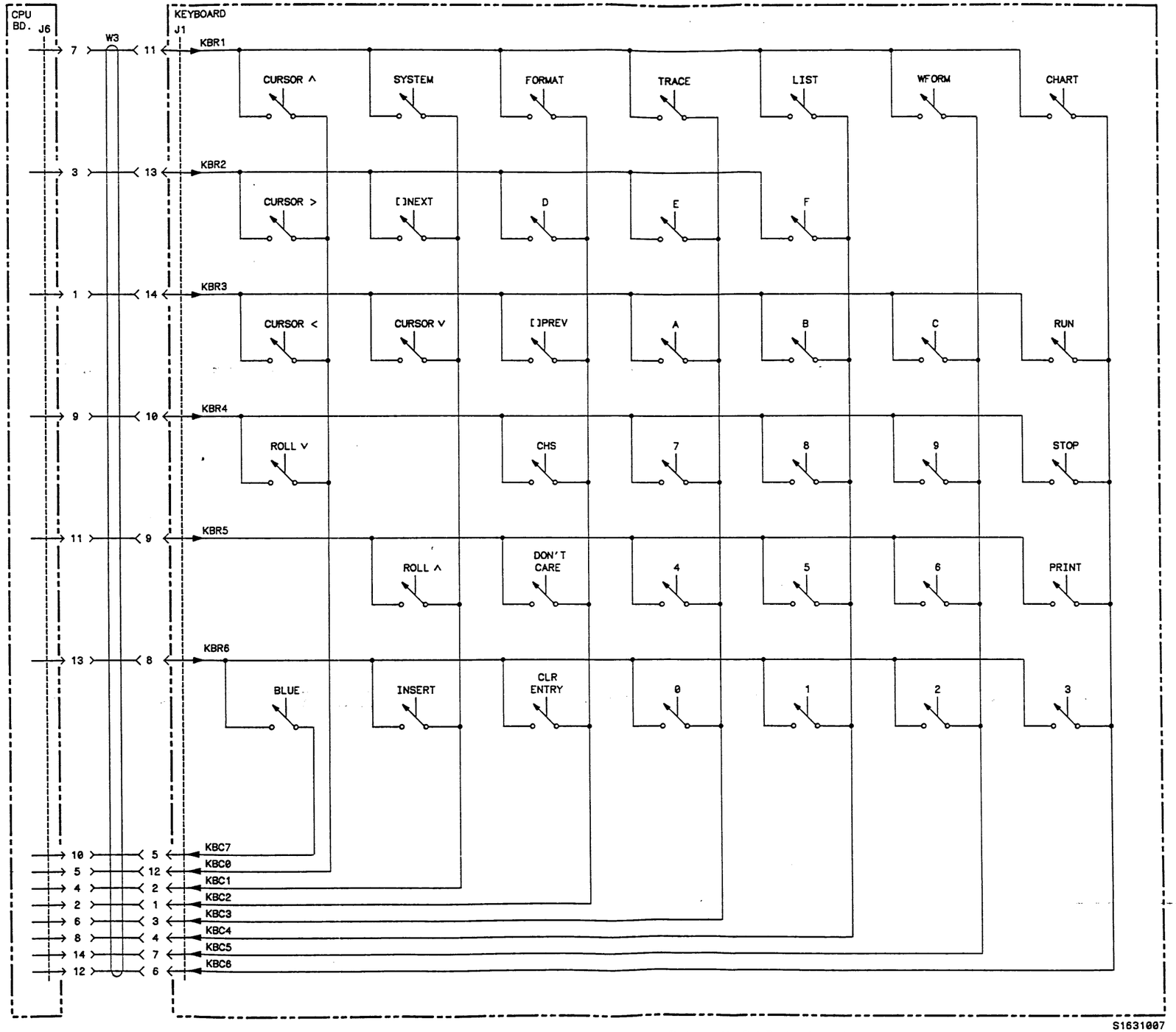
R36 10.

R37 100K VREF

TO/FROM HP-IL



Schematic 8B-7
HP-IB Control, Threshold Reference and Drivers
8B-47



Schematic 8B-8. Keyboard

Service Group 8C Table of Contents

Paragraph		Page
8C-1.	Introduction	8C-1
8C-2.	State Block Theory	8C-1
8C-3.	Theory of Operation	8C-2
8C-4.	State Pods & Pod Interface	8C-2
8C-5.	Acquisition Memory	8C-2
8C-6.	Memory Address Counter	8C-2
8C-7.	Wrap-Around Flip-Flop	8C-2
8C-8.	Pattern Recognition RAM	8C-4
8C-9.	Sequencer	8C-6
8C-10.	Arm Control Flip-Flops	8C-8
8C-11.	State/Timing Flip-Flop	8C-8
8C-12.	Tracepoint One-Shot	8C-8
8C-13.	BNC Latch	8C-8
8C-14.	Poststore Counter	8C-9
8C-15.	Occurrence Counter and Load Latches	8C-10
8C-16.	Clock Selection	8C-12
8C-17.	Clock Delay and Width Control	8C-14
8C-18.	Clock Control	8C-15
8C-19.	CPU Interface	8C-15
8C-20.	Mnemonics	8C-16

List of Illustrations

Figure		Page
8C-1.	State and Timing Acquisition System	8C-3
8C-2.	State Pattern Recognition RAM	8C-5
8C-3.	Acquisition Pattern Recognition	8C-5
8C-4.	Sequencer	8C-6
8C-5.	Trace Format Example	8C-7
8C-6.	State Diagram Example	8C-7
8C-7.	Sequencer Signals	8C-7
8C-8.	Poststore Counter	8C-9
8C-9.	Occurrence Counter and Load Latches	8C-10
8C-10.	Sequence Flow Chart	8C-11
8C-11.	J, K, or L Clock Path	8C-12
8C-12.	Clock Selection	8C-13
8C-13.	Clock Delay and Width Control	8C-14
8C-14.	State Pod	8C-19

List of Tables

Table		Page
8C-1.	Mnemonics	8C-16

List of Schematics

Schematic		Page
8C-1.	Pods 2, 3, and 4 Interface, Counter-Latches	8C-21
8C-2.	MAC, Acquisition RAM	8C-23
8C-3.	Pattern Recognition RAM	8C-25
8C-4.	Measurement Complete, Tracepoint Gate	8C-27
8C-5.	Poststore and Occurrence Counters	8C-29
8C-6.	Clock Selection	8C-31
8C-7.	Clock Delay and Width	8C-33
8C-8.	State Master CPU Interface	8C-35

SERVICE GROUP 8C
STATE MASTER

8C-1. INTRODUCTION

The following paragraphs highlight the features of the State Acquisition Board.

1. SAMPLING. The state board accepts 27 channels from three pods. The timing master and optional timing slave may also be run in state mode, adding either 8 or 16 more state channels.

2. SAMPLE RATE. Sampling is synchronous with the user system in a state analysis system. The maximum sample rate for a single clock is 25 MHz.

3. PATTERN RECOGNITION. The analyzer may be programmed before a run to look for a combination of highs or lows on the parallel 27-bit input word. The logic analyzer will allow up to four different patterns to be specified.

4. SEQUENCE. The operator may specify that a particular sequence of patterns must occur before the analyzer can trigger. Up to four sequence terms are allowed.

5. OCCURRENCE. The operator may specify that the last sequence pattern must repeat a certain number of times. Up to 59999 occurrences can be specified.

6. TRACEPOINT. Trigger plus delay--A valid trigger pattern has been detected and any qualifications such as delay, occurrence, and sequence have been satisfied.

7. POSTSTORE. The operator may specify tracepoint position in memory. The choices are Start, Center, or End.

8C-2. STATE BLOCK THEORY (See Figure 8C-1)

POD INTERFACE. Input data from up to three 9-bit pods is taken at the user's sample rate. Each pod has its own clock, one or more of which may be chosen as the synchronous state sample clock.

ACQUISITION MEMORY. Width is 28 to accommodate the 27 input data channels--one bit in each word is allocated for possible tracepoint. Depth is 1024 on each channel.

MEMORY ADDRESS COUNTER. Holds the address of the next location in acquisition memory to be filled. The CPU uses the memory address counter to find the position of tracepoint in memory.

PATTERN RECOGNITION RAM. Input width is 27 bits and output width is 4 bits. The CPU pre-loads the RAM so that a particular 27-bit data pattern will address a 4-bit word corresponding to one of the four specified patterns.

SEQUENCER. Determines the next analyzer state after receiving current status from the occurrence counter and pattern recognition RAM. The CPU preloads the sequencer RAM to implement the State Trace Specification sequence.

CLOCK SELECTION. Synchronizes data sampling to one or more user clocks. Selects edges and master/slave clocking for multiplexed buses.

OCCURRENCE COUNTER. Counts pattern occurrences. The counter is preloaded by the CPU with up to 59999 occurrences. Terminal count goes to the sequencer.

POSTSTORE COUNTER. Determines tracepoint position in memory. The counter is preloaded by the CPU with the amount of memory to be filled with new data after tracepoint.

CLOCK DELAY/WIDTH CONTROL. Allows adjustment of the state analyzer internal write cycle timing.

CPU INTERFACE. Allows the CPU to read the memory address counter, the poststore counter, and stored data. Also enables the CPU to clock various state analyzer functions.

8C-3. THEORY OF OPERATION

8C-4. State Pods and Pod Interface (see schematic 8C-1)

Three pods (2, 3, 4) each supply nine channels and one clock to the line receivers. The operator may choose any one--or an ORed combination--of the three clocks (J,K,L) to synchronize incoming data.

Twenty-seven channels are allocated for state analysis alone. Additionally, the master and optional slave Timing Boards can each supply eight channels, making possible a total width of 43 State channels.

The nine channels from each pod go from line receivers into 4-bit counters (U2B, U2C, 2E-2I). The counters act as sample latches during a run, or as binary counters for programming Pattern Recognition RAM before a run.

The CPU board supplies ground sensing and precision thresholds to each pod via the motherboard.

8C-5. Acquisition Memory (see schematic 8C-2)

The acquisition RAM is organized as 28 bits wide by 1024 words deep--27 bits for data storage, with 1 bit in each word to indicate tracepoint location. The 27 data channels are written into memory in parallel. When the write signals (LWE1,2) are false, or high, the CPU may read the RAM.

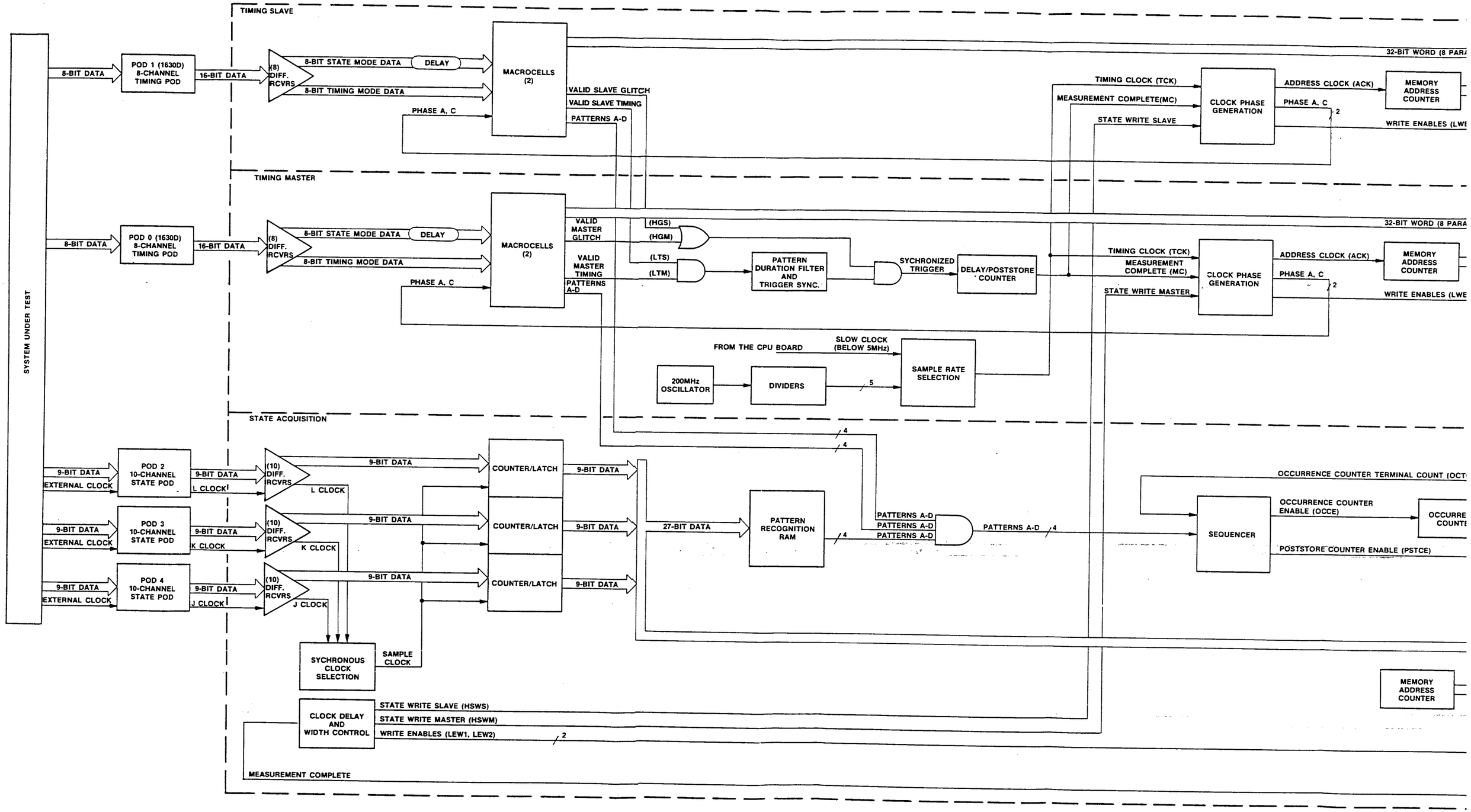
An octal latch (U3N) selects 1K x 8 blocks of RAM for reading, or all blocks for writing.

8C-6. Memory Address Counter (see schematic 8C-2)

The MAC consists of three 4-bit counters of which ten bits are used. The CPU reads the MAC to determine tracepoint position in memory.

8C-7. Wrap-Around Flip-Flop (see schematic 8C-2)

The Wrap-Around Flip-Flop signals that memory has been filled at least once when it receives terminal count from the MAC. This tells the CPU that the memory is filled with valid data.


TIMING SLAVE
TIMING MASTER
STATE ACQUISITION
SYSTEM UNDER TEST
8-BIT DATA
POD 1 (1630D) 8-CHANNEL TIMING POD
16-BIT DATA
(8) DIFF. RCVRS
8-BIT STATE MODE DATA
DELAY
8-BIT TIMING MODE DATA
PHASE A, C
MACROCELLS (2)
VALID SLAVE GLITCH
VALID SLAVE TIMING
PATTERNS A-D
32-BIT WORD (8 PARA
TIMING CLOCK (TCK)
MEASUREMENT COMPLETE(MC)
STATE WRITE SLAVE
CLOCK PHASE GENERATION
ADDRESS CLOCK (ACK)
PHASE A, C
2
MEMORY ADDRESS COUNTER
WRITE ENABLES (LWE
POD 0 (1630D) 8-CHANNEL TIMING POD
VALID MASTER GLITCH
(HGS)
(HGM)
VALID MASTER TIMING
(LTS)
(LTM)
PATTERNS A-D
PATTERN DURATION FILTER AND TRIGGER SYNC.
SYCHRONIZED TRIGGER
DELAY/POSTSTORE COUNTER
STATE WRITE MASTER
MEASUREMENT COMPLETE (MC)
FROM THE CPU BOARD
SLOW CLOCK (BELOW 5MHz)
200MHz OSCILLATOR
DIVIDERS
5
SAMPLE RATE SELECTION
POD 2 10-CHANNEL STATE POD
POD 3 10-CHANNEL STATE POD
POD 4 10-CHANNEL STATE POD
9-BIT DATA
EXTERNAL CLOCK
L CLOCK
K CLOCK
J CLOCK
COUNTER/LATCH
27-BIT DATA
PATTERN RECOGNITION RAM
4
PATTERNS A-D
OCCURRENCE COUNTER TERMINAL COUNT (OCT
OCCURRENCE COUNTER ENABLE (OCCE)
POSTSTORE COUNTER ENABLE (PSTCE)
SEQUENCER
SYCHRONOUS CLOCK SELECTION
SAMPLE CLOCK
CLOCK DELAY AND WIDTH CONTROL
STATE WRITE SLAVE (HSWS)
STATE WRITE MASTER (HSWM)
WRITE ENABLES (LEW1, LEW2)
MEASUREMENT COMPLETE

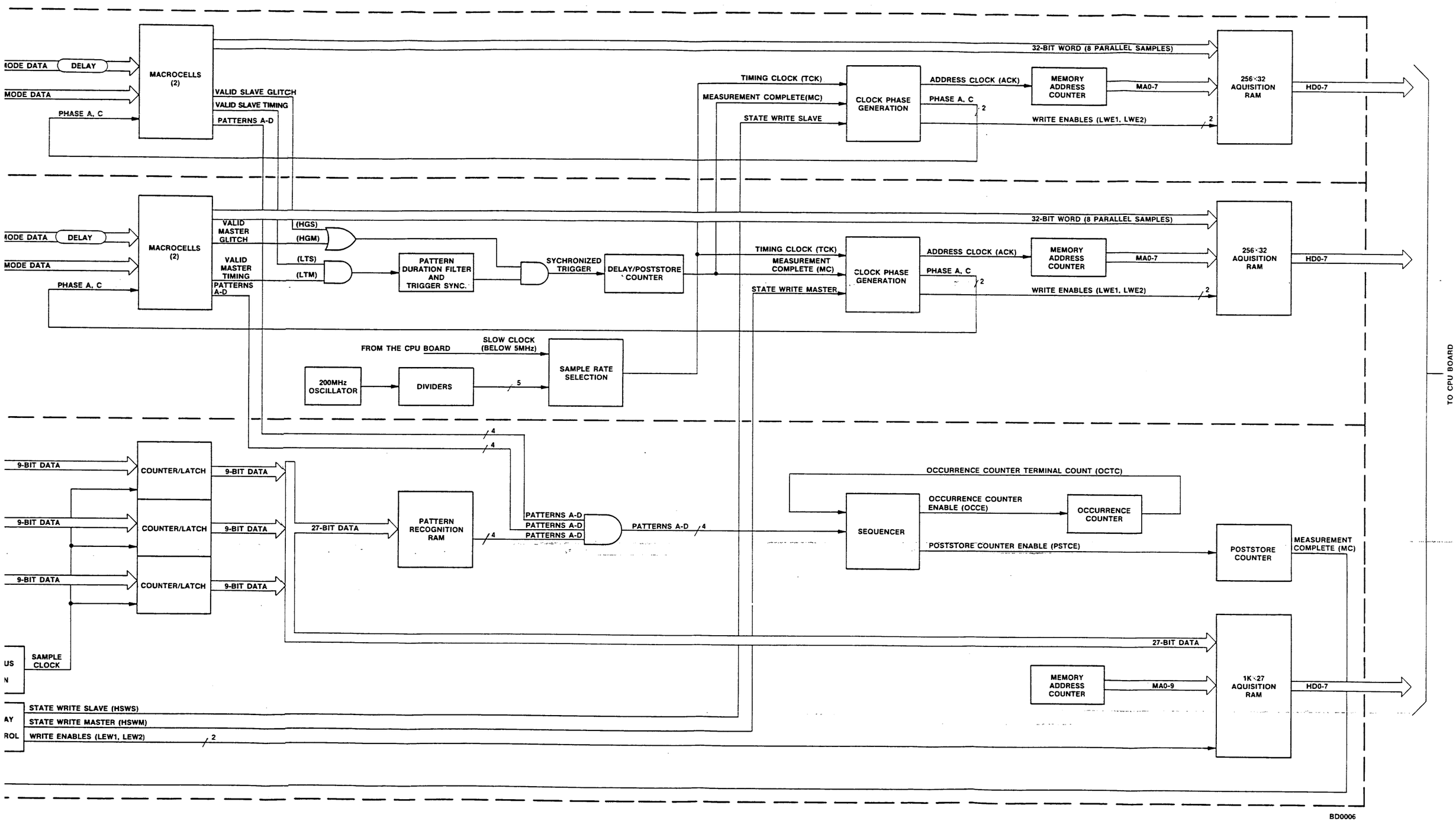


Figure 8C-1. State and Timing Acquisition System

8C-8. Pattern Recognition RAM (see schematic 8C-3)

Pattern Recognition RAM consists of three 256 x 4 ECL RAM chips and one 16 x 4 RAM chip connected in parallel, allowing an addressing width of 28 bits. Input width is 27 bits--since one of the address lines is not used--and output width is 4 bits. The 27-bit incoming sample from the data pods addresses Pattern Recognition RAM. The four bits from each RAM location go out over the pattern lines, LPAT A-D, to the sequencer.

Before a run, the CPU pre-loads each 4-bit RAM location. During a run, when a RAM location is addressed by the incoming sample, its four bits are output on the four pattern lines A-D. When one or more of these four bits is low, the corresponding pattern line will be driven low. A 27-bit incoming data sample that forms a pre-specified pattern of highs, lows, and don't-cares will address one of those RAM locations that was pre-loaded with at least one low.

For example, if the eight input sample bits to a single RAM chip are 00000000, then the first location will be addressed. If the four bits stored in that location are 1100, then pattern output lines A and B--corresponding to the two lows--from that RAM will try to go low.

However, as shown in figure 8C-2 each of the four output bits from each pattern RAM are ECL wire ANDed (ECL outputs may be connected together like open-collector TTL outputs). Thus, a pattern line can be active only when all four RAMs have a low on the same output.

As shown in figure 8C-3, four pattern lines also come into the state board from the timing master and timing slave boards. When the timing boards are in the state mode, their macrocells act like pattern recognition RAM. The four pattern lines from the timing boards are wire ANDed with the four state pattern lines. Thus, for a single pattern line to be driven low, the two timing boards and all four RAM chips on the state board must agree. (When a timing board is not in the state mode, its pattern lines will be normally low.)

If more than one of the pattern lines is low at the same time, the sequencer will select the one required for the next analyzer state according to the trace specification.

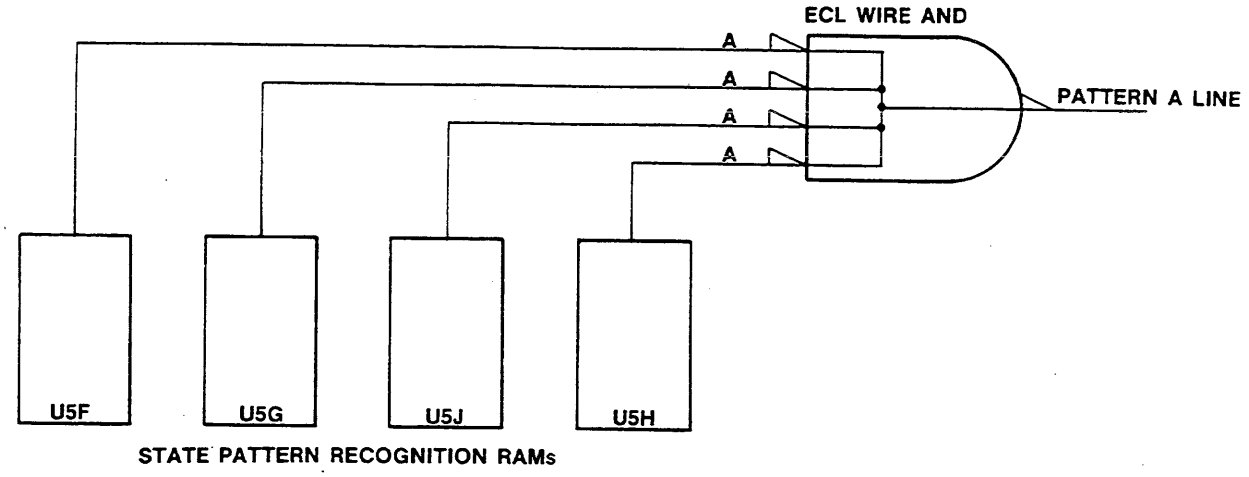


Figure 8C-2. State Recognition RAM

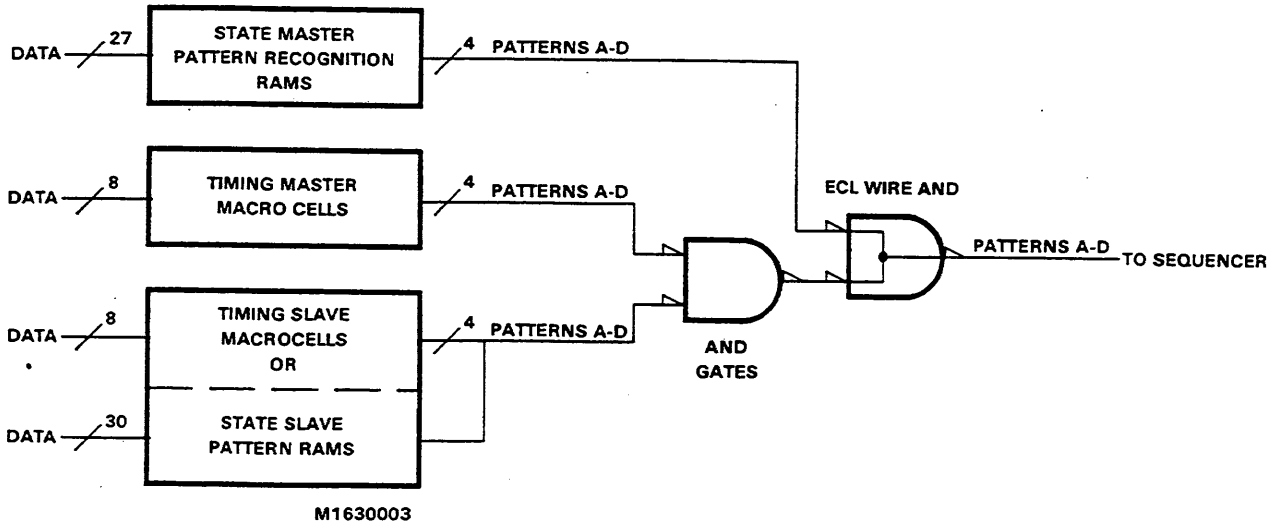


Figure 8C-3. Acquisition Pattern Recognition

8C-9. Sequencer (See schematic 8B-4)

The CPU programs the sequencer to determine the next state the analyzer will enter. Eight input control bits represent the Current State. Given a set of Current input bits, the sequencer emits six output bits representing the Next State.

The heart of the sequencer is a 4-bit binary counter (U6E) and a 256 x 4 RAM (U5E). Before a run, the counter addresses RAM locations for loading by the CPU. The CPU pre-loads the RAM locations with sequences which will occur when those locations are addressed by the eight input control bits. During a run, the counter acts as a latch for the 2-bit Current State.

Tracepoint is when: (1) the occurrence counter is enabled, and (2) it reaches terminal count. Tracepoint indicates that the specified patterns have been found, and that the last pattern has occurred the correct number of times. The ANDing of Occurrence Counter Enable (OCCE) and Occurrence Counter Terminal Count (OCTC) at U7B produces Tracepoint (TP), which is latched in the sequencer latch (U6E).

SEQUENCER INPUTS. The eight bits that drive the sequencer are:

a. Patterns A to D from Pattern Recognition RAM.
b. HOCTC - Occurrence Counter Terminal Count.
c. HTPL - Trace Point Latched from the sequencer latch.
d. CS0,CS1 - The 2-bit code representing Current State.

SEQUENCER OUTPUTS. The six sequence outputs are:

a. NS0,NS1 - The 2-bit code representing Next State.
b. LOCCE - Occurrence Count Enable, which increments the Occurrence Counter.
c. LSQ/TP - Store Qualified or Trace Point, which increments the Memory Address Counter, allowing incoming data to be stored.
d. LPSTCE - Post Store Count Enable, which enables the Poststore Counter.
e. HSQ3 - Sequence State 3, which the CPU uses for time interval measurements.

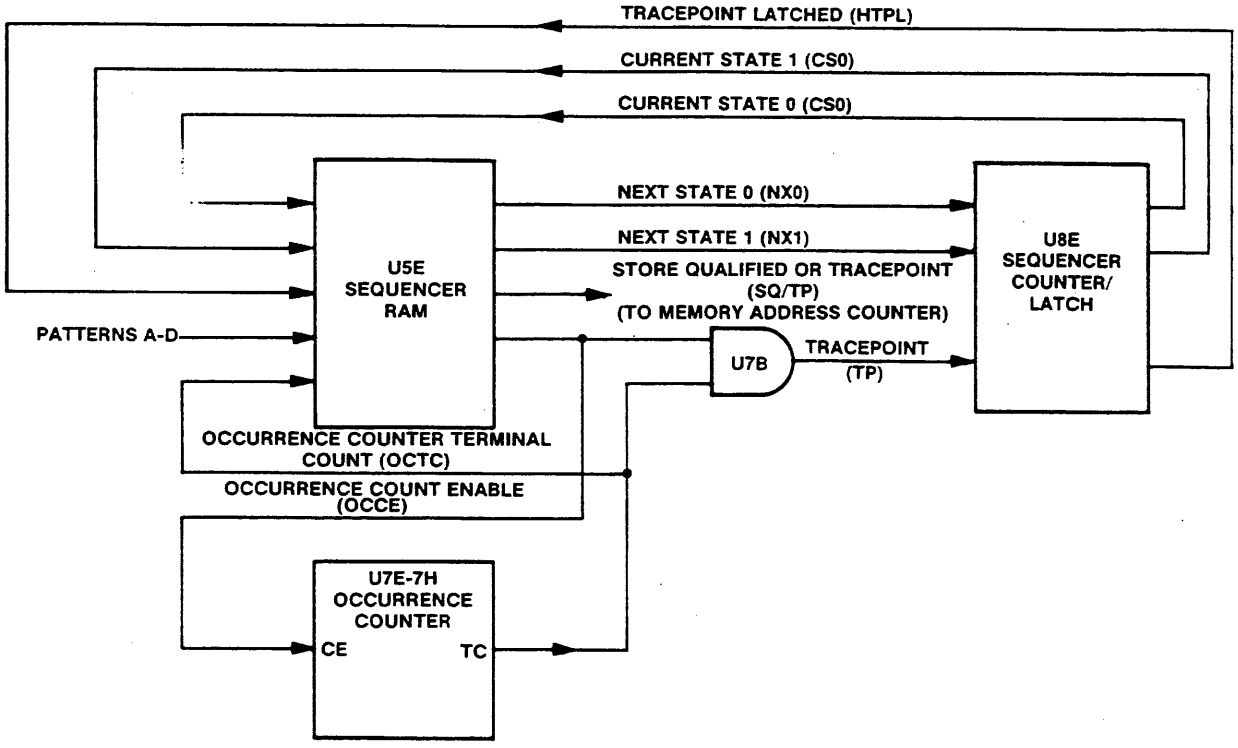


Figure 8C-4. Sequencer

SEQUENCER STATES	TRACE FORMAT
	[single] Trace Mode
	in sequence
0	find [a]
1	then [b]
2	then [c]
	then [start] Trace at [0010] Occurrences of
3	[D] then store [allstates]
0	Sequence Restart on [no state]

Figure 8C-5. Trace Format Example

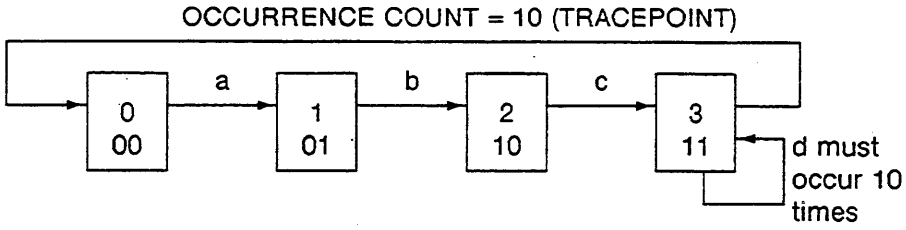


Figure 8C-6. State Diagram Example

SEQUENCER STATES	SEQUENCER INPUTS								SEQUENCER OUTPUTS			
	CS1	CS0	TPL	TC	[a]	[b]	[c]	[d]	NX1	NX0	OCCE	SQTP
0	0	0	0	0	0	0	0	0	0	0	0	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	0	0	1	0	0	0	0	1	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	0	1	0	0	0	1	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
2	1	0	0	0	0	0	1	0	1	1	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
3	1	1	0	0	0	0	0	1	1	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	1	1	0	0	0	0	0	1	1	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	1	1	1	1	0	0	0	1	0	0	1	1
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
0	0	0	1	0	0	0	0	0	0	0	0	1

d occurs n-1 times

d occurs 10 times

Figure 8C-7. Sequencer Signals

Figure 8C-5 shows an example of sequencer action for one trace format. The operator has directed the analyzer to find pattern A, then pattern B, then pattern C. If these patterns occur in the proper order, the analyzer will then look for ten occurrences of pattern D. If these specifications are satisfied, tracepoint will occur. The analyzer will store the first three sequencer states, tracepoint, and 1K of subsequent data. Tracepoint will be seen on line 0000 at the beginning of the display.

The state diagram, figure 8C-6, shows the flow from one sequencer state to the next. The 2-bit Current State code (CS0,CS1) indicates the four possible sequencer states. If one of the terms--for example, C--were not specified in the trace format, the sequencer would jump from state 1 to state 3.

Figure 8C-7 shows the sequencer input and output signals when the events specified in the above trace format occur. The sequencer Current State is given by CS0 and CS1. As can be seen by the Store Qualified signal (SQ/TP), the first three patterns are also stored by the analyzer, even though tracepoint has not yet occurred.

8C-10. ARM CONTROL FLIP-FLOPS (U1K,7J). These control the arming of the State analyzer which may either arm or be armed by Timing. The output, LARMEN, enables Occurrence Counter terminal count to the sequencer, and the Next State outputs from the Sequencer. Without occurrence counter terminal count, tracepoint cannot occur.

8C-11. STATE/TIMING Flip-Flop (U1K). Selects either State or Timing as the master. When state is the master, both inputs to the AND gate U8D will be high when tracepoint occurs, allowing the state analyzer to arm the timing analyzer via the motherboard (P85).

8C-12. TRACEPOINT ONE-SHOT (U6J,3M). Generates a 20 ns pulse when tracepoint occurs. This is provided to the BNC output connector.

8C-13. BNC LATCH (U8C). Selects one of four different sequencer outputs to go out to the external BNC connector:

Tracepoint Pulse (U8C-5)	A 20ns negative-going pulse when tracepoint occurs.
Timer (U8C-4)	Low level on Current State 3 (CS0,CS1=1); This is equivalent to HSQ3, which is sent to the CPU for the Overview Time measurement.
Tracepoint High (U8C-12)	This BNC output will stay low as long as the analyzer is looking for tracepoint, then go high until another measurement is begun.
Tracepoint Low (U8C-10)	This BNC output will stay high as long as the analyzer is looking for tracepoint, then go low until another measurement is begun.

8C-14. Poststore Counter (See schematic 8C-5)

The state analyzer provides three different measurement techniques:

Start-Trace — Memory is completely filled with new data after tracepoint; tracepoint is displayed at the beginning. (If a sequence is specified, the sequence patterns--up to three--will be stored before tracepoint.)

End-Trace — Displayed memory consists entirely of pre-tracepoint data; tracepoint is displayed at the end.

Center-Trace — Displayed memory consists of half pre-tracepoint data and half posttracepoint data; tracepoint is displayed in the center.

The poststore counter counts out the amount of data to be stored after a start, center, or end-trace measurement. The poststore counter is enabled by the sequencer (LPSTCE) when tracepoint occurs. The counter is then incremented on every store-qualified state following tracepoint. The following signals must be true:

LTPL (U6F-13) — Tracepoint Latched: occurs at occurrence counter terminal count and occurrence counter enable; and stays set.

LSQ/TP (U6F-12) — Store-qualified or Tracepoint: indicating that data is available for memory storage. This will always be true out of the sequencer when more data is to be post-stored.

During a measurement, the CPU reads the poststore counter's output to determine the number of words to completion of the state measurement. Terminal count from the poststore counter goes to the sequencer where it enables End of Measurement (HEOM) and Measurement Complete (LMC), which stop the data collection process by shutting down the write strobes and the memory address counter, respectively. Measurement Complete signals the CPU via interrupt that the memory is full, and the state measurement is complete.

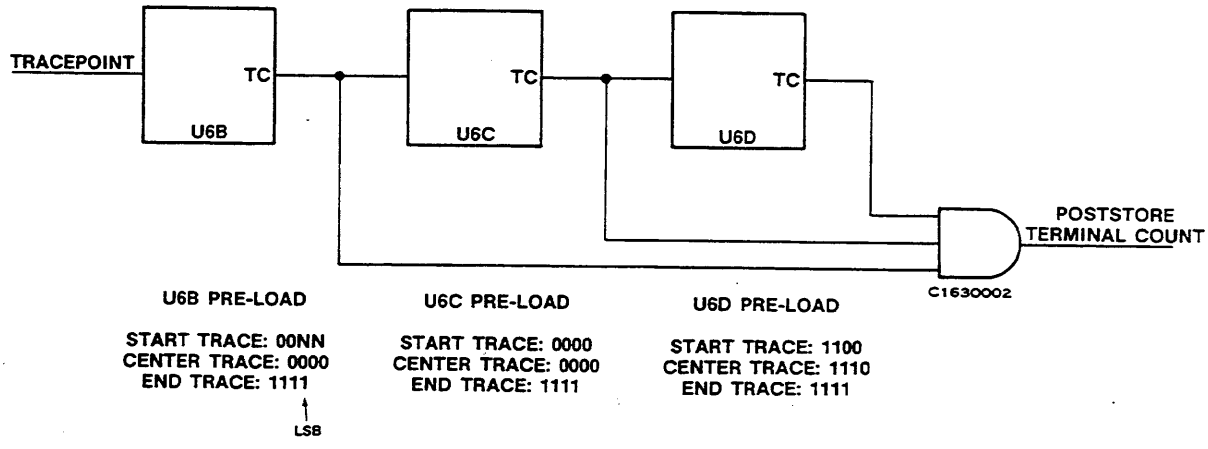


Figure 8C-8. Poststore Counter

8C-15. Occurrence Counter and Load Latches (see schematic 8B-5)

The occurrence counter (U7E-7H) counts repetitions of the last pattern to be found. Although up to four patterns may be specified, only the last pattern may have an occurrence specification.

When the operator specifies the pattern repetitions required to produce tracepoint, the CPU loads sequencer RAM to recognize that pattern, and presets the occurrence counter with the number of repetitions. Then, whenever that pattern occurs, the sequencer increments the occurrence counter. The sequencer enables the occurrence counter, clocked by the index clock (ICK), on every Occurrence Count Enabled state (LOCCE).

The sequencer is always restarted after every tracepoint. CPU Master Reset (HMR) presets the counter initially during operator setup. Whenever tracepoint occurs, the sequencer restarts, going to Sequence State Zero, and begins looking for the original sequence again.

Immediately after tracepoint is found, or before the sequencer is restarted, the next sequencer state will be 0. This is decoded by U7B as HPE, which reloads the occurrence counter to the original preset value. The Load Latches (U8E-8H) store the original occurrence counter preset value, allowing the counter to be reloaded after every tracepoint or sequence restart. This is so the tracepoint pulse can be continually sent out over the BNC after it is found the first time.

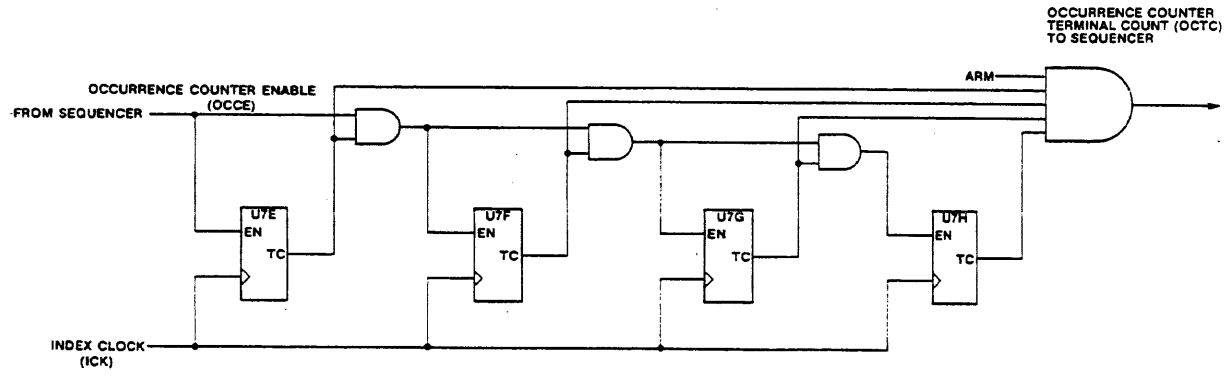


Figure 8C-9. Occurrence Counter and Load Latches

Tracepoint is the ANDing of LOCCE and LOCTC. That is, the occurrence counter must be enabled and it must reach terminal count for tracepoint to occur. All the other sequence terms must be satisfied before the sequencer can begin incrementing the occurrence counter. For example, if three other patterns were specified, the analyzer will look for these before counting the repetitions of the fourth pattern. An occurrence search is always the last process in a sequence. See figure 8C-10 below.

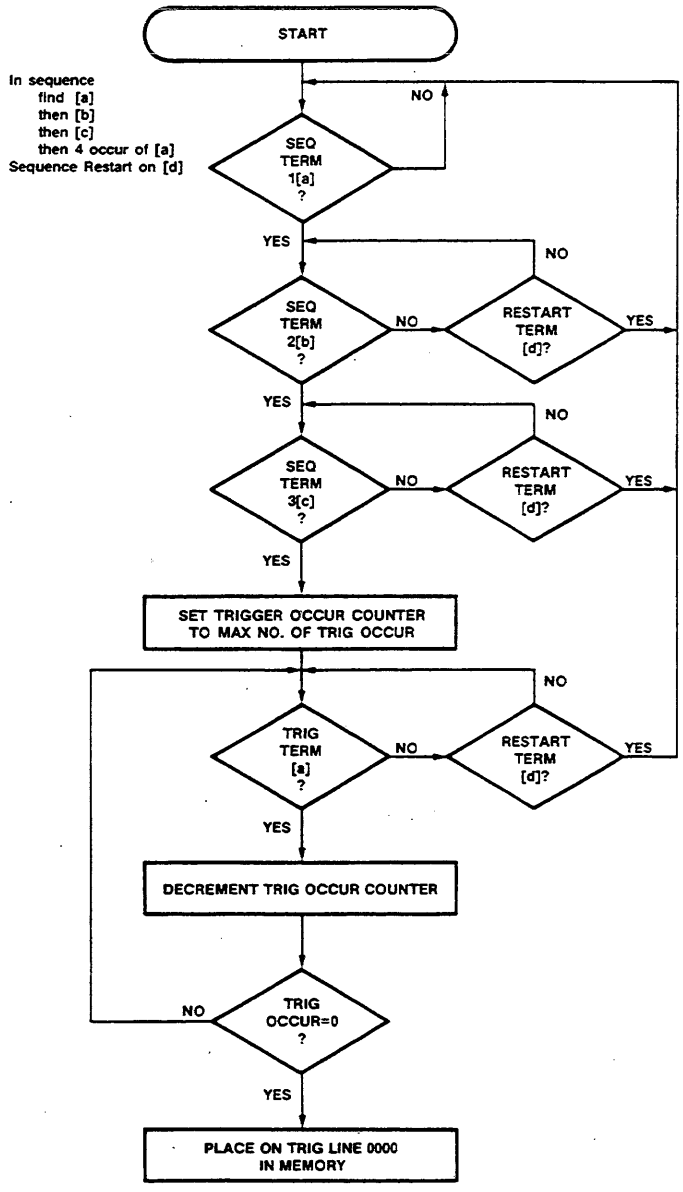


Figure 8C-10. Sequence Flow Chart

8C-16. Clock Selection (See schematic 8B-6)

A state analyzer is synchronous: sampling must be in step with the external clock from the system being analyzed.

Each of the three state pods (2,3,4) provides a clock input (L,K,J). The operator selects one or more of these clocks to synchronize the analyzer to the user system. Up to three clocks can be ORed together. For multiplexed user busses, one clock can be chosen as the master and another as the slave. Positive, negative, or both edges of any of these clocks may be selected.

As shown in figure 8C-11 below, each clock input is associated with four flip-flops whose D inputs are loaded by the CPU with the clock and edge selections. For example, if the J clock's negative edge is to be selected as master, the MJN input (U7M-10) will be programmed high. When the J clock transitions from high to low, the flip-flop output (U7M-15) will go high, causing the master one-shot to pulse and reset the flip-flop. The master clock will then consist of pulses whose positive edges are synchronized with the incoming negative J clock from Pod 2.

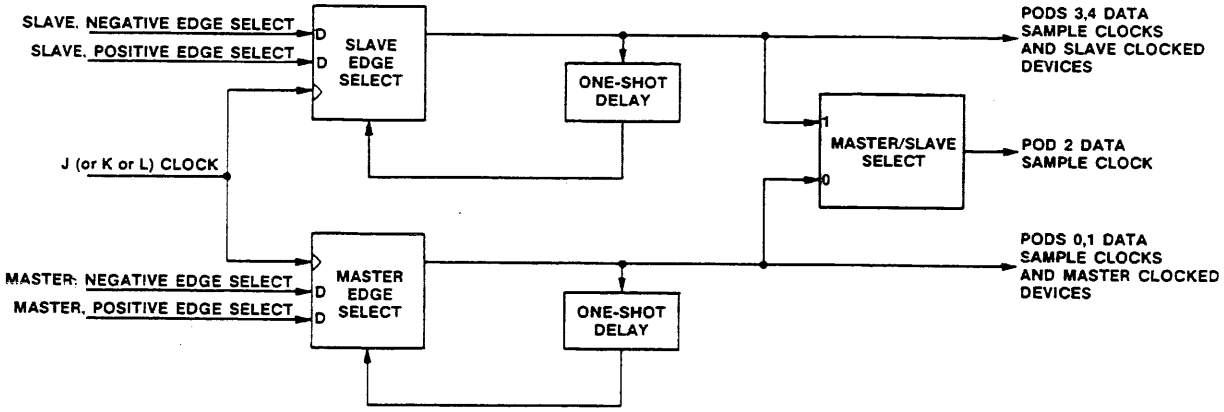


Figure 8C-11. J, K, or L Clock Path

As shown in figure 8C-12 below, any edge of any clock, or an ORed combination, may be chosen as the master or slave. The same clock may be both master and slave if different edges are used. In the non-multiplexed mode both master and slave clocks are identical.

The Delay/Width Control and the Timing Boards--when in the State Mode--are always clocked by the master clock. The Run/Halt Control and the Pod 3 and 4 data latches are always clocked by the slave clock. The Pod 2 data latches may be clocked by either the master or slave.

The Master-Slave Selector (8L) allows the Pod 2 data latches (U2B,2C,2D) to be clocked by the master or the slave clock selections.

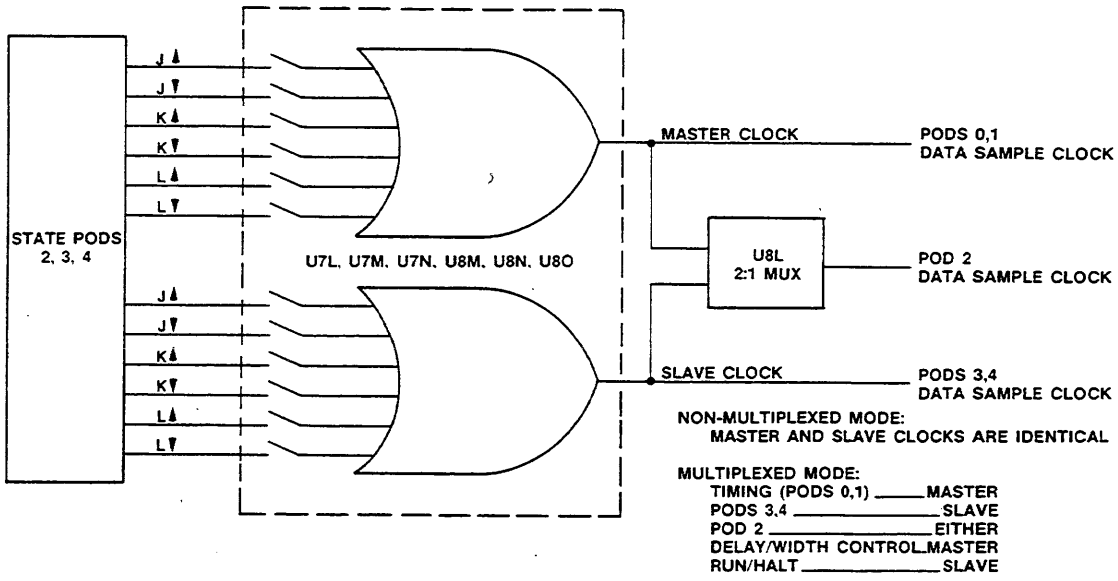


Figure 8C-12. Clock Selection

8C-17. Clock Delay and Width Control

(see schematic 8B-7)

The master clock (MCK) from the clock selector is shaped and delayed by two one-shots, which make up the heart of this circuit.

Clock delay is varied in the Delay One-Shot (U5L,5M). The output of the delay one-shot is then fed to a Width One-Shot (U5M,5N), which adjusts clock width.

Since both circuits work the same, only the delay one-shot will be described. An ECL output must be pulled down to produce a low. The pulldown for flip-flop U5L-2 is the resistor network R7 and the adjustable R5. Capacitor C4 has a quick charge path through the flip-flop on high- going signals, but must charge through the resistor network for lows. The delay for low-going signals is therefore adjustable.

Figure 8C-13 shows the timing relationship for the circuit. Since disconnected ECL inputs are internally pulled low, the D input is always low. In this type of flip-flop, D is clocked on a positive transition and S is active high. Because of the delay caused by the capacitor, the flip- flop cannot go low immediately. When it does go low the inverter, which has positive feedback, sets the flip-flop again for the next cycle.

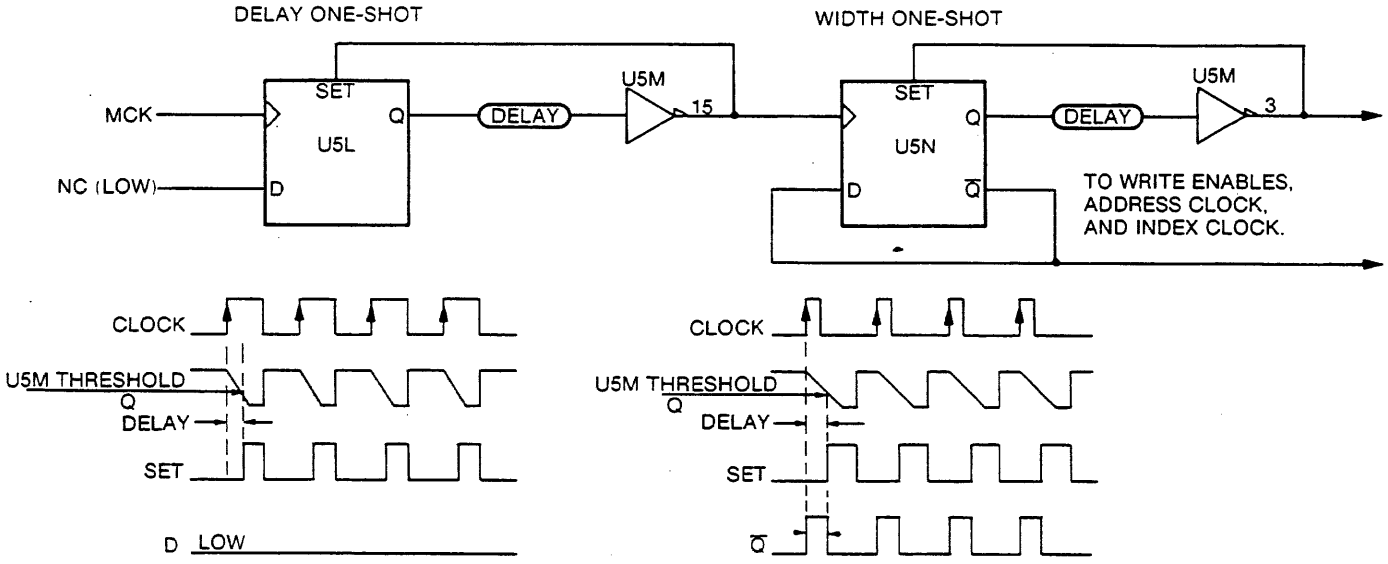


Figure 8C-13. Clock Delay and Width Control

8C-18. CLOCK CONTROL.

The shaped and delayed clock output eventually becomes four clocks:

ACK Address Clock.

ICK Index Clock.

LWE1, LWE2 Write Enable signals for acquisition memory.

ACK increments the memory address counter; ICK increments the occurrence, poststore counters, and the sequencer. The memory address and poststore counters are incremented only for store-qualified states, i.e., when data is to be stored in memory. During programming mode, the CPU substitutes its own clocks, HRDCK and HLDCK for ACK and ICK.

The Write Enable signals, LWE1 and LWE2, enable data acquisition RAM for the storing of data. Except for being delayed by 6ns to allow for RAM hold time, ACK and ICK are similar to the write enable signals.

LRUN, from the RUN/HALT FF (U5L), causes the pod interface counters (U2B- 2I) to go into the preset mode and act like latches, so they can latch in new probe data. When LRUN is high, the pod interface counters act as address counters, allowing the CPU to load Pattern Recognition RAM during programming mode.

8C-19. CPU Interface (See schematic 8B-8)

The CPU interface allows the CPU to read the contents of the memory address counter, the post-store counter, and state acquisition memory. Because the CPU loads the contents of state RAM into CPU RAM, it needs to reference data and tracepoint to these counters in order to correctly position the display. Counter and memory information is multiplexed onto the data bus by the Read Selectors (U5A-5D).

The CPU writes to the analyzer, providing clocks and enable signals for different analyzer functions, by means of the Write Strobe Demultiplexer (U1N). The following is a list of the clocks coming out of the demux:

BKCK Block Clock. Loads the data storage RAM block selector (U3N).

OCK1, 0CK2 Occurrence Clock. Loads CPU data into occurrence counter latches.

LCCK Counter Clock. Enables preset of occurrence and post-store counters.

LP1WE, LP2WE Pattern recognition RAM write enables.

SLCK Loads slave clock edge selector and pod 2 master/slave clock selector. Generates CPU controlled clocks for loading pattern recognition RAM.

MSCK Loads master clock edge selector.

Instead of using the internal clocks, the CPU itself may clock the memory address, occurrence, and post-store counters. HCCK clocks the memory address counter, and HLDCK clocks the post-store and occurrence counters.

The Run Control Latch (U1K) sets the RUN or HALT mode. Its output, HRNCTL, controls LRUN, which enables the pod interface and sequencer latches.

The pre-run and pre-halt signals from U1L control the operation of the BNC output latch (U8C) in the Sequencer.

8C-20. MNEMONICS

The following signals, listed in alphabetical order, are used on the State Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing and State boards are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8C-1. Mnemonics

Mnemonic	Description
ACK	Address clock to the memory address counters.
BKCK	Block clock to the acquisition memory chip selector.
CS0,1	Two-bit code for the current state used by the sequencer.
D0-7	Data outputs from acquisition memory.
GS2-4	Ground sensing to the three State pods.
HA0-7	Motherboard address bus.
HARM	Arm. Allows State to arm Timing, or vice versa.
HBRK1-3	Signals to break feedback paths for signature analysis.
HD0-7	Motherboard data bus.
HEOM	End of measurement. Stops the memory address counters.
HLDK	Load clock. CPU clocks the poststore and occurrence counters.
HMR	Master reset. Resets sample latches and occurrence counter.
HOCTC	Occurrence counter terminal count.
HPE	Preset enable. Presets occurrence counters on Next State 0.
HPREHALT	Pulse that occurs just before a halt.
HRDK	Read clock. CPU clocks the memory address counter.
HRDRST	Read reset. Allows the CPU to cause End of Measurement (EOM).
HRLW	High read low write. Enables reading and writing to the CPU.
HRUN	Enables sample and sequencer counters as latches during a run.

Table 8C-1. Mnemonics (Cont'd)

Mnemonic	Description
HSQ3	Sequencer state 3. Used by CPU for time interval measurements.
HSWM	State write enable master. State writes data into Timing Master RAM.
HSWS	State write enable slave. State writes data into Timing Slave RAM.
HTPL	Tracepoint latched from the sequencer.
ICK	Index clock. Clocks the occurrence counter, poststore counter, and all sequencing functions.
LARMEN	Arm enable. Enables occurrence counter terminal count.
LAM LAS LBM LBS LCM LCS LDM LDS	Pattern recognition lines from master and slave timing boards.
LMC	Measurement complete. Stops the write-enables to memory.
LMF	Memory-full signal from the memory address wrap-around FF.
LOCCE	Occurrence counter enable. Increments the occurrence counter.
LPAT A-D	Pattern lines from pattern recognition memory to the sequencer.
LPRERUN	Pulse that occurs just before a run.
LPSTC	Poststore counter terminal count.
LPSTCE	Poststore counter enable. Increments the poststore counter.
LRNCTL	Run control. Controls HRUN to the sample latches.
LSQTP	Store Qualified or Tracepoint. Enables data storage in RAM.
LSQWE	Sequencer RAM write enable. Used for programming the sequencer.
LSTB	Strobe. Control signal from the CPU that, when used with HRLW, indicates a data transfer.
LWE1,2	Write enable signals to acquisition memory.

Table 8C-1. Mnemonics (Cont'd)

Mnemonic	Description
MA0-9	Memory address counter output.
MCK	Master clock. Source of the address and index clocks.
MSCK	Master select clock. Selects positive or negative edge.
NS0-1	Two-bit code for the next state from the sequencer.
OCK1,2	Enables the occurrence and sequencer latches for programming.
P1WE, P2WE	Write enable signals to pattern recognition RAM.
RUNSEL	Run select. Selects memory address or poststore outputs to CPU.
SCLK1,2	Slave clocks to the sample latches.
SD0-26	Twenty-seven channel data lines from the sample latches.
SLCK	Slave select clock. Selects positive or negative edge.
SMCK	Master clock to the sample latches.
THR2-4	Thresholds to the three state pods.

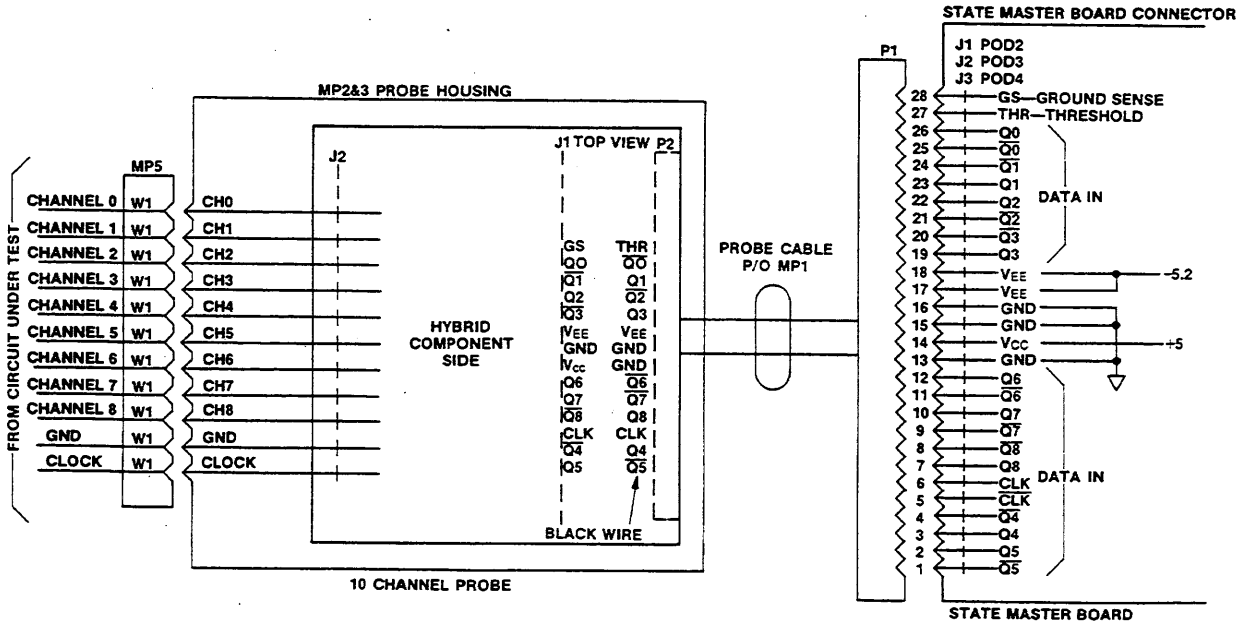
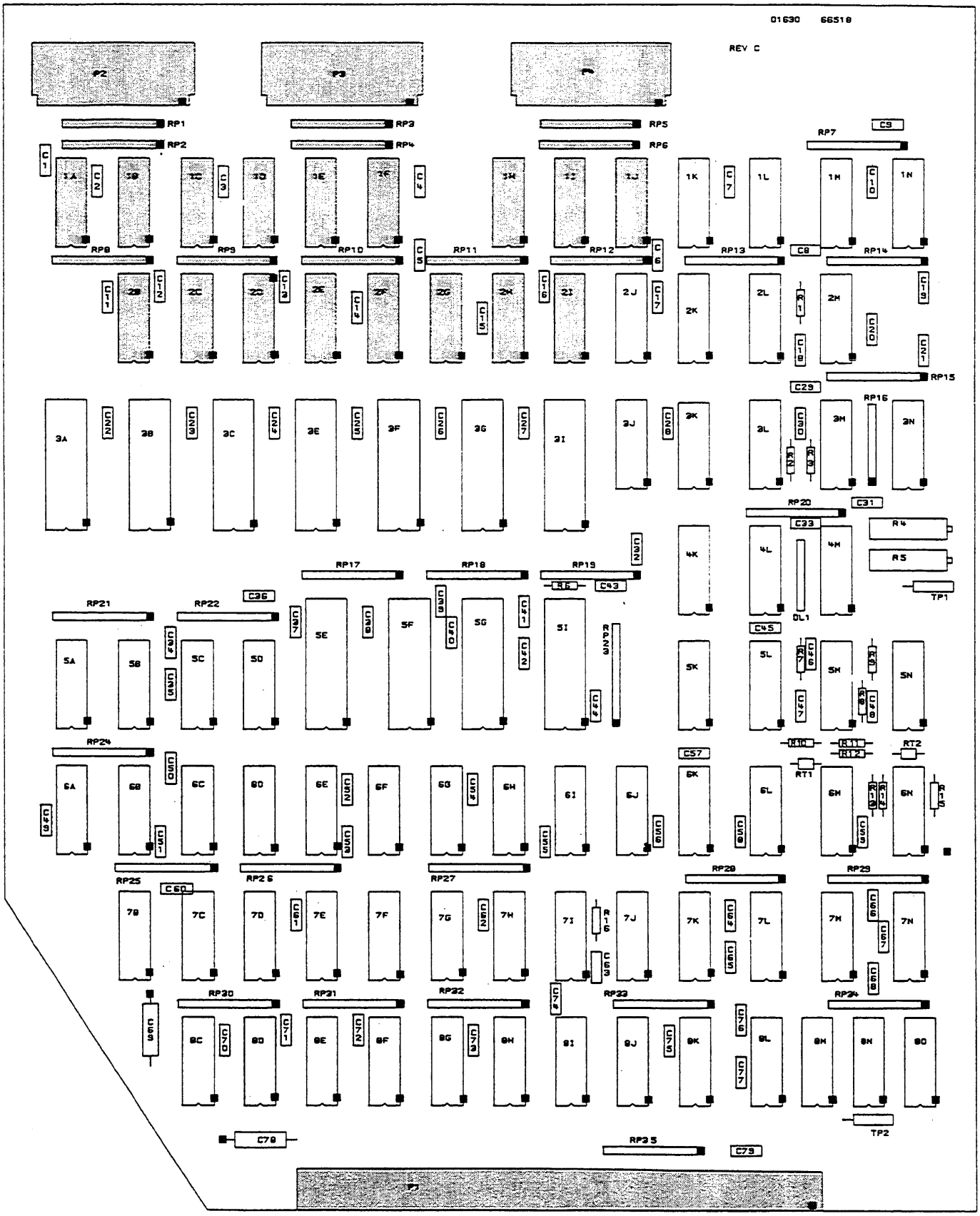


Figure 8C14. State Pod

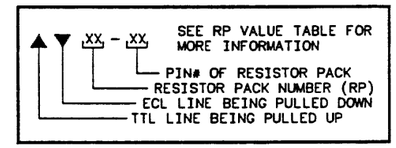


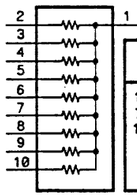
Component Locator for Schematic 8C-1

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1A-F,1H-J, U2B-2I

RESISTOR PACK DESCRIPTIONS:





RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

U1A-F,1H-J,2B-I, J1,2,3 RP1-6,8-12 J1,2,3	

P/O A4 STATE MASTER
PODS 2, 3, AND 4 INTERFACE,
COUNTER-LATCHES

STATE BOARD
PROBE INTERFACE

POD2

POD3

POD4

P/O J1

P/O J2

P/O J3

P/O P1 GS2 THR2

P/O P1 GS3 THR3

P/O P1 GS4 THR4

+5

-5.2

U1A U1B U1C U1D U1E U1F U1H U1I U1J

VBB

HMR
LAUN
SCK2
SCK1
SMCK

ECL
CTR DIV 16
G1
R
M2
M3
G4
CT=15
1, 2, 4+/1, 3C5

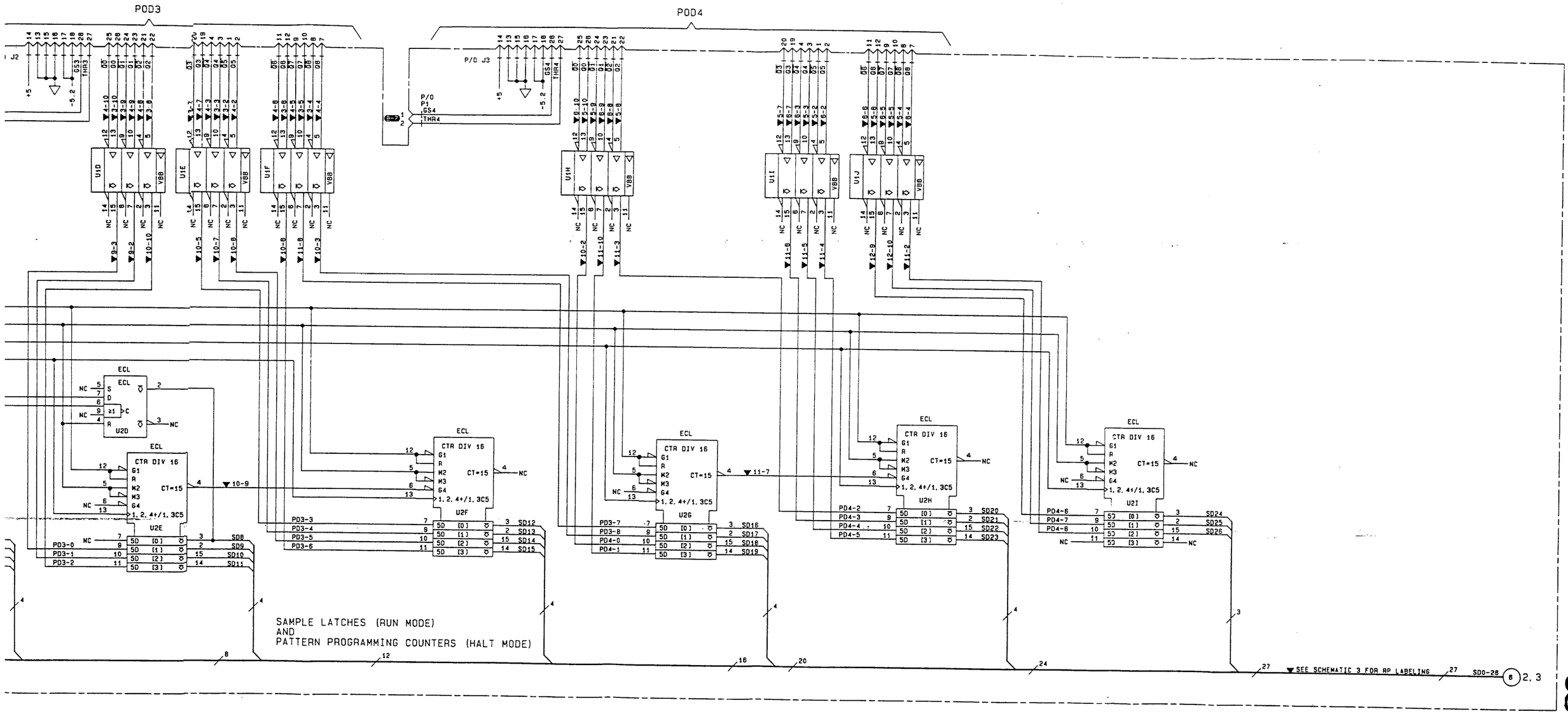
U2B U2C U2D U2E U2F U2G

5D [0] [1] [2] [3]

PD2-0 PD2-1 PD2-2 PD2-3 PD2-4 PD2-5 PD2-6 PD2-7
PD3-0 PD3-1 PD3-2 PD3-3 PD3-4 PD3-5 PD3-6
PD3-7 PD3-8 PD4-0 PD4-1 PD4-2 PD4-3 PD4-4 PD4-5

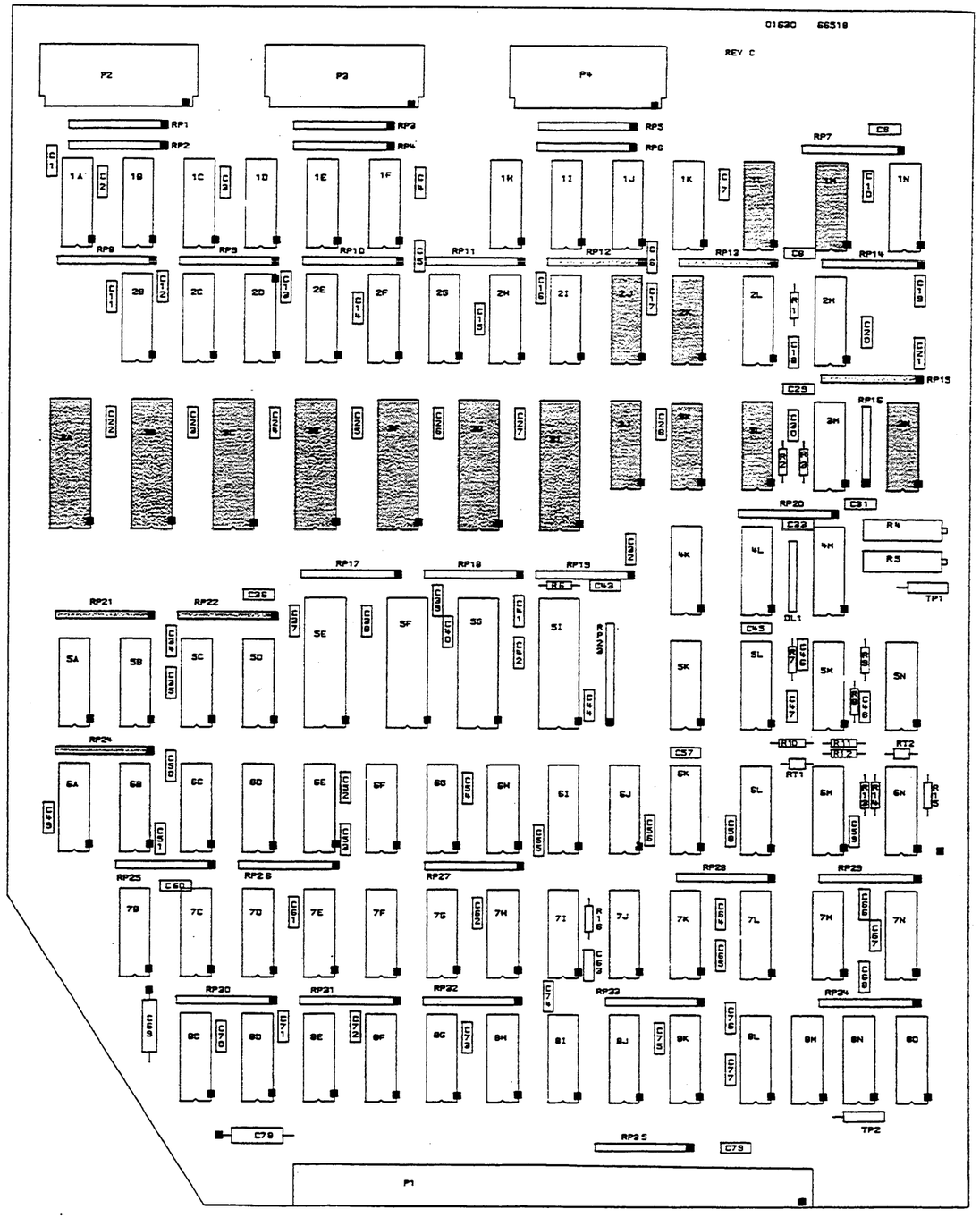
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SD8 SD9 SD10 SD11 SD12 SD13 SD14 SD15 SD16 SD17 SD18 SD19

SAMPLE LATCHES (RUN MODE)
AND
PATTERN PROGRAMMING COUNTERS (HALT MODE)



8C-

Schematic 8C-1
Pods 2, 3, and 4 Interface, Counter-Latches
8C-21



Component Locator for Schematic 8C-2

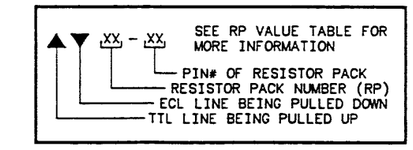
NOTE

ON STATE MASTER BOARD 01630-66505, U3N PINS 14 AND 15 ARE CONNECTED TO U4M PIN 4 AND U6K PIN 5 RESPECTIVELY (SCHEMATIC 8C-7). THESE LINES ARE ALSO PULLED DOWN BY PARTS OF RP-15.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1L,1M,2J,2K 3J-3L,3N
Vcc(gnd) Vcca(gnd) Vee(-5.2)	24 1 12	U3A-3C,3E-3G, 3I

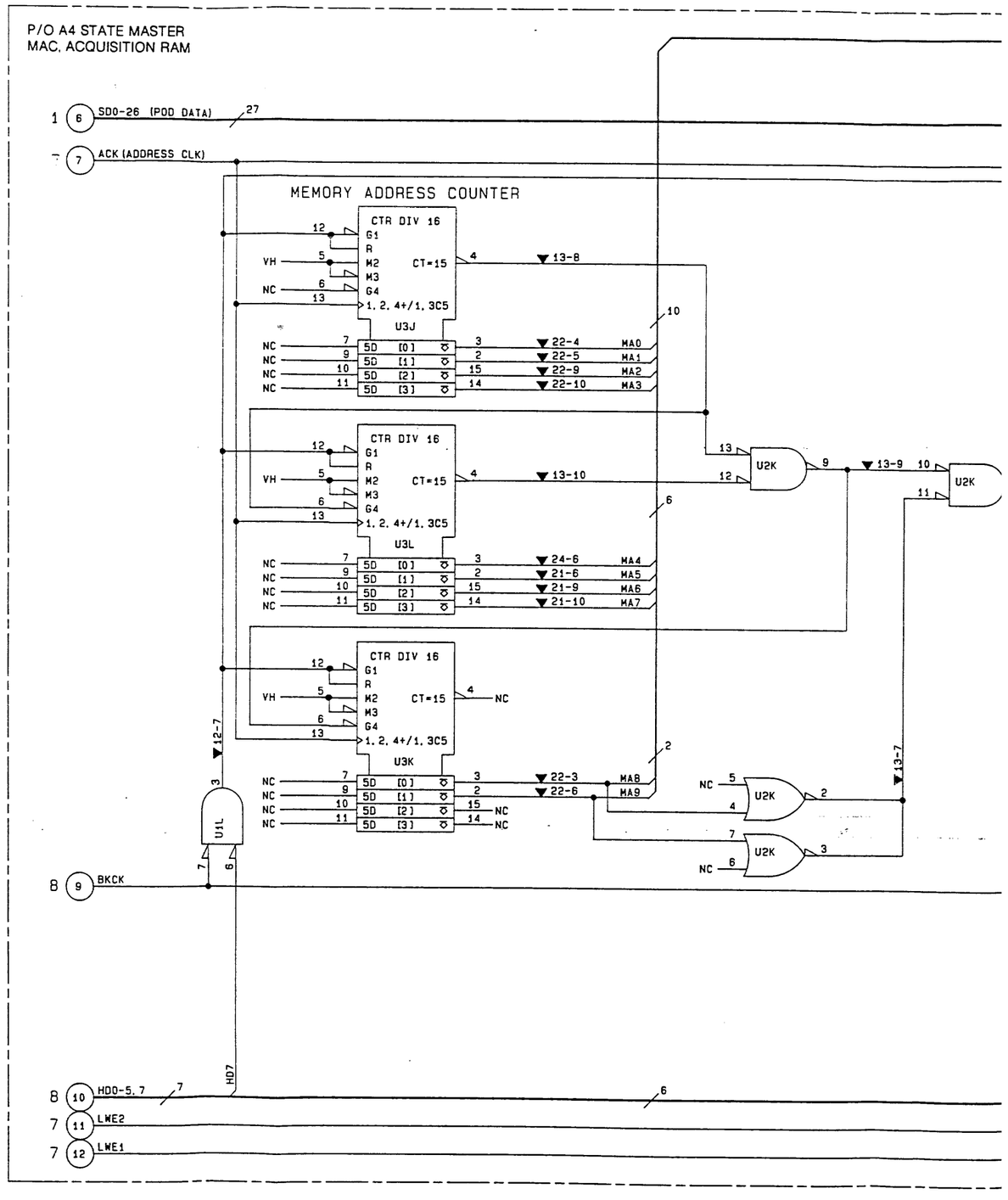
RESISTOR PACK DESCRIPTIONS



RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

RP12,13,15,21-22,24 U1L,1M,2K,2J,3A-3C U3E-3G,3I,3J-3L,N	



TE MASTER BOARD 01630-66505,
S 14 AND 15 ARE CONNECTED TO
4 AND U6K PIN 5 RESPECTIVELY
TIC 8C-7). THESE LINES ARE ALSO
DOWN BY PARTS OF RP-15.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
'cc1(gnd) 'cc2(gnd) 'ee(-5.2)	1 16 8	U1L,1M,2J,2K 3J-3L,3N
'cc(gnd) 'cca(gnd) 'ee(-5.2)	24 1 12	U3A-3C,3E-3G, 3I

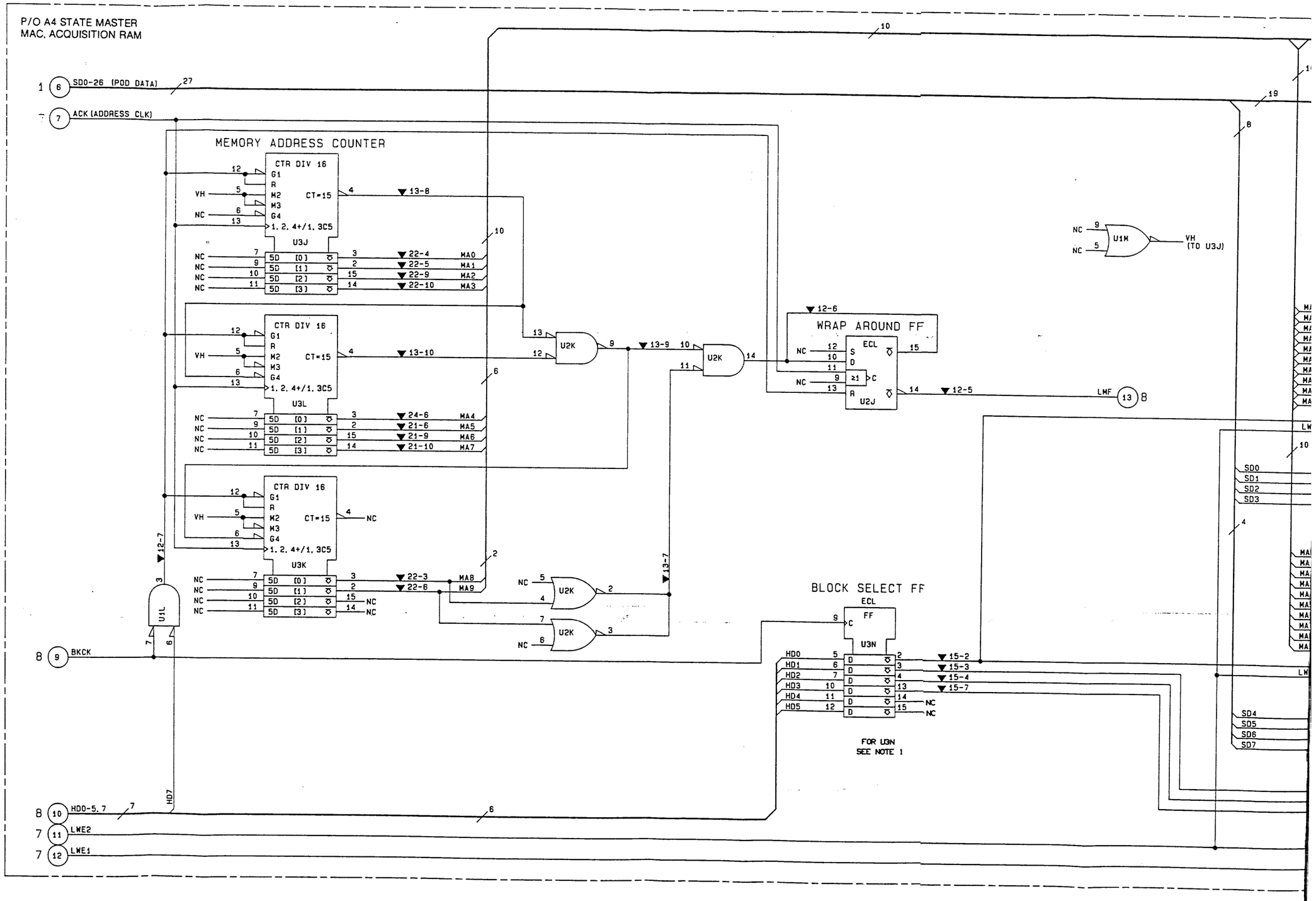
SISTOR PACK DESCRIPTIONS

XX - XX SEE RP VALUE TABLE FOR MORE INFORMATION
PIN# OF RESISTOR PACK
RESISTOR PACK NUMBER (RP)
ECL LINE BEING PULLED DOWN
TTL LINE BEING PULLED UP

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6	330 X 9	1	-5.2
7-15	100 X 9	1	-2.4

RTS ON THIS SCHEMATIC

2,13,15,21-22,24 .,1M,2K,2J,3A-3C -3G,3I,3J-3L,N	



ACQUISITION RAM

WRAP AROUND FF

BLOCK SELECT FF

FOR U3N
SEE NOTE 1

U1M

U2J

U3N

U3A

U3B

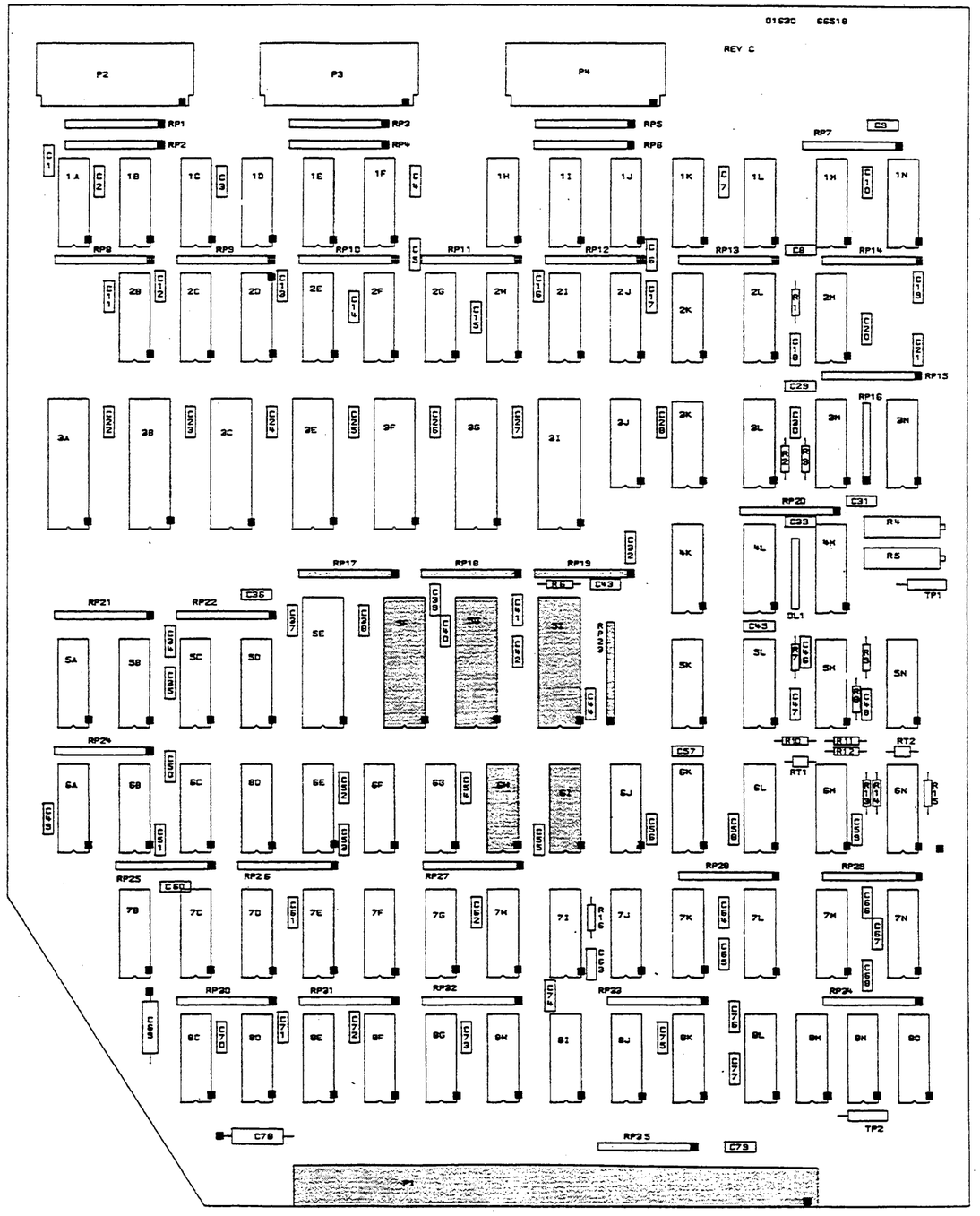
U3C

U3E

U3F

U3G

U3I

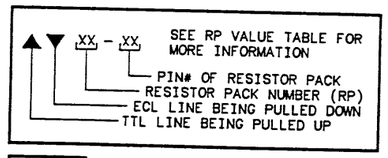


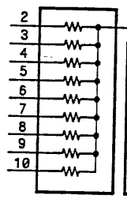
Component Locator for Schematic 8C-3

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U6I
Vcc(gnd) Vcca(gnd) Vee(-5.2)	24 1 12	U5F,5G,5I
Vcc(gnd) Vee(-5.2)	16 8	U6H

RESISTOR PACK DESCRIPTIONS





RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

P/O P1 RP17-19,23,35 U5F,5G,5I,6H, U6I	

P/O A4 STATE MASTER
PATTERN RECOGNITION RAM

1 6 SD0-26 — 27 — 19 — 11
8 10 HD0-7 — 8 — 8 — 8 — 8
8 19 LP2WE
8 20 LP1WE

4 — 8 — 4 — 8 — 4 — 8

RAM 256X4 (U5F)
SD0 17-6 13
SD1 17-7 14
SD2 17-8 15
SD3 17-9 16
SD4 17-10 17
SD5 17-5 9
SD6 17-4 10
SD7 17-3 11
A 0/255
NC 3 G1
NC 5 G2
NC 20 G3
NC 22 G4
8 C [WRITE]
EN [READ]

HD0 6 1AD 1A 2
HD1 7 2AD 2A 4
HD2 18 3AD 3A 21
HD3 19 4AD 4A 23

RAM 256X4 (U5G)
SD8 17-2 13
SD9 18-10 14
SD10 18-9 15
SD11 18-8 16
SD12 18-4 17
SD13 18-5 9
SD14 18-6 10
SD15 18-7 11
A 0/255
NC 3 G1
NC 5 G2
NC 20 G3
NC 22 G4
8 C [WRITE]
EN [READ]

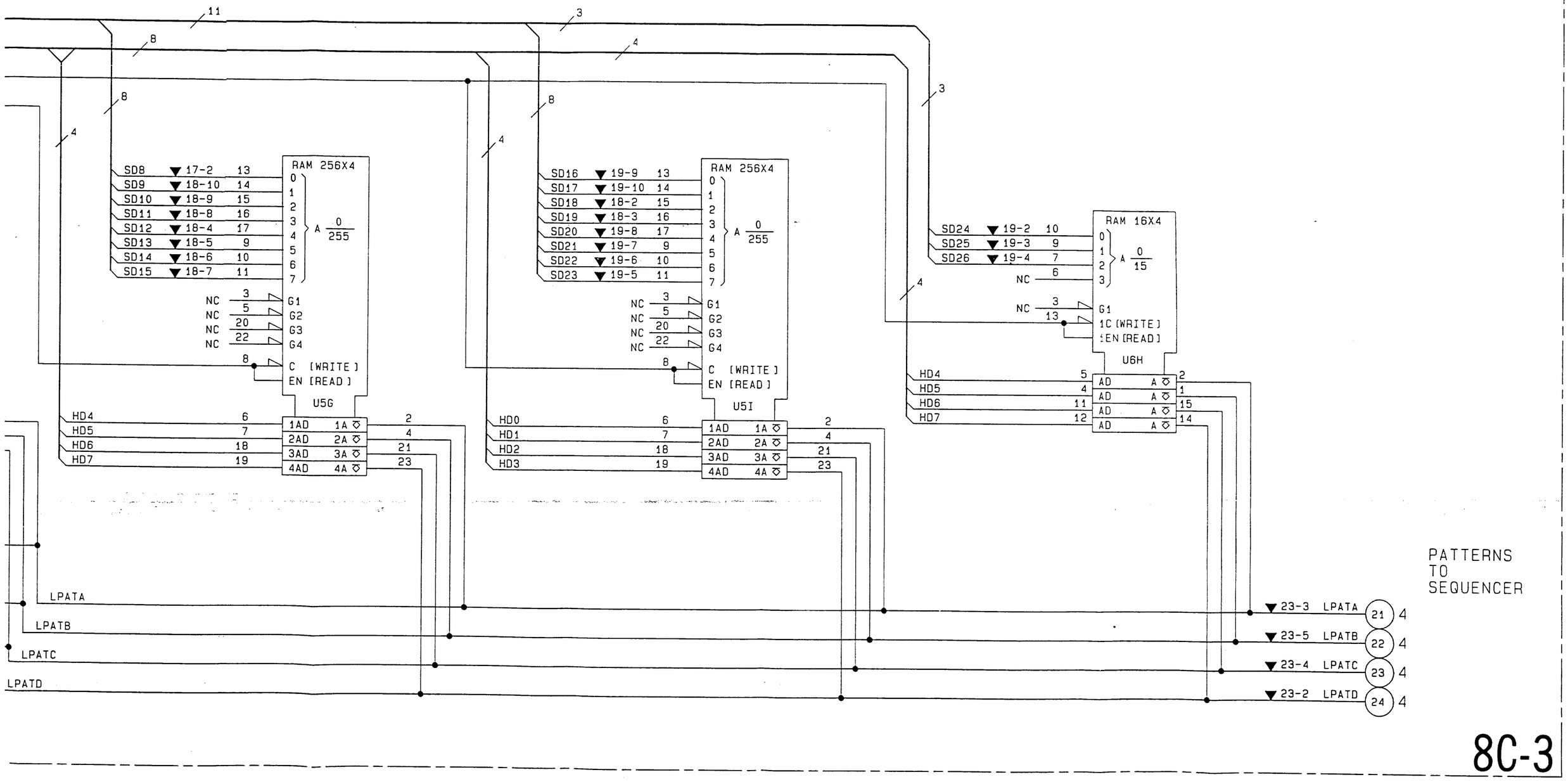
HD4 6 1AD 1A 2
HD5 7 2AD 2A 4
HD6 18 3AD 3A 21
HD7 19 4AD 4A 23

HD0
HD1
HD2
HD3

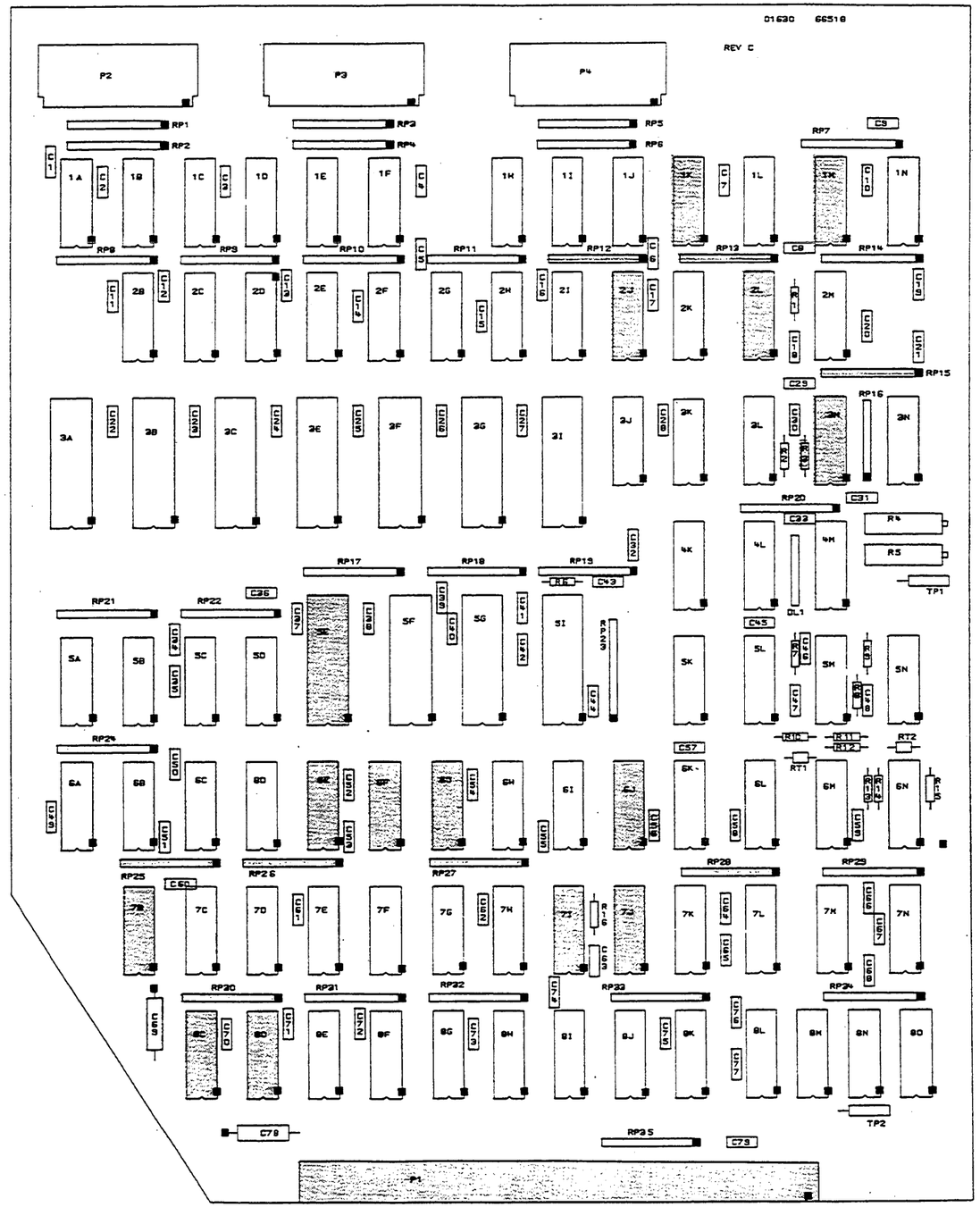
PATTERNS FROM MASTER AND SLAVE TIMING

35-10 13 U6I 15
35-9 12 U6I 9 NC
35-8 11
35-7 10 U6I 14 LPATA
35-6 7
35-5 6 U6I 3 LPATB
35-4 5
35-3 4 U6I 2 LPATC
LPATD

LAM LAS LBM LBS LCM LCS LDM LDS
P/O P1
36 35 34 33 32 31 30 29
D-1
E-1
F-2



Schematic 8C-3
Pattern Recognition RAM



Component Locator for Schematic 8C-4

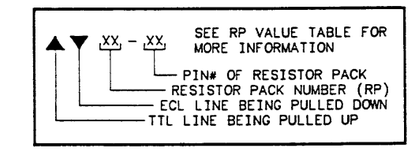
NOTE 1

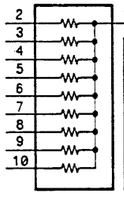
ON STATE MASTER BOARD 01630-66505, J3 PINS 12, 13, AND 14 ARE CONNECTED TO PINS OF U6G AND U6F. U6G PINS 12, 13, 14, AND 15 HAVE NO FUNCTION IN ANY 163X.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1K,1M,2J,2L, 3M,6E-6G,6J, 7B,7I,7J,8C,8D
Vcc(gnd) Vcc(gnd) Vee(-5.2)	12 1 24	U5E

RESISTOR PACK DESCRIPTIONS





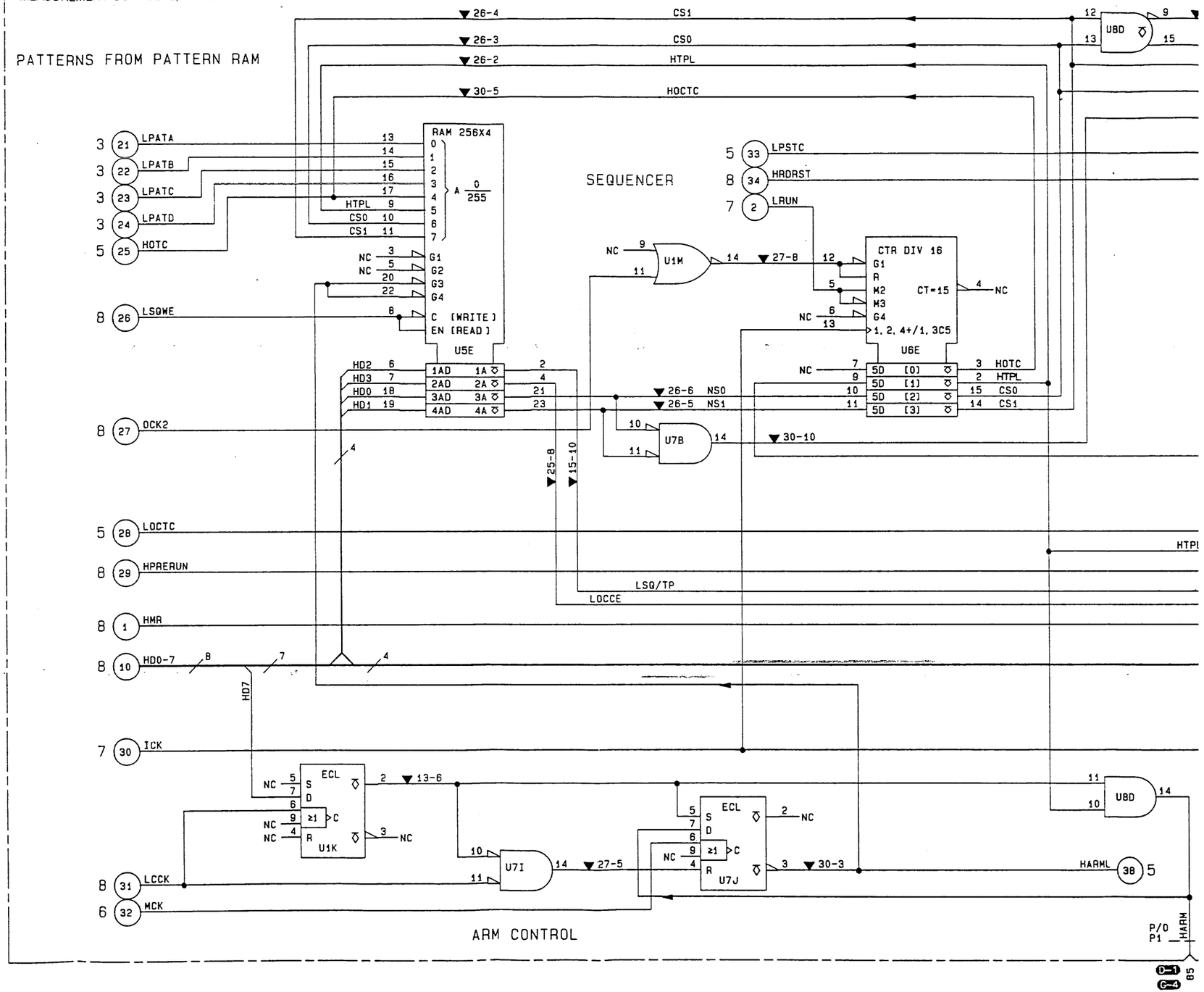
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

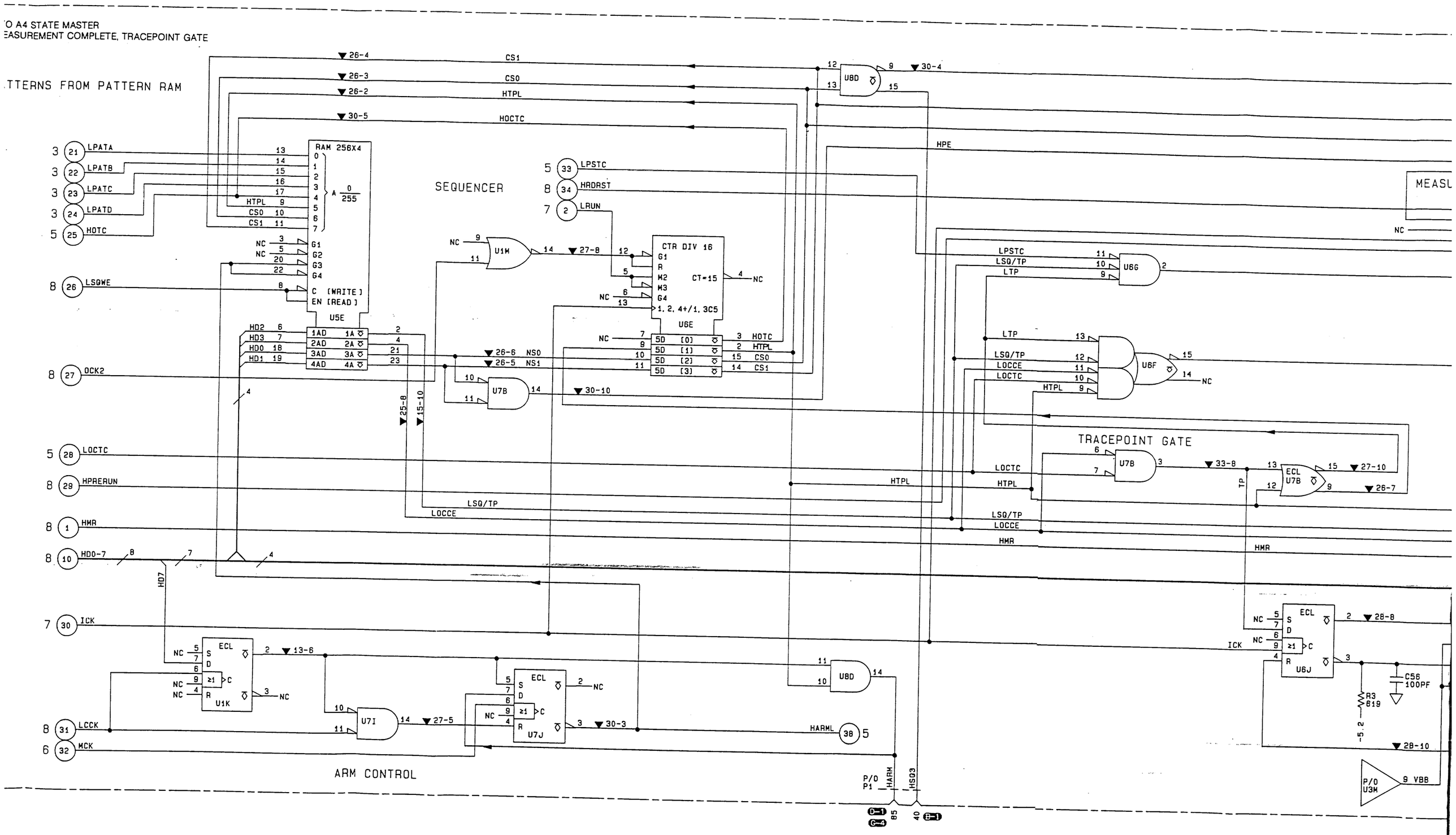
PARTS ON THIS SCHEMATIC

C56 P/O P1 R3 RP12,13,15,25-28 30,33 U1K,M,2J,L,3M, U5E,6E-G,J,7B, U7I,J,8C,D	

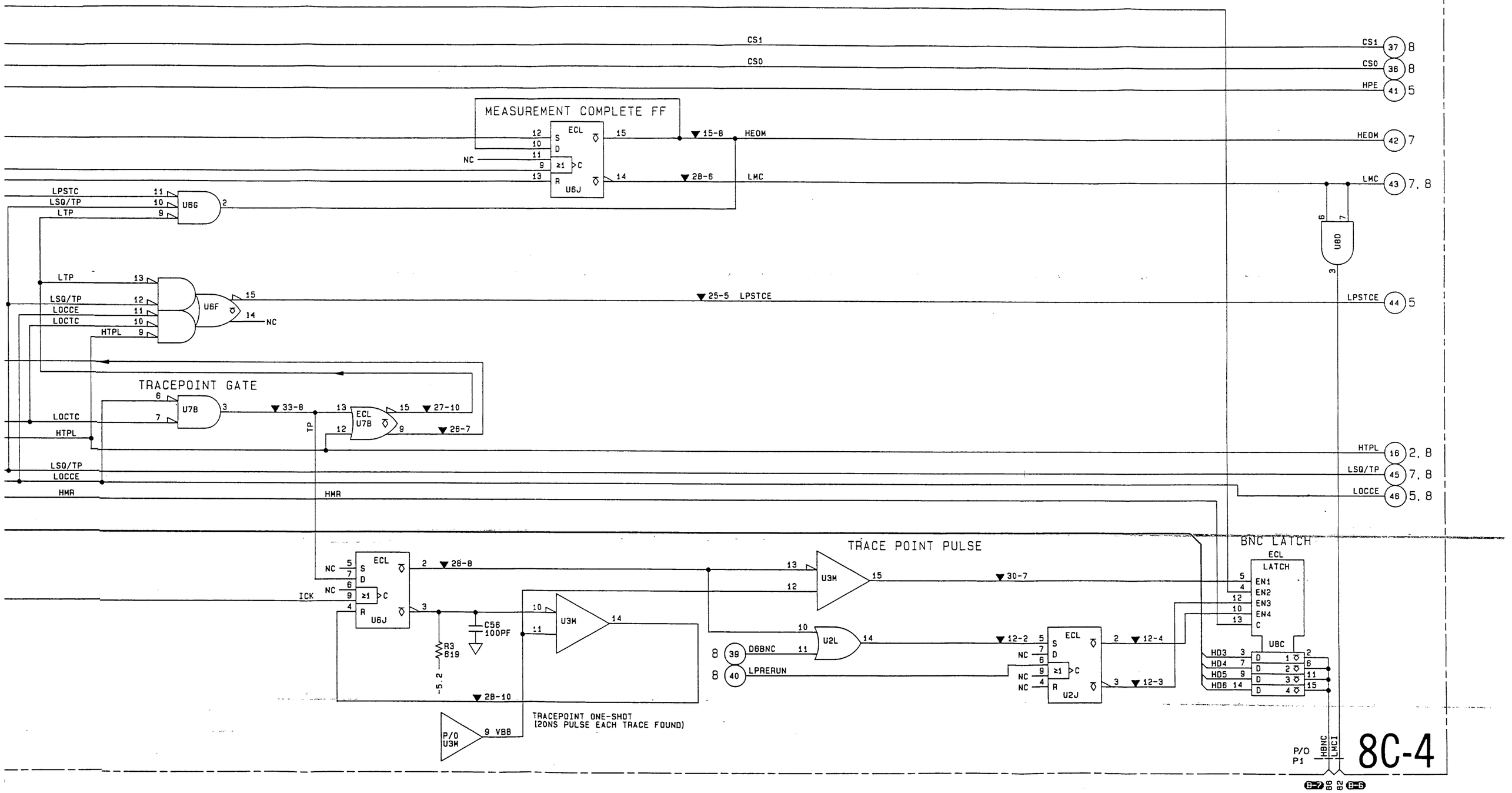
P/O A4 STATE MASTER
MEASUREMENT COMPLETE, TRACEPOINT GATE

PATTERNS FROM PATTERN RAM





'O A4 STATE MASTER
EASUREMENT COMPLETE, TRACEPOINT GATE
TTERNS FROM PATTERN RAM
SEQUENCER
TRACEPOINT GATE
ARM CONTROL
MEASU
RAM 256X4
CTR DIV 16
U5E
U6E
U1M
U7B
U8D
U6G
U6F
U7B
ECL
U1K
U7I
U7J
U6J
LPATA
LPATB
LPATC
LPATD
HOTC
LSQWE
OCK2
LOCTC
HPRERUN
HMR
HD0-7
ICK
LCCK
MCK
LPSTC
HRDRST
LRUN
HPE
HTPL
HOCTC
CS1
CS0
LSQ/TP
LOCCE
LTP
HARML
HARM
HSQ3
P/O P1
P/O U3M
VBB
C56 100PF
R3 619
-5.2

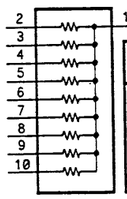


Schematic 8C-4
Measurement Complete, Tracepoint Gate
8C-27

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1M U6B-6D,7B-7I 8D
Vcc(gnd) Vee(-5.2)	16 8	U8E-8H

RESISTOR PACK DESCRIPTIONS

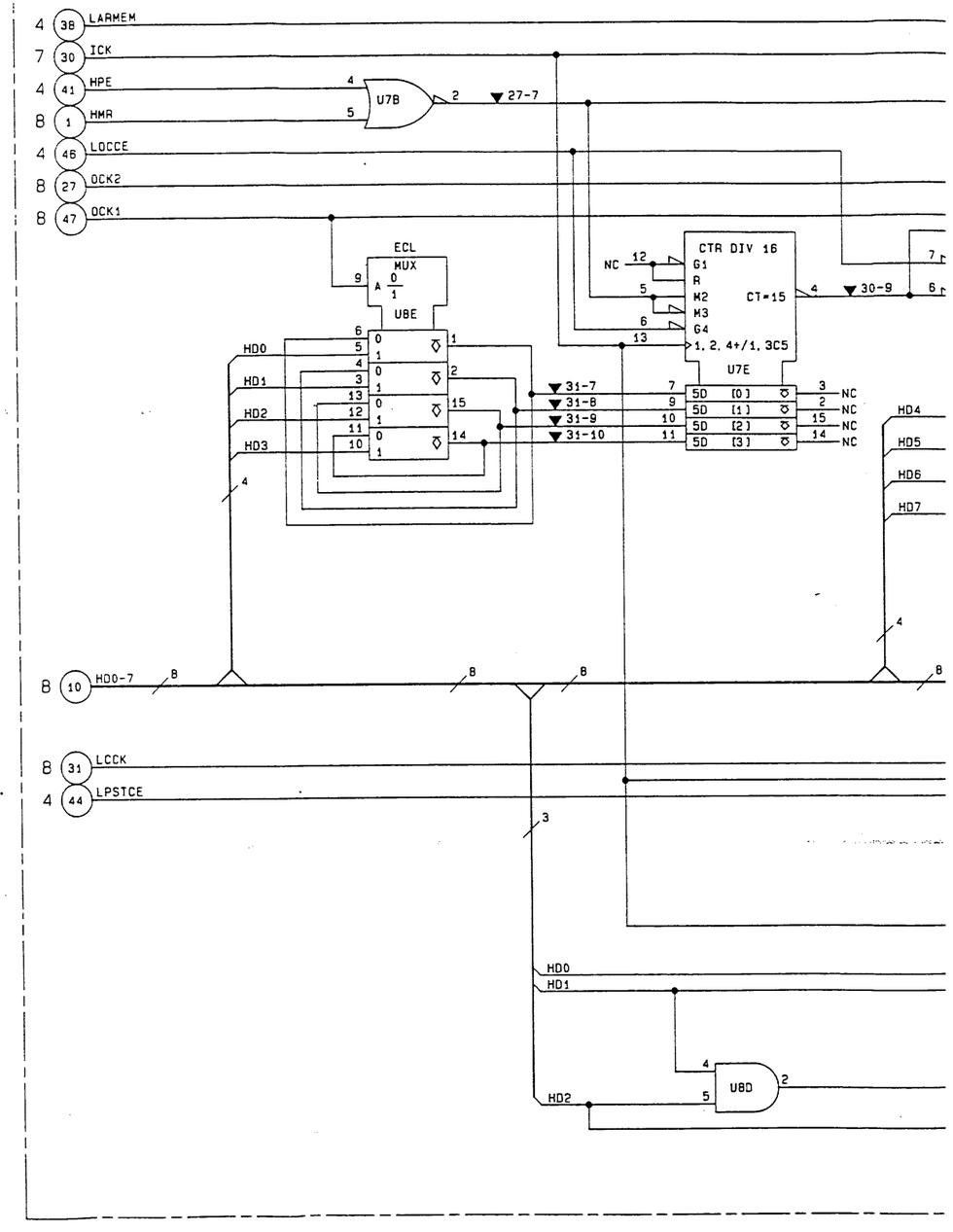


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

RP24-27,30-32 U1M,6B-D,7B-I, U8D-H	

P/O A4 STATE MASTER
POSTSTORE AND OCCURRENCE COUNTERS



IC DEVICE
OWER CONNECTIONS

'LY	PIN NO.	IC GROUP
d) d) 2)	1 16 8	U1M U6B-6D,7B-7I 8D
) 2)	16 8	U8E-8H

OR PACK DESCRIPTIONS

5 - XX — SEE RP VALUE TABLE FOR MORE INFORMATION
— PIN# OF RESISTOR PACK
— RESISTOR PACK NUMBER (RP)
— ECL LINE BEING PULLED DOWN
— TTL LINE BEING PULLED UP

1

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

ON THIS SCHEMATIC

30-32),7B-I.	

P/O A4 STATE MASTER
POSTSTORE AND OCCURRENCE COUNTERS

4 38 LARMEM
7 30 ICK
4 41 HPE
8 1 HMR
4 46 LOCCE
8 27 OCK2
8 47 OCK1

U7B ▼27-7

ECL MUX U8E — HD0 HD1 HD2 HD3

CTR DIV 16 U7E — G1 R M2 M3 G4 CT=15 — 1, 2, 4+/1, 3C5 — ▼30-9

U7C ▼30-6

ECL MUX U8F — HD4 HD5 HD6 HD7

CTR DIV 16 U7F — ▼31-2 ▼31-3 ▼31-4 ▼31-5 — ▼30-8

U7C

OCCURRENCE COUNTER
AND LOAD LATCHES

HD0 HD1 HD2 HD3

8 10 HD0-7

8 31 LCCK
4 44 LPSTCE

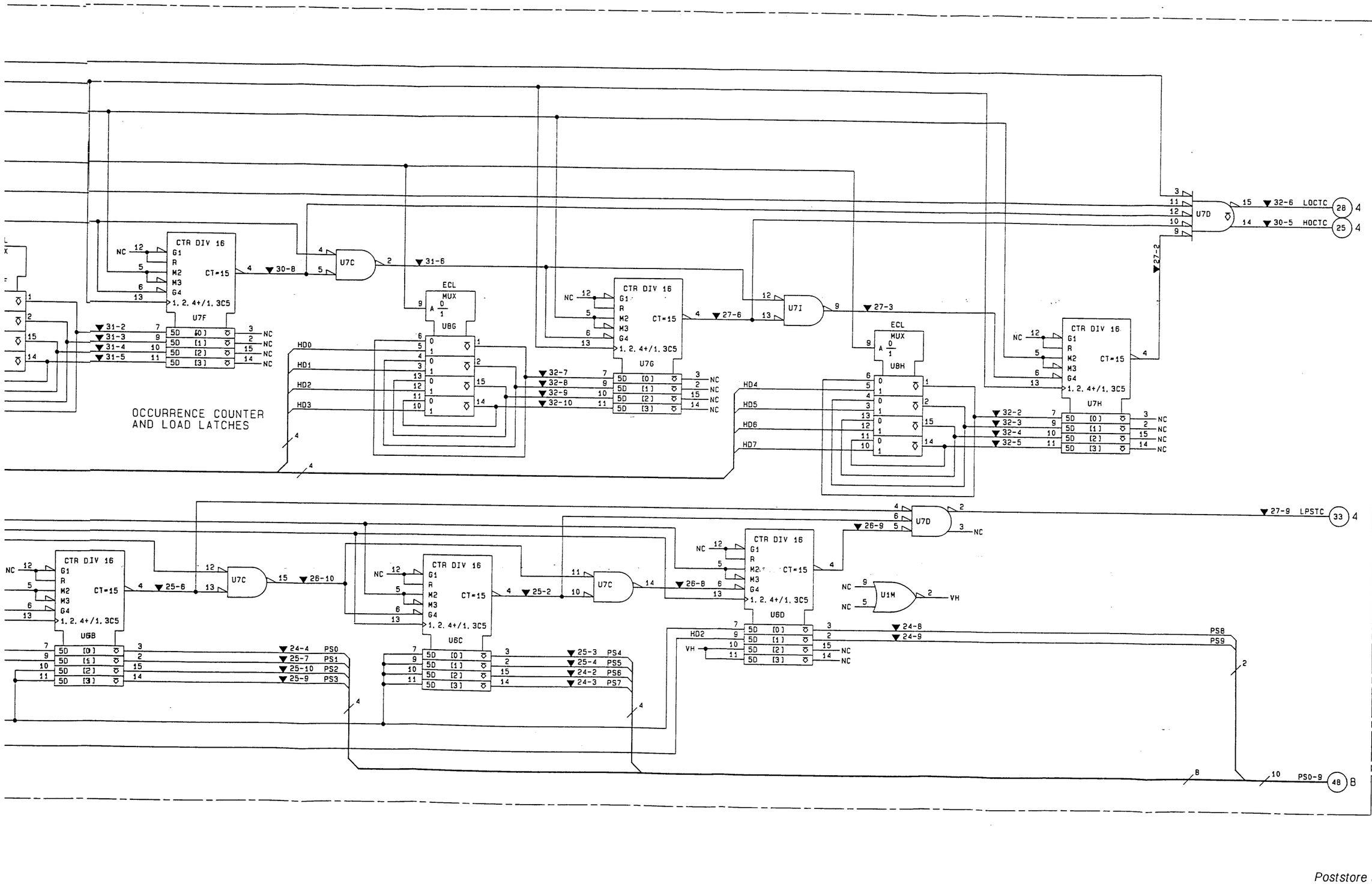
CTR DIV 16 U8B — ▼25-6

U7C ▼26-10

HD0 HD1 HD2

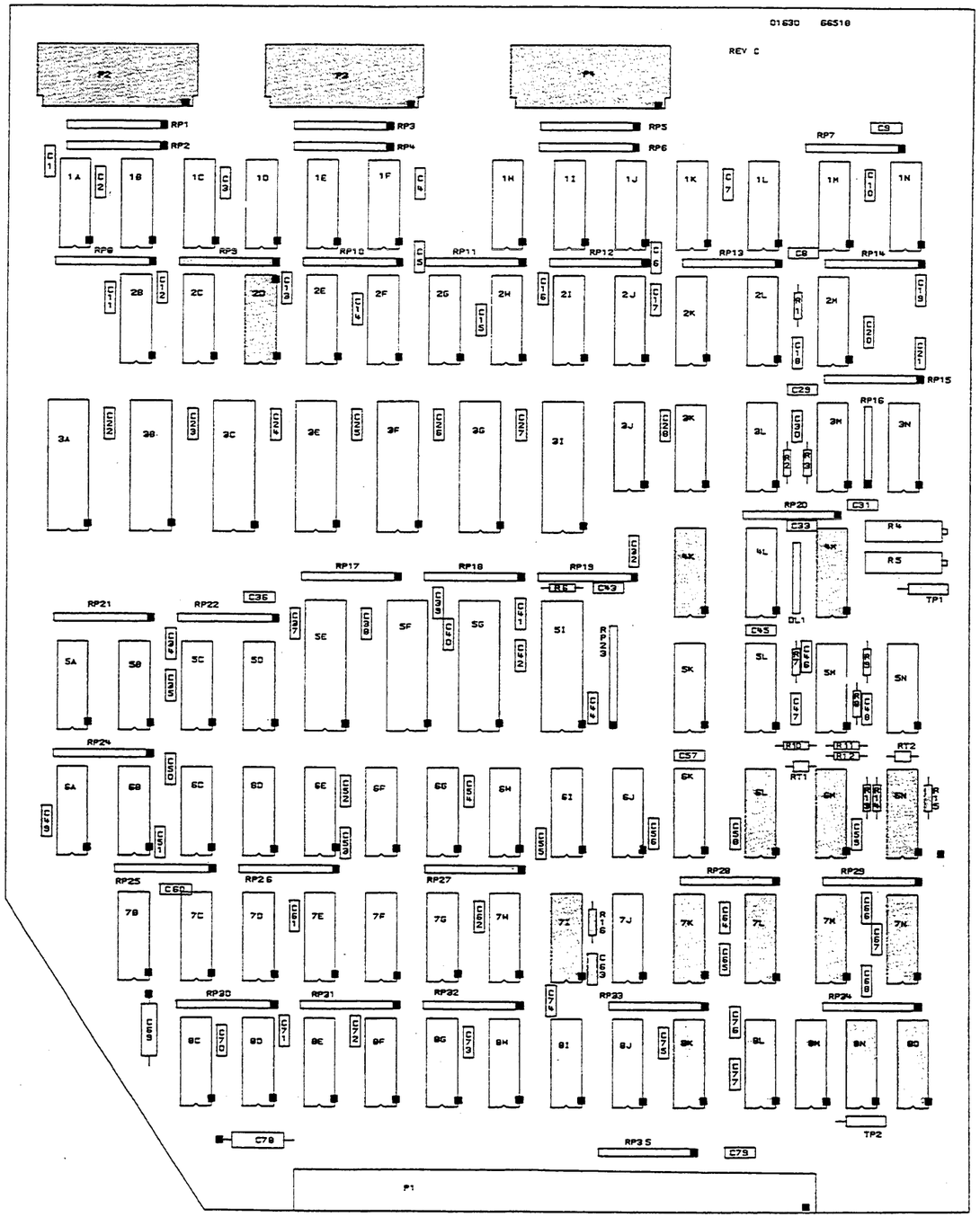
U8D ▼30-2

▼24-4 PS0
▼25-7 PS1
▼25-10 PS2
▼25-9 PS3



8C-5

Schematic 8C-5
Poststore and Occurrence Counters
8C-29

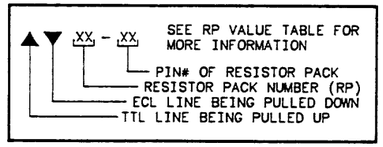


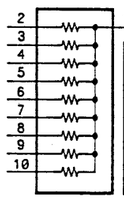
Component Locator for Schematic 8C-6

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2D,4K,4M,6L-N, 7I,7K-N,8M-8O
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1,15 16 8	U8K
Vcc(gnd) Vee(-5.2)	16 8	U8L

RESISTOR PACK DESCRIPTIONS

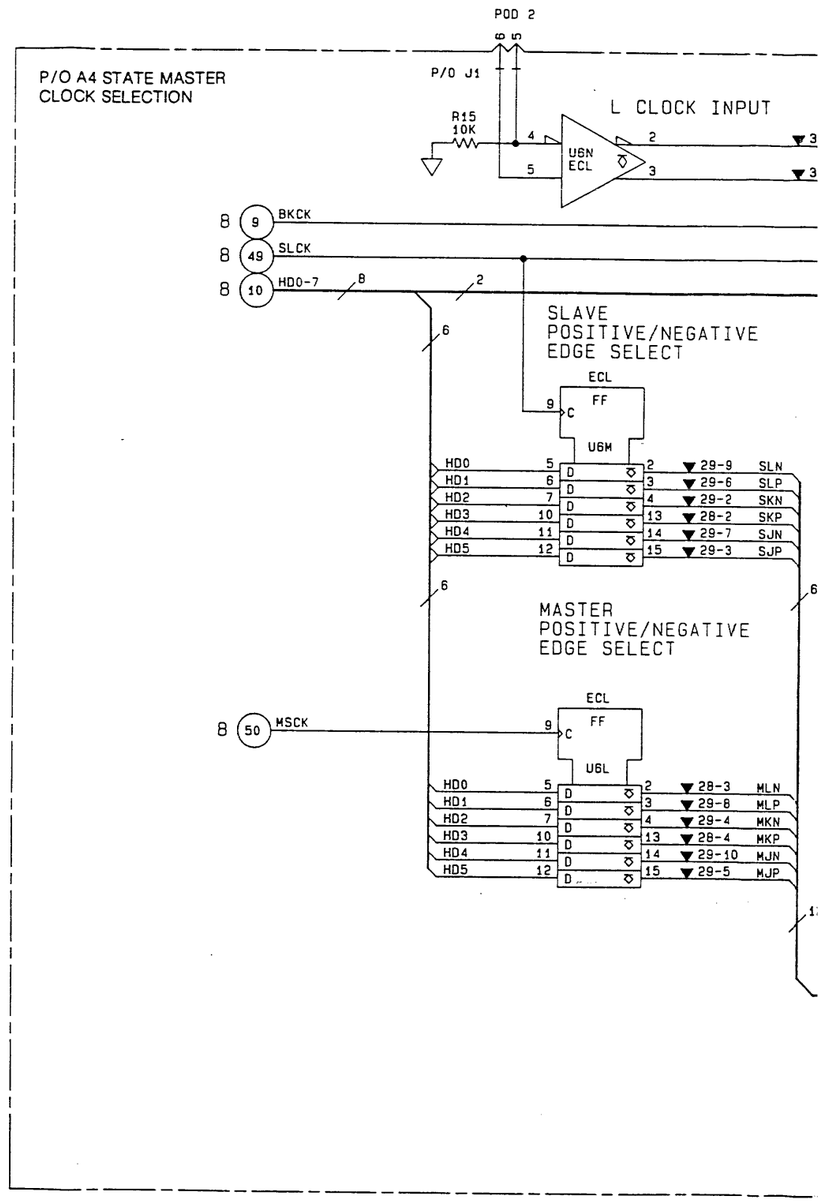




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

PARTS ON THIS SCHEMATIC

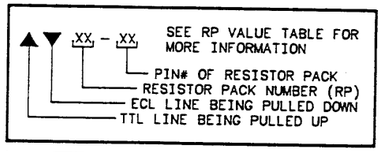
C43,63 J1,2,3 P/O P1 R5,13-16 RP9,10,20,27-29, 33-35 U2D,4K,M,6L-N U7I,K-N,8K-O	



IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2D,4K,4M,6L-N, 7I,7K-N,8M-8O
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1,15 16 8	U8K
Vcc(gnd) Vee(-5.2)	16 8	U8L

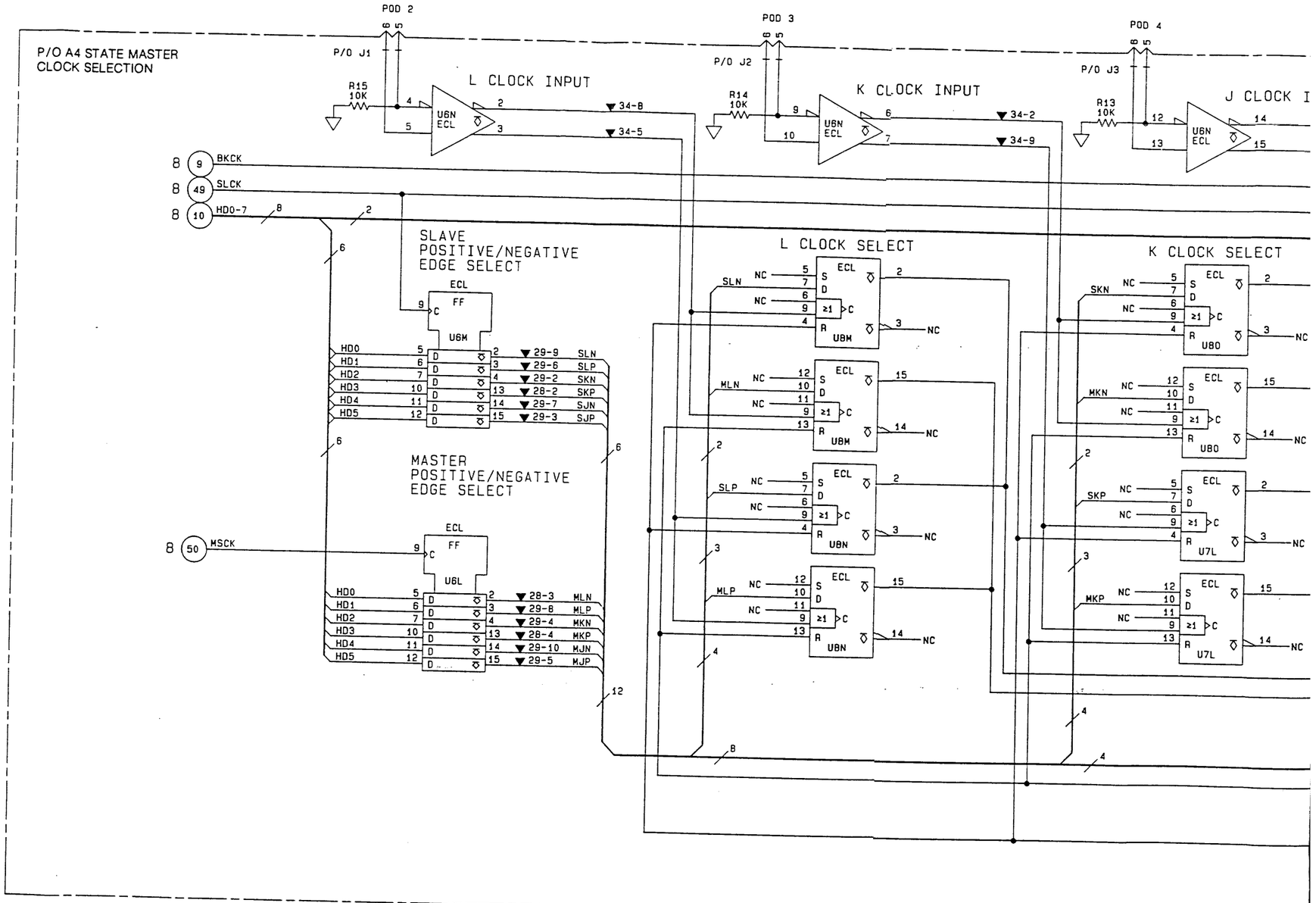
RESISTOR PACK DESCRIPTIONS

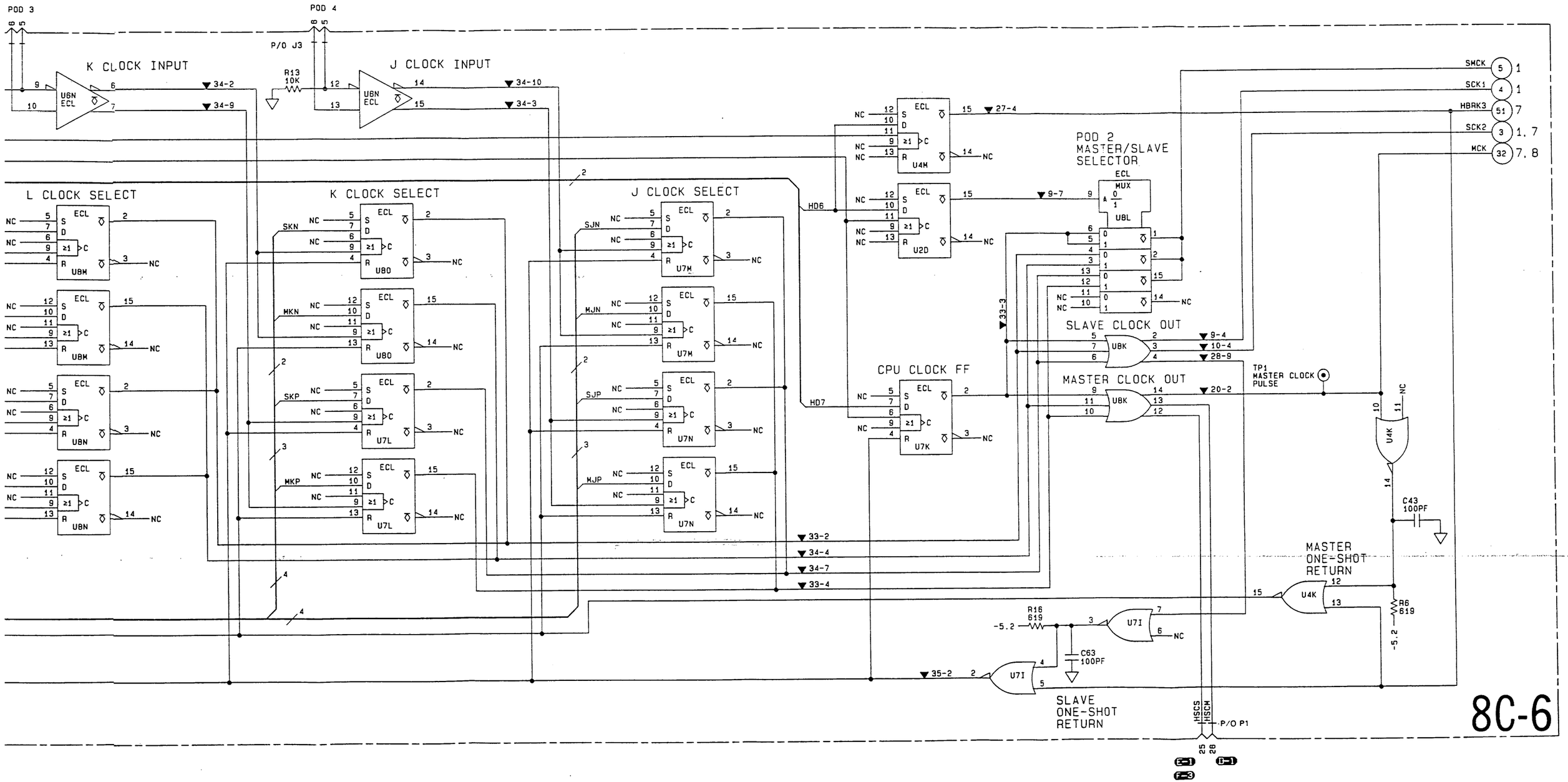


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6	330 X 9	1	-5.2
7-15	100 X 9	1	-2.4
17-35			

PARTS ON THIS SCHEMATIC

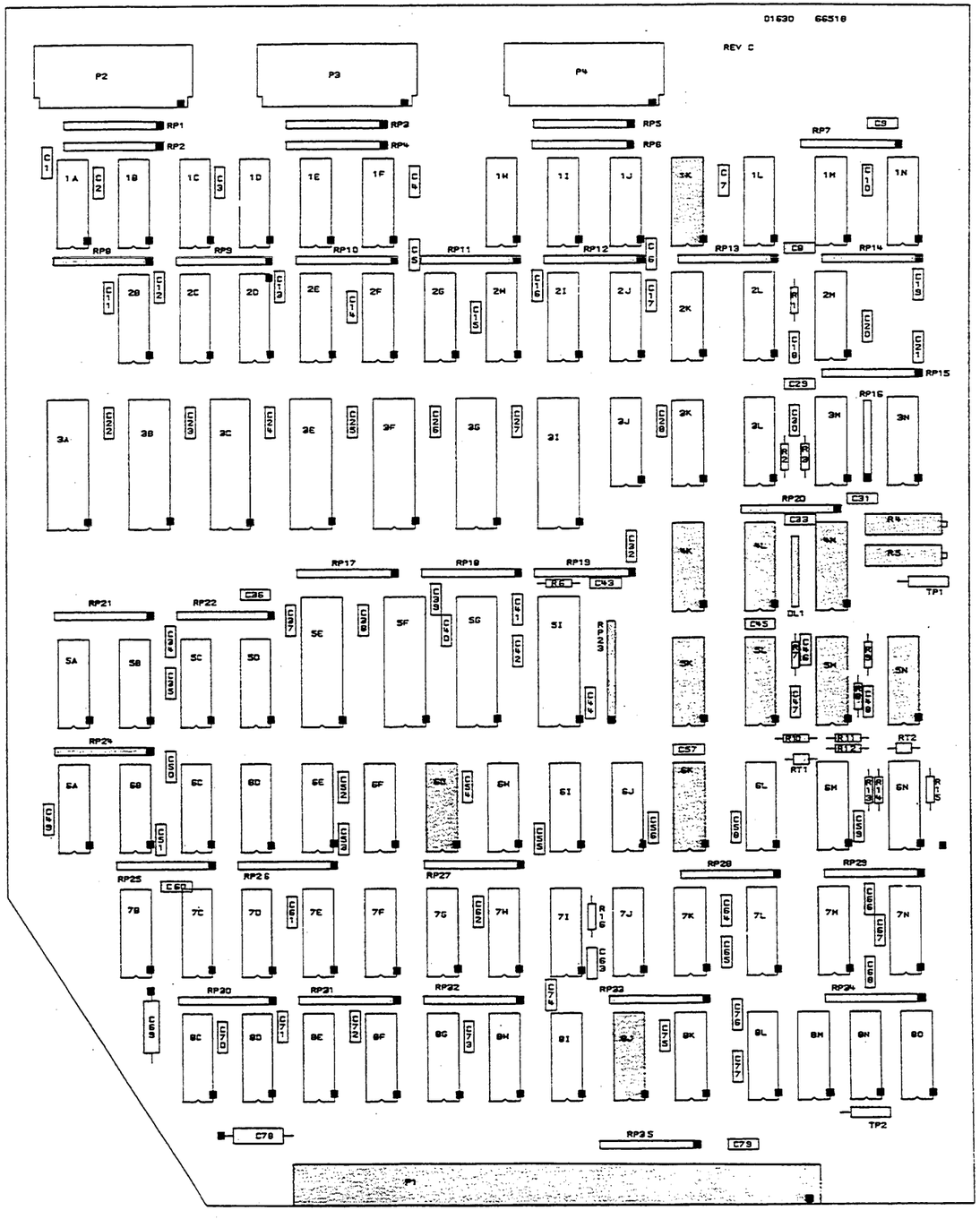
C43,63 J1,2,3 P/O P1 R6,13-16 RP9,10,20,27-29, 33-35 U2D,4K,M,6L-N U7I,K-N,8K-O	





8C-6

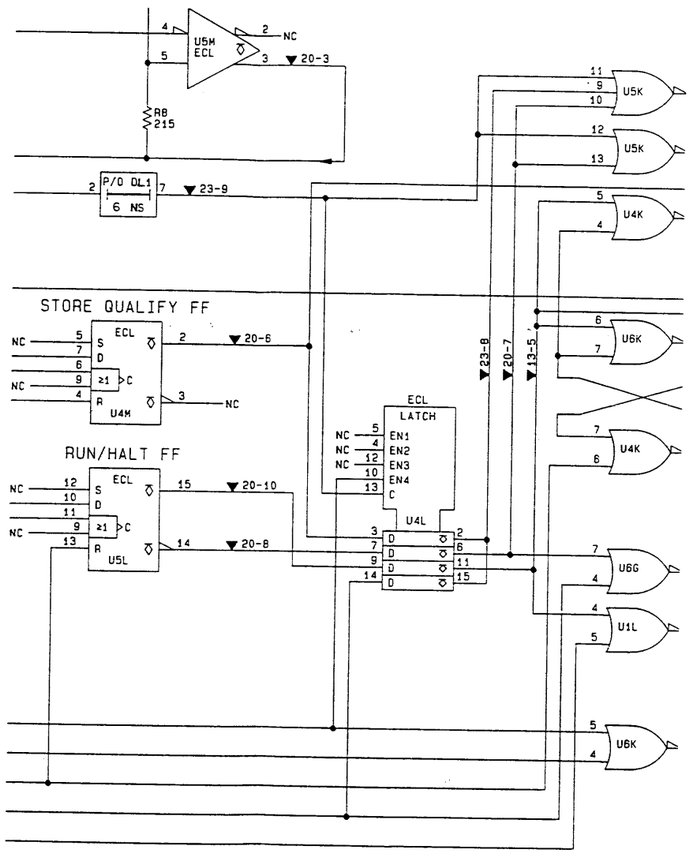
Schematic 8C-6
Clock Selection
8C-31



Component Locator for Schematic 8C-7

NOTE 1

ON STATE MASTER BOARD 01630-66505, THE SCHEMATIC BELOW REFLECTS THE USE OF A DIFFERENT PART FOR U4L, 1820-2451, AND THE CIRCUIT DIFFERENCES THAT ACCOMMODATE THAT PART.



NOTE 2

ON STATE MASTER BOARD 01630-66505, U4M PIN 4 IS CONNECTED TO U3N PIN 14 (8C-2) AND U6K PIN 5 IS CONNECTED TO U3N PIN 15 (8C-2).

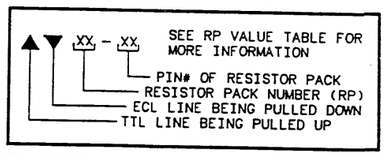
NOTE 3

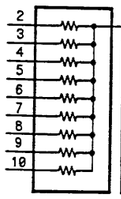
ON STATE MASTER BOARDS 01630-66505 AND 01630-66509, DELAY LINE DL1 IS MADE 7ns BY MAKING THE OUTPUT CONNECTION TO PIN 7 RATHER THAN PIN 6.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1L,4K,M 5K-N,6G,K, 8J
Vcc2(gnd) Vee(-5.2)	16 8	U4L

RESISTOR PACK DESCRIPTIONS:



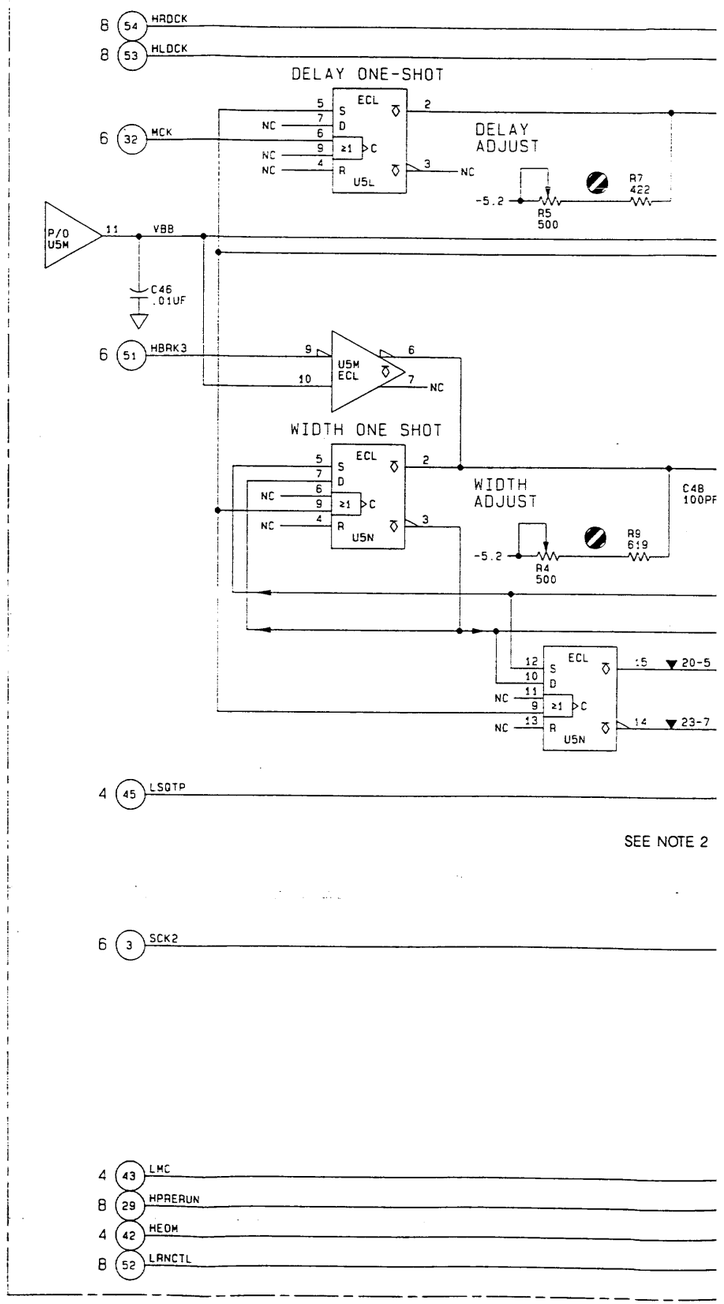


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 7-15 17-35	330 X 9 100 X 9	1 1	-5.2 -2.4

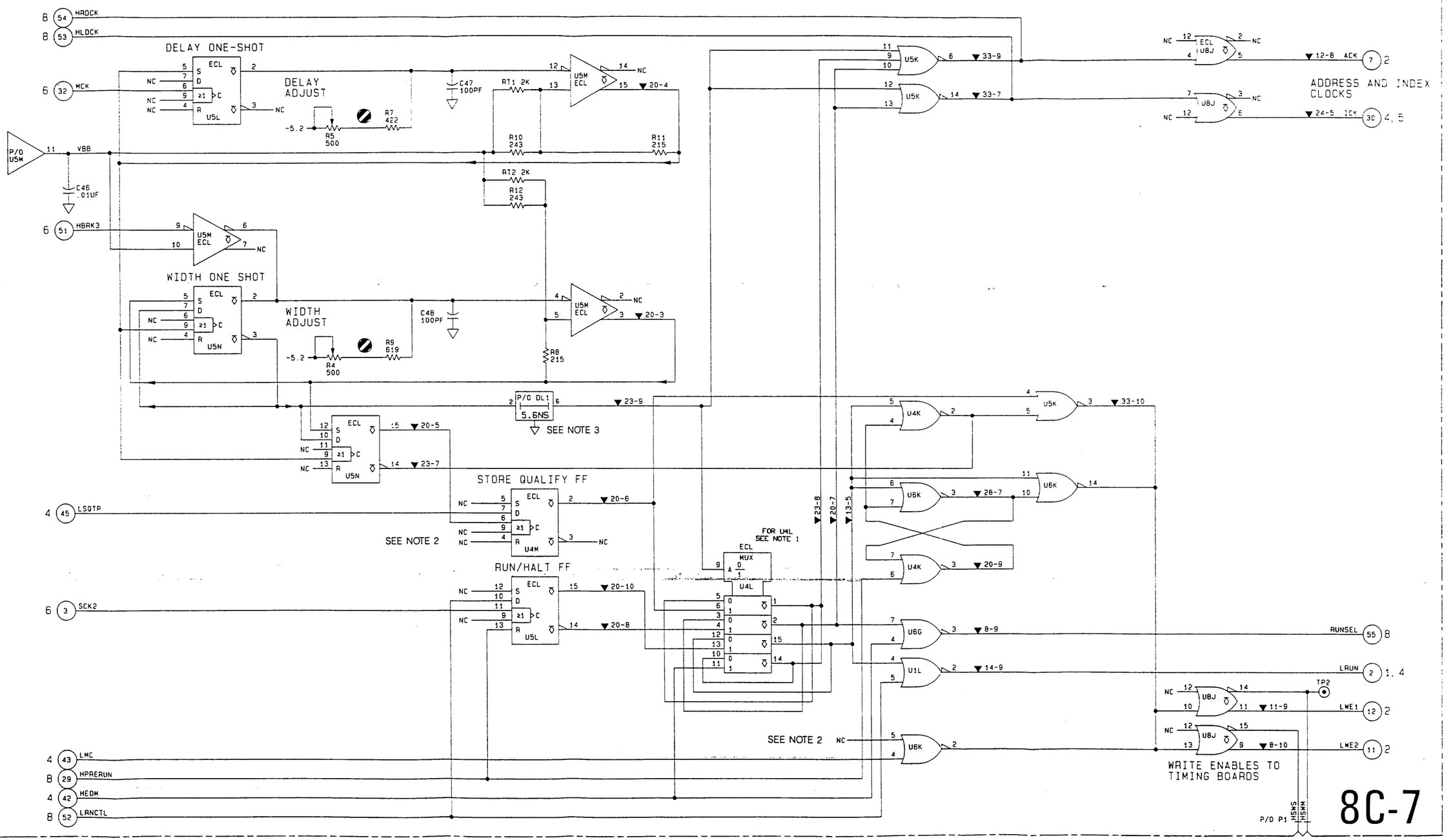
PARTS ON THIS SCHEMATIC

C46-48 DL1 R4-5,7-12 RP8,11-14,20,23-24, 28,33 RT1,2 TP2	U1L,4K-M,5K-N, U6K,8J

P/O A4 STATE MASTER
CLOCK DELAY AND WIDTH



P/O A4 STATE MASTER
CLOCK DELAY AND WIDTH



'ICE IECTIONS

NO.	IC GROUP
5	U1L,4K,M 5K-N,6G,K, 8J
5	U4L

ESCRIPTIONS:

RP VALUE TABLE FOR
E INFORMATION

OF RESISTOR PACK
OR PACK NUMBER (RP)
E BEING PULLED DOWN
BEING PULLED UP

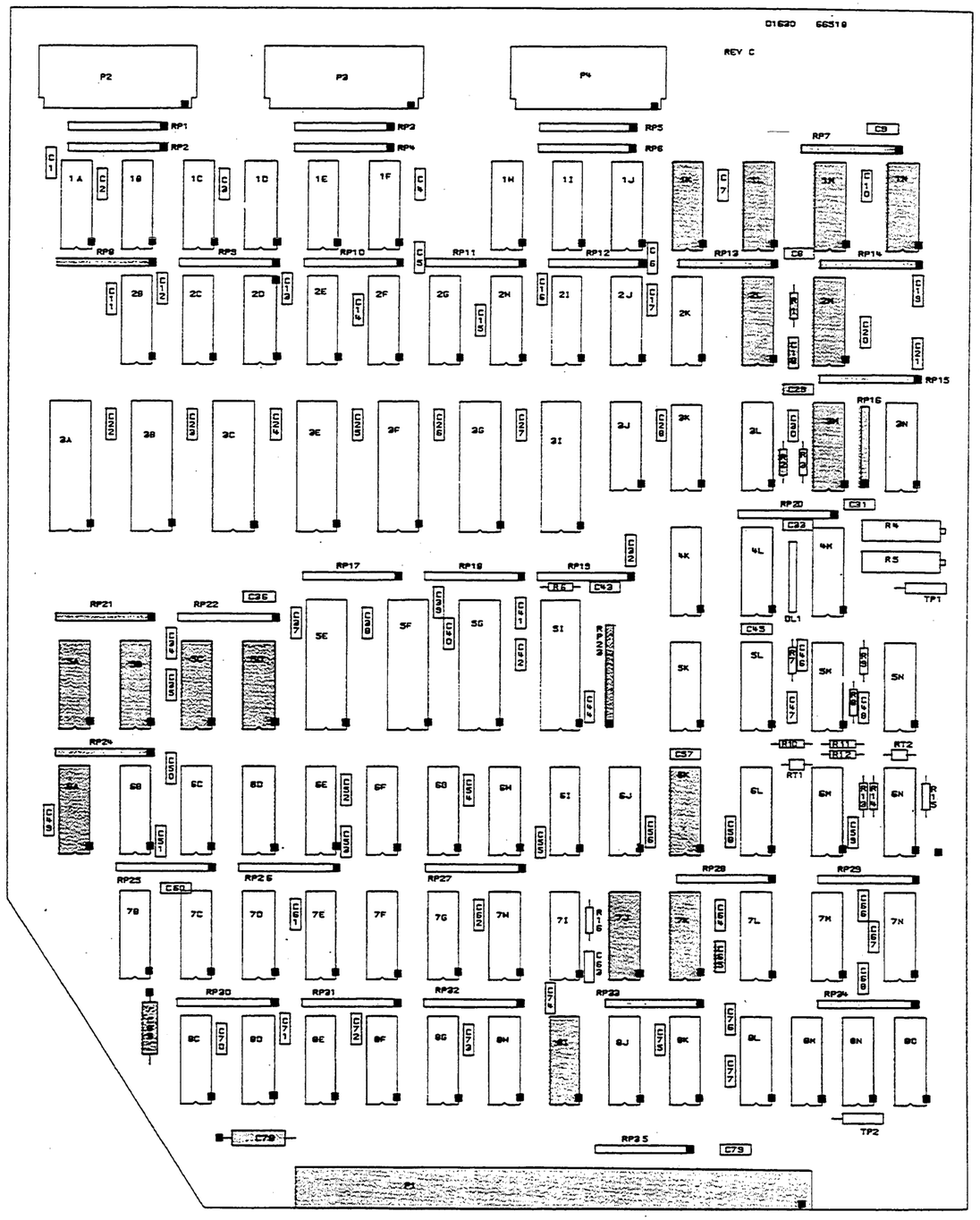
STOR .UE	POWER PIN	VOLTAGE
X 9	1	-5.2
X 9	1	-2.4

SCHEMATIC

U1L,4K-M,5K-N, U6K,8J

8C-7

Schematic 8C-7
Clock Delay and Width
8C-33

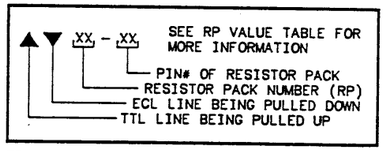


Component Locator for Schematic 8C-8

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1K-1N,2L-2M, U3M,5A-5D,6K, 7J-7K,8I
Vcc(gnd) Vee(-5.2)	16 8	U6A

RESISTOR PACK DESCRIPTIONS

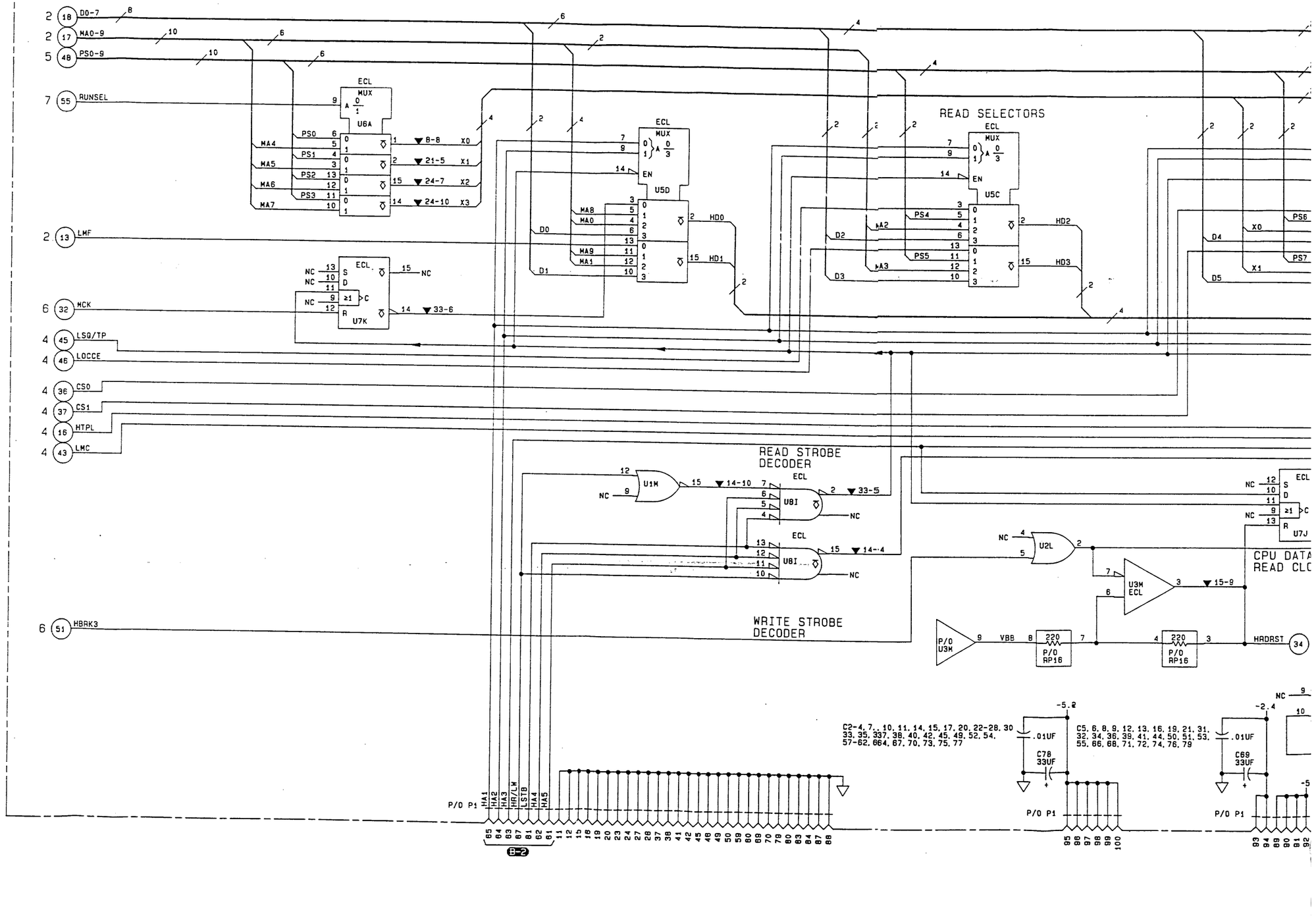


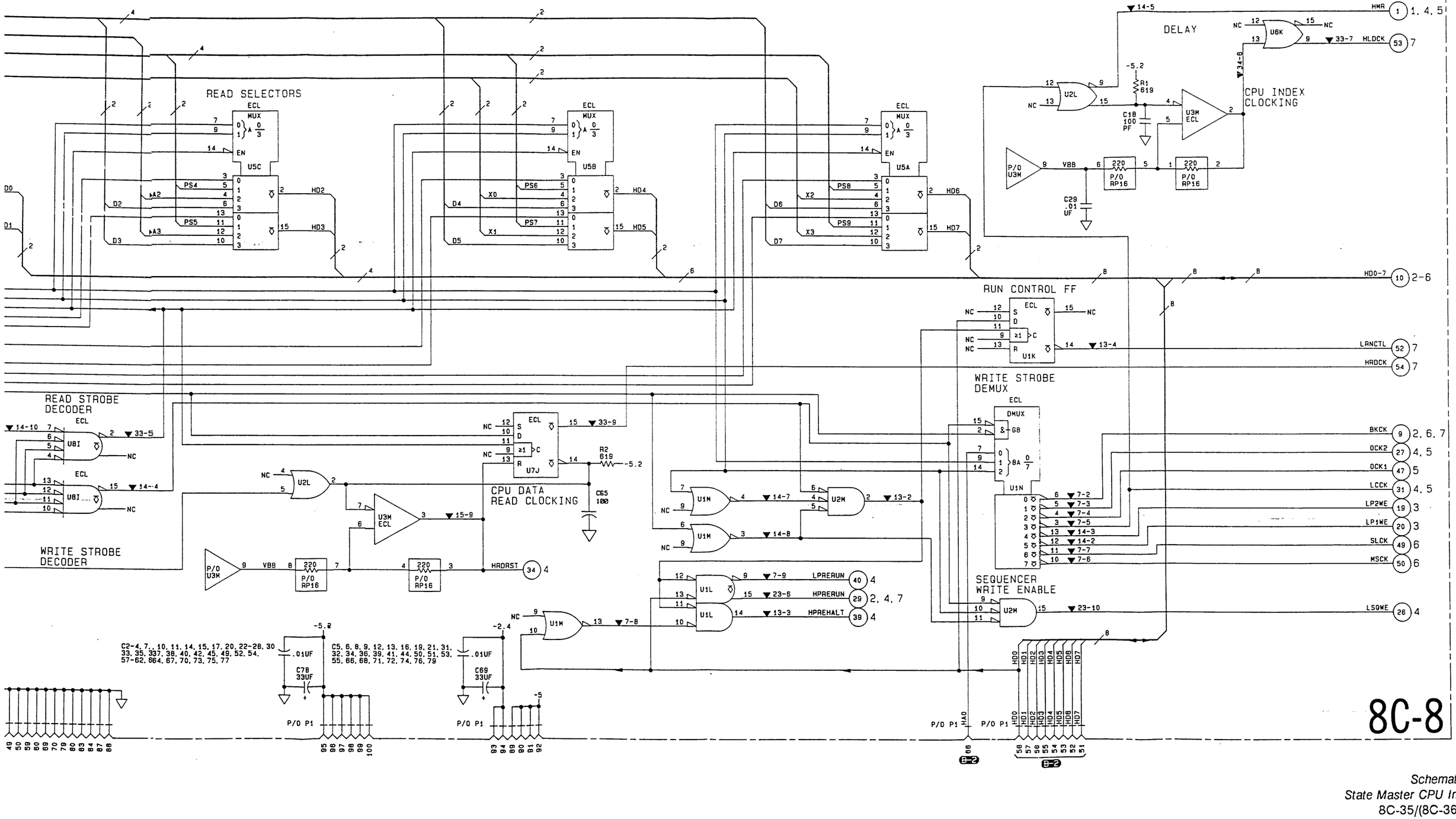
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6	330 X 9	1	-5.2
7-15	100 X 9	1	-2.4
17-35			

PARTS ON THIS SCHEMATIC

C1-42,44-45,49-55, C57-62,64-79 R1,2 RP7-8,13-16,21, RP23,24,33,34 U1K-1N,2L-2M;3M, 5A-5D,6A,K,7J,K,8I	

P/O A4 STATE MASTER
STATE MASTER CPU INTERFACE





Schematic 8C-8
State Master CPU Interface
8C-35/(8C-36 blank)

Service Group 8D Table of Contents

Paragraph		Page
8D-1.	Introduction	8D-1
8D-2.	Timing Block Diagram Theory	8D-1
8D-3.	Theory of Operation	8D-5
8D-4.	Timing Pod and Pod Interface	8D-5
8D-5.	Timing Pod	8D-5
8D-6.	Line Receivers	8D-5
8D-7.	Macrocells	8D-5
8D-8.	Data Samplers	8D-5
8D-9.	Edge Detectors	8D-5
8D-10.	Data Encoders	8D-5
8D-11.	Pattern Detectors	8D-5
8D-12.	State Mode	8D-7
8D-13.	Acquisition RAM	8D-7
8D-14.	Memory Address Counter	8D-7
8D-15.	Block Select	8D-8
8D-16.	Memory Address Latches	8D-8
8D-17.	Memory Full Flip-Flop	8D-8
8D-18.	Prestore Valid Flip-Flop	8D-8
8D-19.	Pattern Duration Filter	8D-11
8D-20.	Glitch Flip-Flop	8D-11
8D-21.	Pattern Latch	8D-11
8D-22.	Pattern Trigger Delay Shift Register	8D-11
8D-23.	Trigger Flip-Flop	8D-11
8D-24.	Sync Trigger Flip-Flop	8D-12
8D-25.	Delay/Poststore Counter	8D-12
8D-26.	Delay	8D-13
8D-27.	Poststore	8D-13
8D-28.	Start Trace	8D-14
8D-29.	End Trace	8D-14
8D-30.	Clock Generation	8D-14
8D-31.	Phase Generation	8D-15
8D-32.	Hold/Encoder State Counter	8D-15
8D-33.	Hold	8D-15
8D-34.	Encoder	8D-15
8D-35.	CPU Interface	8D-15
8D-36.	Read Selectors	8D-15
8D-37.	Mode Select Latch	8D-15
8D-38.	Write Strobe Demultiplexer	8D-16
8D-39.	State Mode	8D-16
8D-40.	Macrocell Removal	8D-16
8D-41.	Macrocell Installation	8D-17
8D-42.	Mnemonics	

List of Illustrations

Figure		Page
8D-1.	State and Timing Acquisition System	8D-3
8D-2.	Macrocell Block Diagram	8D-4
8D-3.	Acquisition Memory and Memory Address Counter	8D-6
8D-4.	Simplified Pattern Duration Filter	8D-9
8D-5.	Pattern Duration Path for 500 us	8D-10
8D-6.	Delay/Poststore Counter	8D-12
8D-7.	Start/Center/End Proportions	8D-13
8D-8.	Phase Waveforms--Timing Mode	8D-14
8D-9.	Memory Write Waveforms--State Mode	8D-16
8D-10.	Timing Pod	8D-19

List of Tables

Table		Page
8D-1.	Resistor-Capacitor Combinations	8D-9
8D-2.	Mnemonics	8D-17

List of Schematics

Schematic		Page
8D-1.	Pod Interface, Acquisition RAM, MAC	8D-21
8D-2.	Delay/Poststore Counter, Pattern Duration Filter	8D-23
8D-3.	Clock Generation/Selection, 200MHz Oscillator	8D-25
8D-4.	Phase Generation	8D-27
8D-5.	Timing Master CPU Interface	8D-29

SERVICE GROUP 8D
TIMING MASTER

8D-1. INTRODUCTION

SAMPLING. The timing master board accepts eight channels from the timing probe. Samples come in as an 8-bit parallel word. Data is compared with thresholds from the CPU board: sampled levels above threshold are high; levels below are low. Storage capacity is 1024 8-bit words. Then, if no trigger pattern has been found, new data will continue to write over old.

SAMPLE RATE. The timing analyzer provides its own sample clocks, which may be varied for different resolutions. Sampling is therefore asynchronous with the system being measured.

TRIGGERING. Before a run the analyzer is programmed to look for a certain pattern of highs or lows on each parallel 8-bit sample. Four of the eight channels may also be programmed to trigger on glitches, or rising or falling edges. When a correct pattern of the proper duration occurs, the analyzer produces a trigger.

TRACEPOINT. The trigger may be delayed while information continues to be stored. Trigger + Delay is defined as Tracepoint.

POSTSTORE. The amount of new data stored after tracepoint determines tracepoint position in displayed memory. Start, Center, or End are the options. For End-on, measurement is stopped immediately after tracepoint, causing about 1K of pre-tracepoint data to be displayed. For Start-on, almost 1K of new data is stored before stopping the measurement, causing tracepoint to be displayed at the beginning.

ARMING. The timing analyzer may be prevented from looking for the trigger pattern until enabled by the state analyzer. The timing trigger may also arm the state analyzer.

8D-2. TIMING BLOCK DIAGRAM THEORY (Figure 8D-1)

PROBE INTERFACE. Collects data from eight pod channels.

MACROCELL. There are two of these custom chips on both the master and slave timing boards. Four of the eight pod channels go into each macrocell. After storing four parallel 4-bit samples, each macrocell outputs a 16-bit word to the RAM at one-fourth the sample rate. Besides this data encoding function, the macrocells contain data and glitch pattern detectors: when an 8-bit sample contains proper pattern, the macrocells emit a trigger signal.

ACQUISITION RAM. This is a 256 x 32 RAM, which is loaded by a 32-bit word from the macrocells (each macrocell sends out 16 bits). The 32-bit word from the two macrocells contains four 8-bit samples. Effective memory size is 1K x 8.

MEMORY ADDRESS COUNTER (MAC). An 8-bit counter which increments at one-fourth the sample rate, as each 32-bit macrocell word is stored in acquisition RAM.

TRACEPOINT LATCH. Saves the contents of the Memory Address Counter when tracepoint occurs.

MEMORY BLOCK SELECT. Chip Select signals for acquisition RAM.

PATTERN DURATION FILTER. Determines whether a trigger pattern lasts long enough.

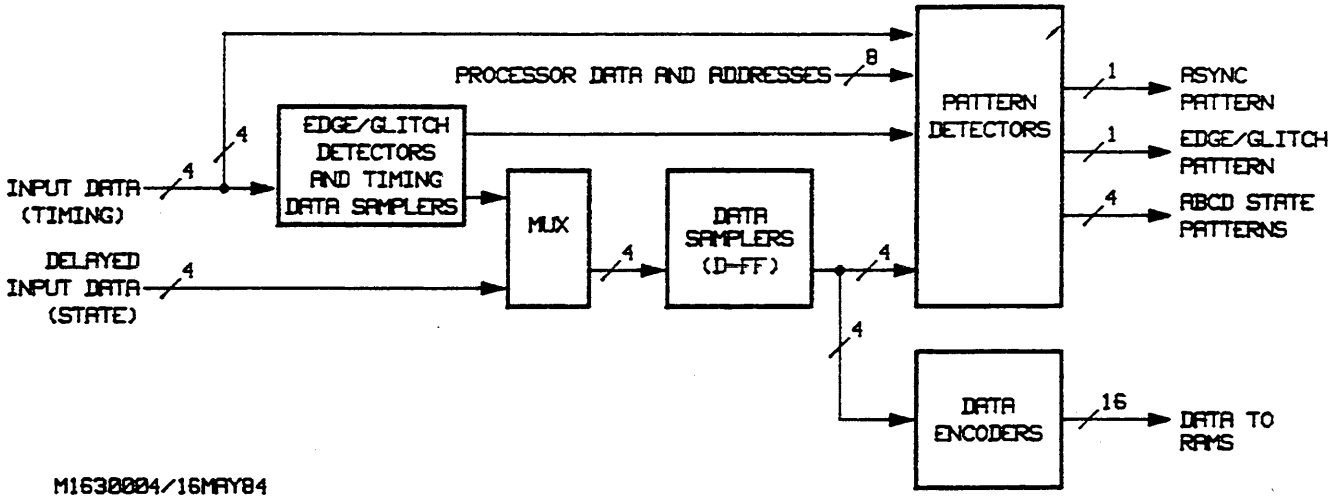
DELAY/POSTSTORE COUNTER. A 16-bit counter for delaying the trigger by as much as four times 59,999 sample states. Five of the counter outputs are decoded for Poststore. The amount of data stored after the trigger determines trigger position in displayed

memory for Start, Center, or End measurements. Terminal count becomes Measurement Complete (MC). The selected decoded output becomes Tracepoint (TP).

CLOCK GENERATION/SELECTION. Contains a 200 MHz oscillator, and frequency selection multiplexers for choosing sample rate. The CPU supplies frequencies below 5 MHz.

PHASE GENERATOR. Divides the timing clock into four phases for running various analyzer functions. For example, to allow for settling time, memory is written on Phase D, and the Memory Address Counters are incremented on Phase B.

CPU INTERFACE. Allows CPU programming and interrogation.



CAUTION

When either master or slave timing boards are installed in the service slot in the upright position, forced air must be maintained across the macrocell heat sinks.

Figure 8D-2. Macrocell Block Diagram

8D-3. THEORY OF OPERATION

8D-4. Timing Pod and Pod Interface (see schematic 8D-1)

8D-5. TIMING POD (see Figure 8D-10). The timing pod compares eight data channels against a single threshold, and converts each single input to two complementary ECL inputs for transmission to the timing board.

8D-6. LINE RECEIVERS The Line Receivers convert the differential ECL signals from the pod to two single-ended outputs. One set of outputs is delayed by 19 ns to guarantee zero hold time on data in the State Mode. The other set of outputs goes directly into the macrocells for use in the Timing Mode.

8D-7. Macrocells (see schematic 8D-1)

There are two macrocells, each handling four channels, on both the primary and optional secondary timing boards. The macrocells are a custom gate array. The design can be broken down into four functional blocks:

1. Data Samplers.
2. Edge Detectors.
3. Data Encoders.
4. Pattern Detectors.

8D-8. DATA SAMPLERS. The Data Samplers clock in data for State, Time, or Glitch Modes.

8D-9. EDGE DETECTORS. The Edge Detectors find edges in the Timing Mode by looking for a transition on data between sample clocks. Two of the four macrocell input channels have edge detectors, allowing 4-channel glitch detection and triggering on each group of eight timing channels. For each data input with glitch detection, there are two positive and two negative edge detectors.

8D-10. DATA ENCODERS. The Data Encoders convert four parallel bits of high speed sampled data into 16 parallel bits of low speed data for writing into acquisition RAM. In State Mode the data encoders pass the sampled data directly to the 16 outputs, each bit of sampled data being output on four pins.

8D-11. PATTERN DETECTORS. The Pattern Detectors look for 1/0/X on each of the data inputs. During Halt, the CPU programs the specified pattern into the macrocells' internal registers. When the proper combination of highs, lows, don't cares, or glitches occurs, the macrocells will emit either LTM or HGM. LTM goes true when the preselected pattern is valid at the pod input. HGM is true whenever the correct glitch pattern appears on the selected data channels.

8D-12. STATE MODE. In State Mode the macrocells serve the same purpose as Pattern Recognition RAM on the state board. Four patterns, A-D, may be stored in the macrocells internal registers. The state pattern detectors look at the sampled data, while the timing pattern detectors look directly at the input data (and at the edge detector outputs, when in Glitch Mode).

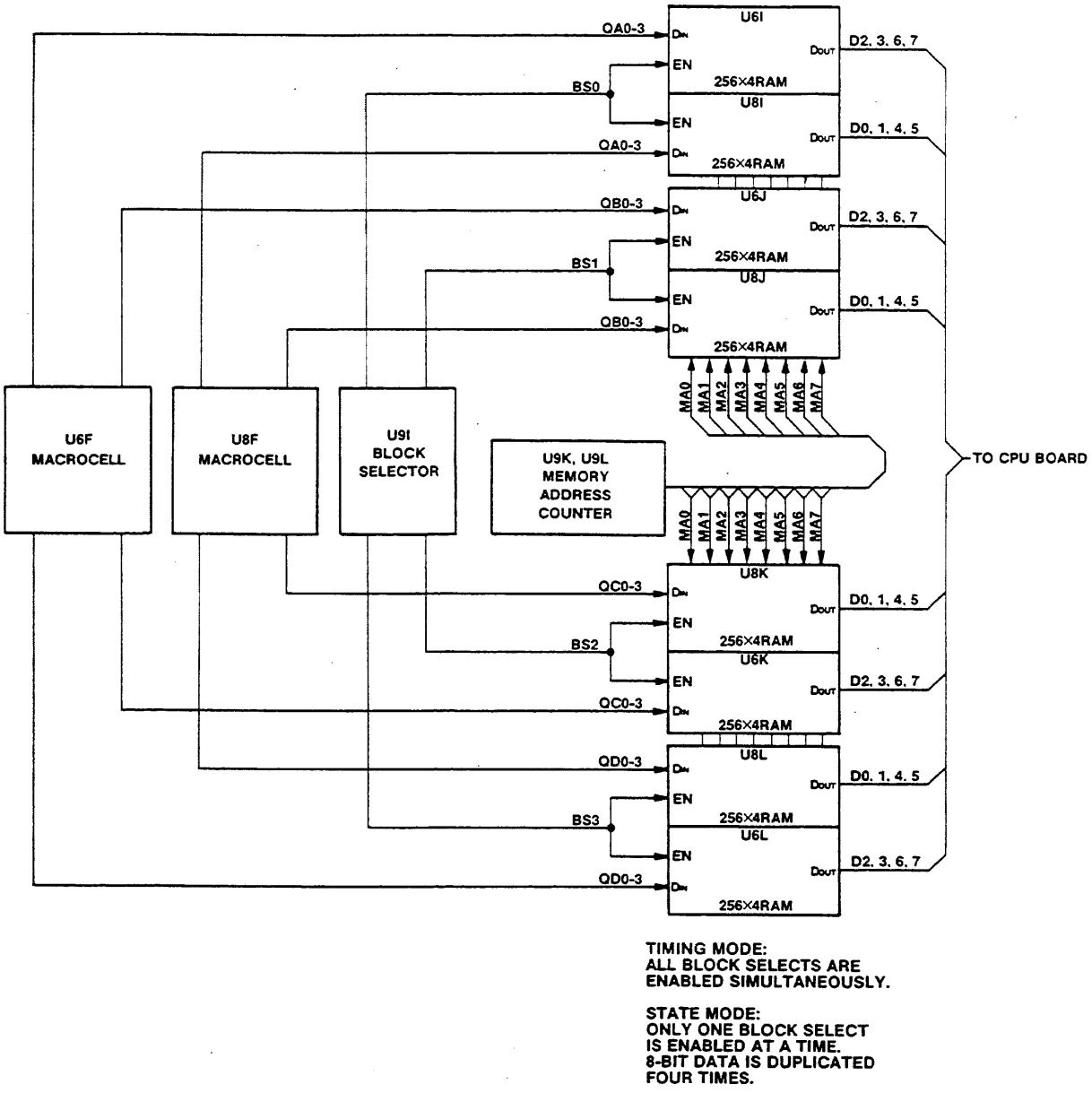


Figure 8D-3. Acquisition Memory and Memory Address Counter

8D-13. Acquisition RAM (see schematic 8D-1)

The RAM is organized 32 bits wide by 256 words deep. Since the 32-bit output data from the two macrocells is demultiplexed or fanned out to four times its width of eight channels, it is loaded into RAM at one-fourth of the sample speed, 32 bits at a time.

Each 16-bit parallel word from one macrocell contains four 4-bit data samples. The RAM for each macrocell is therefore, in effect, 1K x 4. With two macrocells and two groups of RAM, the effective memory size is 1K x 8.

8D-14. Memory Address Counter (see schematic 8D-1)

The Memory Address Counter is an 8-bit counter which keeps track of where data is being stored. Since memory is loaded 32 bits at a time, to a depth of 256, the counter only needs to count to 256 in order to store 1024 8-bit samples.

The Phase Generator increments the Memory Address Counter when writing during acquisition. The CPU increments the counter during reads.

The Memory Address Counter has three decoded outputs: MACTC1 (terminal count from the low order counter, U9K); MA7, the eighth, or most significant address bit; and MACTC2 (terminal count from the high order counter, U9L). These outputs indicate when the counter has counted 15, 128, or 240, i.e., the Start, Middle, or End of the 32 x 256 word memory.

8D-15. Block Select (see schematic 8D-1)

Memory chip-selects (U9I,9J) are controlled differently for State Mode, Timing Mode, and CPU Read Mode.

Timing Mode — All chip-selects are true. Four 8-bit samples are stored simultaneously as a 32-bit word.

State Mode — The 8-bit data word is now duplicated in four places on the macrocell outputs. At sample time, the Block Selector holds one chip-select true, enabling two 4-bit wide RAMs to store one byte. After four 8-bit samples, the Block Selector increments the Memory Address Counter. (see figure 8D-9).

CPU Read — Since RAM outputs are bussed 8 wide, two 4-bit RAMs at a time are enabled for reading. The Block Selector now enables two RAMs, as in State Mode; but now the Block Selector is clocked by the CPU clock, instead of the state sample clock.

8D-16. Memory Address Latches (see schematic 8D-1)

These latches hold the current memory address, allowing the CPU to unload memory at the end of a run. When Measurement Complete goes true, the CPU reads the latches to determine tracepoint position in acquisition memory.

8D-17. Memory Full Flip-Flop (see schematic 8D-1)

In the Run Mode the Memory Address Counter is continually running. When the counter has gone around once, reaching terminal count, the Memory-Full FF emits LMF, indicating memory has been completely filled at least once. The Memory Full FF is not reset until master reset occurs at the end of a run. The Memory Full FF ensures that the memory has been filled only with valid data.

8D-18. Prestore Valid Flip-Flop (see schematic 8D-1)

A trigger cannot occur until the Memory Address Counter indicates that memory has been sufficiently filled: For a Center-on measurement, half of memory must be filled;

for End-on, all of memory; and even in Start-on, 56 samples are taken to allow a pre-trigger display.

Depending on whether the measurement is Start, End, or Center, one of the three memory address counter decoded outputs--MACTC1, MACTC2, or MA7--is selected to arm the trigger. This ensures a full load of prestore in the Timing Mode.

8D-19. Pattern Duration Filter (see schematic 8D-2)

The operator can specify minimum pattern durations. The Pattern Duration Filter determines whether the pattern trigger (LTM) from the macrocell satisfies a selected minimum time interval.

The Pattern Duration Selector (U4C) chooses the minimum pattern duration. Depending on the duration selected, one or more of its outputs will turn on differential pairs in the transistor arrays (U2A,3A,3B). The transistors switch in different RC time constants, causing the output of U2D-14 to ramp down at different rates. The ramp must decline fast enough to reach Schmitt Trigger threshold before the input signal goes low again.

As shown in Figure 8D-4, the transistors are merely switches which connect different sets of resistors and capacitors into the circuit. The resistors provide an "R" multiplier of 2, 5, or 10; and the capacitors provide a "C" multiplier of powers of 10. As shown in Table 8D-1, the "R" multiplier times the "C" multiplier gives the time duration.

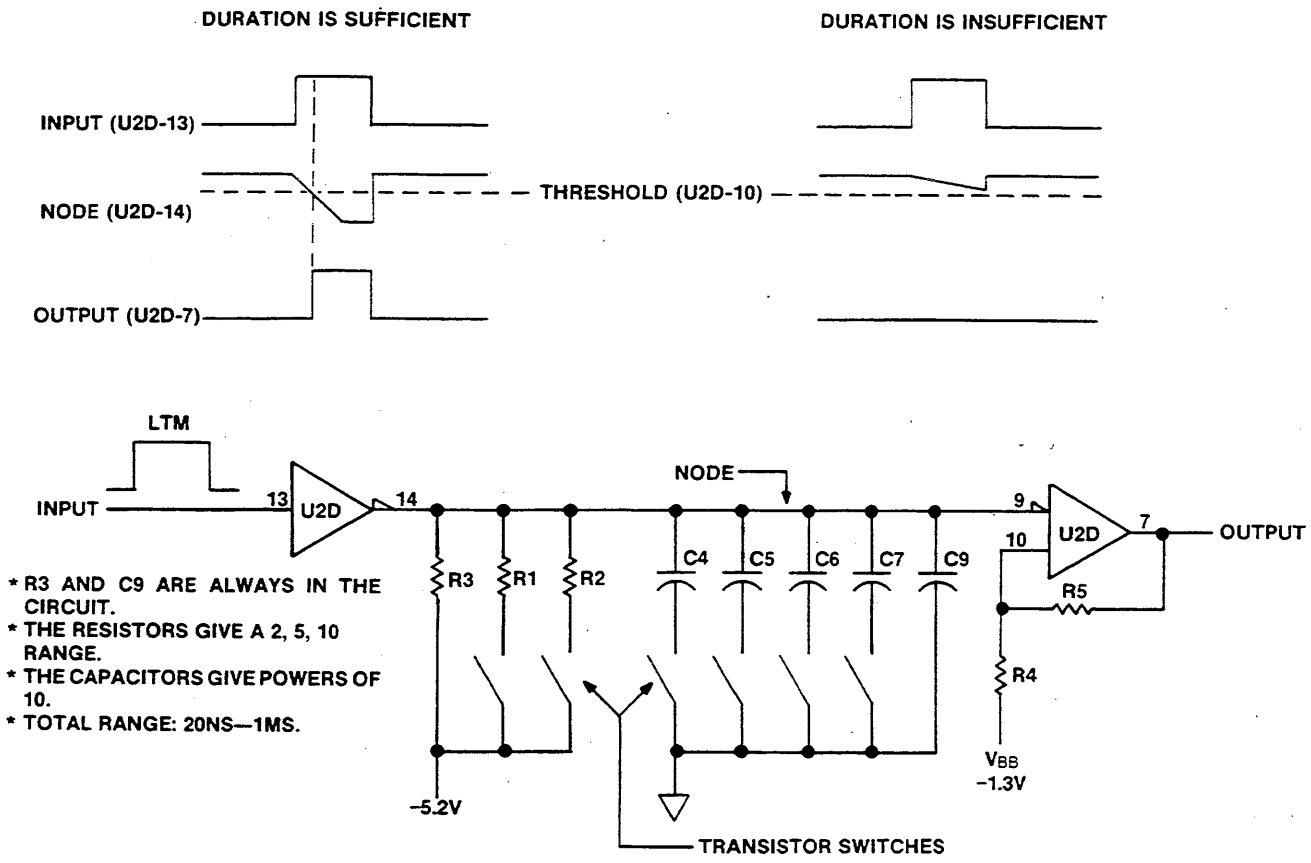


Figure 8D-4. Simplified Pattern Duration Filter

Table 8D-1. Resistor-Capacitor Combinations

RESISTORS	R MULTIPLIER
R3 (1.58K)	10
R1||R3 (1.71K||1.58k)	5
R1||R2||R3 (1.71k||681||1.58k)	2
CAPACITORS	**C MULTIPLIER**
C9 (300pf)	10^{-8}
C7 (3600pf)	10^{-7}
C6 (.04μf)	10^{-6}
C5 (.4μf)	10^{-5}
C4 (4μf)	10^{-4}

R multiplier x C multiplier = seconds

For the following Pattern Duration detailed theory see figure 8D-5 and table 8D-1.

Let's assume the operator has selected a minimum time interval of 500 us. We need a resistor multiplier of 5 and a capacitor multiplier of .0001. As shown in table 8D-1, R1 in parallel with R3 gives the resistor multiplier; and C4 gives the capacitor multiplier.

Pin 15 of the Duration Selector must go low to switch in R1; pin 13 must also go low to switch in C4.

A low on pin 15 turns on the left side of U2A, which then turns on U3A. R1 is now connected directly to -5.2V, putting it in parallel with R3. This gives us a resistor multiplier of 5.

A low on pin 13 turns on the right side of U3A, which turns on U3C. C4 is now connected to ground in parallel with the much smaller C9, which it swamps out. We now have C4 in series with the parallel combination of R1 and R3, which gives us a duration of 500 us.

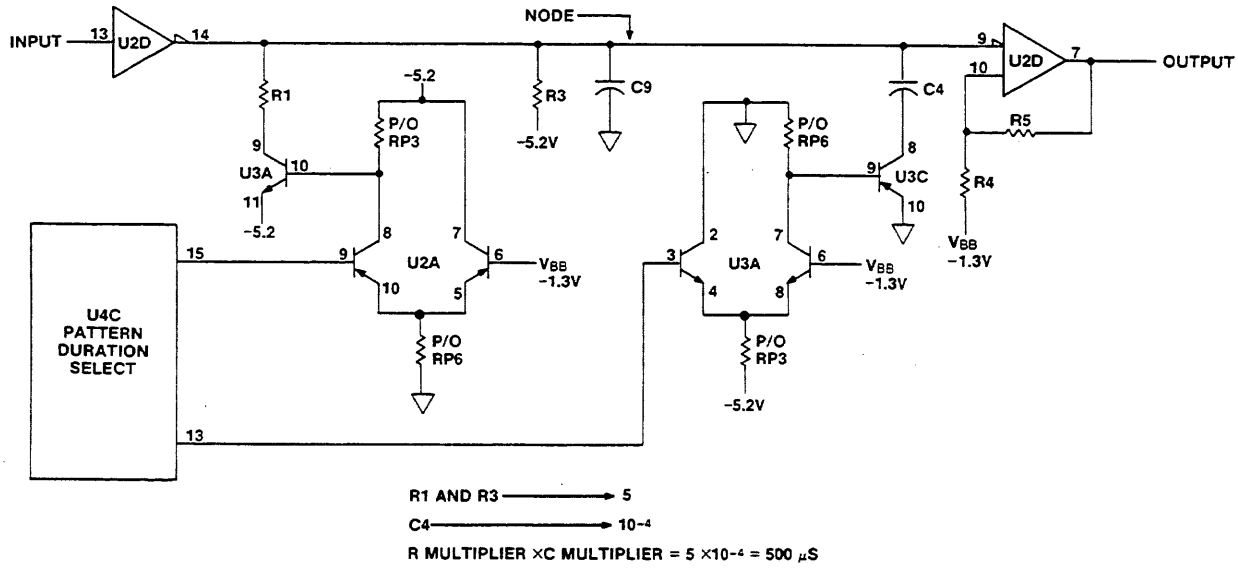


Figure 8D-5. Pattern Duration Path for 500 us

8D-20. Glitch Flip-Flop (see schematic 8D-2)

The Glitch FF synchronizes the glitch trigger HGM, from the output of the macrocell, with the timing clock TCK2.

8D-21. Pattern Latch (see schematic 8D-2)

The Pattern Latch synchronizes the asynchronous pattern trigger from output of the pattern duration filter with the timing clock TCK2.

8D-22. Pattern Trigger Delay Shift Register (see schematic 8D-2)

Because the glitch trigger HGM is delayed in the macrocell relative to the pattern trigger LTM, the two need to be re-aligned before they can be ANDed at the input to the Combination FF (U3G-10). The Delay Shift Register delays the pattern trigger by four sample clocks to synchronize it with the glitch trigger.

8D-23. Trigger Flip-Flop (see schematic 8D-2)

LTM and HGM are wire-ANDed at the input to the Trigger FF (U3G-10), which synchronizes the ANDed trigger with the timing clock TCK2. The second half of the FF (U3G-7) latches the trigger high even after the pattern goes away.

8D-24. Sync Trigger Flip-Flop (see schematic 8D-2)

The Sync Trigger FF sychronizes the trigger with Phase C (LPHC), which is one fourth the sample rate (the rate that data is stored in memory).

8D-25. Delay/Poststore Counter (see schematic 8D-2)

When a valid trigger pattern is recognized, data will still continue to be stored. The trigger may be delayed by some amount. This delayed trigger is called Tracepoint--trigger + delay. And even when tracepoint occurs, the measurement may still not be stopped. The additional data stored after tracepoint is called Poststore--the distance in memory between Tracepoint and Measurement Complete. Poststore determines where tracepoint will be displayed--at the Start, Center, or End. Measurement Complete, then, equals trigger + delay + poststore.

8C-26. DELAY. When the operator wishes to observe data downstream from a valid trigger pattern, the CPU will pre-load the delay counter with the amount of delay desired before data storage is to be stopped. The valid trigger signal starts the delay counter. When the counter reaches terminal count (FFFFH), it stops further data storage--Measurement Complete.

For maximum delay, the CPU would load the counter to 0000H: then the counter must count all the way to FFFFH to reach terminal count. Minimum delay would be a pre-load of FFFFH, since terminal count then occurs immediately. Because the counter runs at one-fourth the sample rate, maximum possible delay, plus poststore, is four times 65,536 samples.

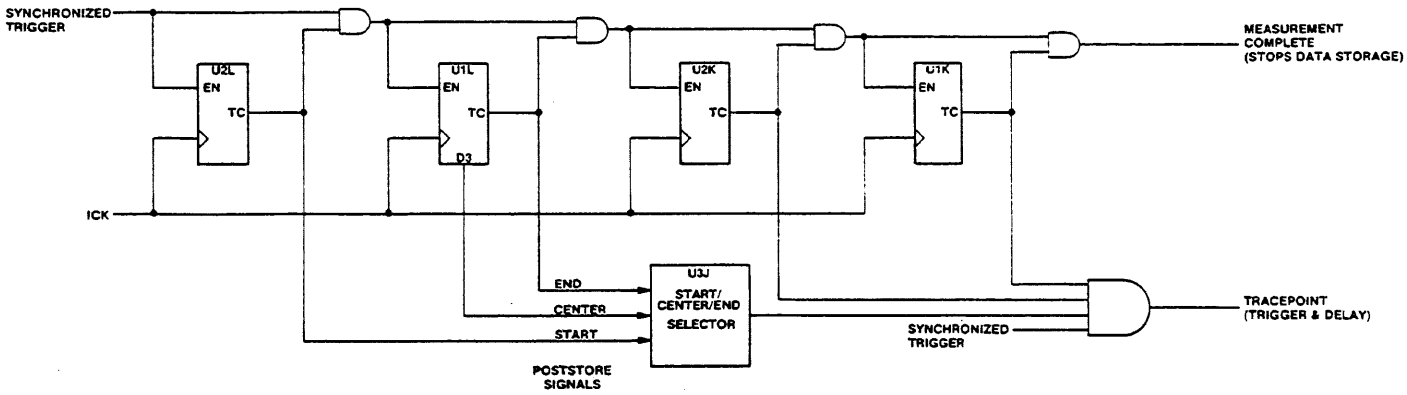


Figure 8D-6. Delay/Poststore Counter

8D-27. POSTSTORE. Assuming no delay, the counter would be loaded to the following values for Start, Center, or End trace.

START: FF0FH

CENTER: FF80H

END: FFF0H

For Start, Center, and End, display memory will therefore contain the proportions of prestore and poststore data shown in figure 8D-7.

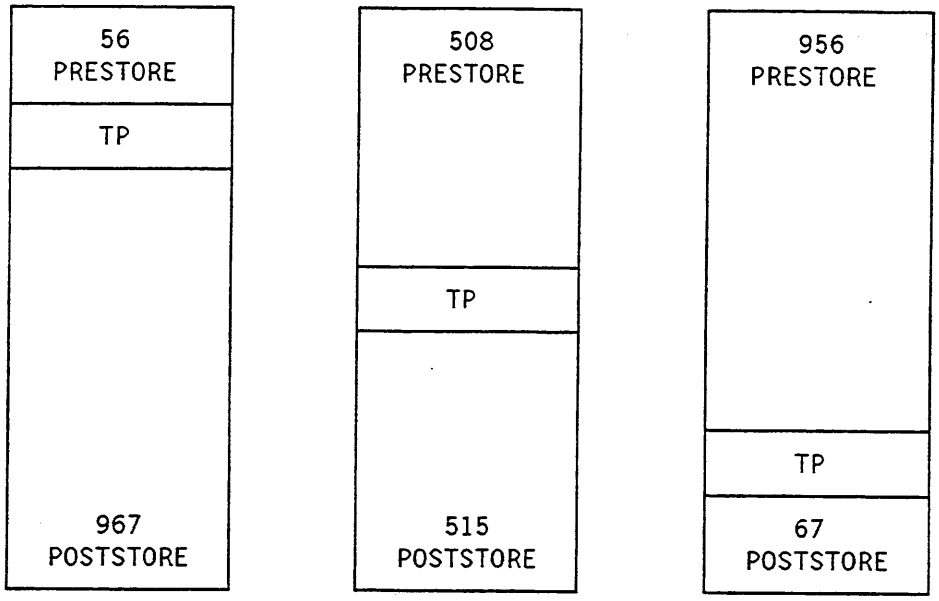


Figure 8D-7. Start/Center/End Proportions

8-28. START-TRACE. For Start-Trace, the counter is preloaded to FF0FH, but it cannot begin counting until the trigger has been armed by the Prestore Valid FF, which ensures a minimum prestore. This allows the trigger to be observed even when it it occurs at the beginning of the display. In the case of Start-Trace, minimum prestore is 56 samples.

For Start-Trace, The CPU has previously programmed the Start/Center/End Selector (U3J) to select the terminal count of the least significant counter (U2L). For a preload of FF0FH, this terminal count will be true as soon as the delay counter begins counting. Tracepoint Latched will then occur immediately. Tracepoint will be stored in one of the next four positions after the prestore of 56 samples.

For poststore after a start-trace, the delay counter must now count from FF0FH to its terminal count, FFFFH, before the measurement is stopped. Poststore is then approximately four times the subtraction of FFFFH minus FF0FH.

When delay is desired, it is subtracted from the Start-Trace preload, FF0FH. For example, a delay of 60 sample clocks would require the

delay counter to be loaded with FF0FH minus 15--since the counter counts at 1/4 the sample rate--or FF00H. The counter must then count 15 additional times to reach FFFFH and stop the measurement.

8-29. END-TRACE. Now the delay counter is preloaded to FFF0H, and the Start Center/End Selector selects the terminal count of the second counter (U1L). The Prestore Valid FF arms the trigger after approximately 956 samples have been stored. If a trigger has occurred, the delay counter is started and reaches terminal count after approximately 60 samples of poststore.

Any desired delay is subtracted from the End-Trace preload of FFF0H. For a delay of 960 sample clocks, for example, the counter preload would be FF00H. The counter must then count an additional 240 times (at 1/4 the sample rate) before it can stop the measurement.

8D-30. Clock Generation (see schematic 8D-3)

The Clock Generator consists primarily of a 200 MHz oscillator, dividers, and multiplexers which select sample rates for the timing analyzer.

The timing clock is selected by the CPU at the multiplexer (U8C). The multiplexer selects 10 MHz, 20 MHz, 40 MHz, 100 MHz, 200 MHz, or the CPU clock. The CPU clock is used for Self-Test. The frequency selected by the multiplexer is further divided in the final flip-flop (U9D) and sent to the motherboard and other parts of the timing system.

The Start Synchronizers are two flip-flops (9C) making up a shift register which allows the clock to start cleanly.

8D-31. Phase Generation (see schematic 8D-4)

The phase generator uses the timing clock (TCK) to generate four phases which ensure the proper relationship between different parts of the timing analyzer.

Phase A drives the macrocells.

Phase B drives the address and index clocks, which clock the memory address counter and the poststore counter, respectively.

Phase C drives the macrocells. The trigger signal from the pattern duration filter is synchronized to Phase C.

Phase D drives the Write Enable Selector (U9H), which writes incoming data samples into RAM (via LWE1, LWE2). Also clocks the Memory Address Latches (U5K,5L), which store the current address of the Memory Address Counters when Tracepoint goes true.

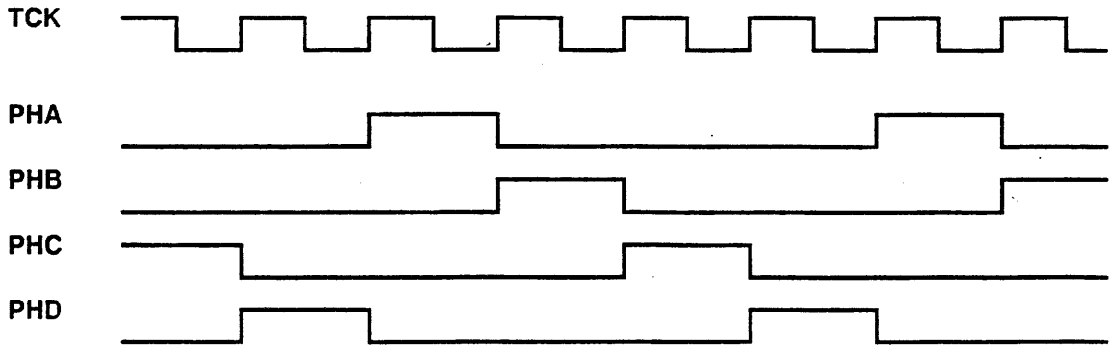


Figure 8D-8. Phase Waveforms--Timing Mode

8D-32. Hold/Encoder State Counter (see schematic 8D-4)

This counter performs a dual function.

8D-33. HOLD. At the beginning of a run, the counter counts to 16 before de-activating the HOLD line. As long as the HOLD line is active, no data is clocked into memory. This clears the macrocells of old data from past runs, so that only new data is stored.

8D-34. ENCODER. The two least significant counter bits track the macrocell encoders, which store four bytes at a time in memory. The latched trigger stops the counter. When the counter is stopped, the CPU reads the code, and uses this and the Memory Address Counter output to determine exactly where in memory the trigger is stored.

8D-35. CPU Interface (see schematic 8D-5)

8D-36. READ SELECTORS (U3k-4K, U3L-4L). By multiplexing Status, Data, and Address bits, the Read Selectors allow the CPU to interrogate the timing analyzer. The CPU uses the address information to load all the timing acquisition memory data into its own RAM on the CPU board. The tracepoint address and the two encoder bits (ENC0, ENC1) tell the CPU where to find tracepoint in acquisition memory. HMEMFUL, another status bit, tells whether all the data in timing acquisition memory is valid, in case case of a partial run.

8D-37. MODE SELECT LATCH (U5C). The CPU programs some of the analyzer via the Mode Select Latch. By means of PS0 and PS1, it can select Start, Center, or End Trace. When HARMD is high, the Timing Analyzer can arm the State Analyzer; when it is low, State arms Timing. HBNCD sends the trigger from the output of the Pattern Duration Filter to the BNC connector. HSSEL determines whether the timing board is in the State or Timing mode. HGL selects Glitch Mode.

8D-38. WRITE STROBE DEMULTIPLEXER (U4D). The CPU writes to the timing analyzer, providing clocks and enable signals for different analyzer functions, by means of the Write Strobe Demultiplexer. The following is a list of clocks coming out of the demux:

LPE1,LPE2	Parallel enable signals for the Delay/Poststore Counter.
CPUCK	Timing clock from the CPU for PV purposes.
SCK	Allows the CPU to abort a run, to generate HRST, or to break the measurement complete loop for Self-Test.
LMACRST	Resets the Memory Address Counter.
PCK	Loads the Pattern Duration Selector.
SELCK	Programs the sample rate.
HRST	Master Reset for the timing analyzer.
LOADCK	Loads the index clock to the poststore counter.
READCK	Loads the address clock to the memory address counter.

8D-39. STATE MODE. The timing master board can be run in the state mode as a part of the state analyzer. In this case HSCM (State Clock Master) and HSWM (State Write Master) are supplied by the state board. Figure 8D-9 shows the relationship between the different memory write signals in the state mode. Unlike the timing mode, where all block selects are active at the same time for writing the 32-bit word, only one block select at a time is active in the state mode.

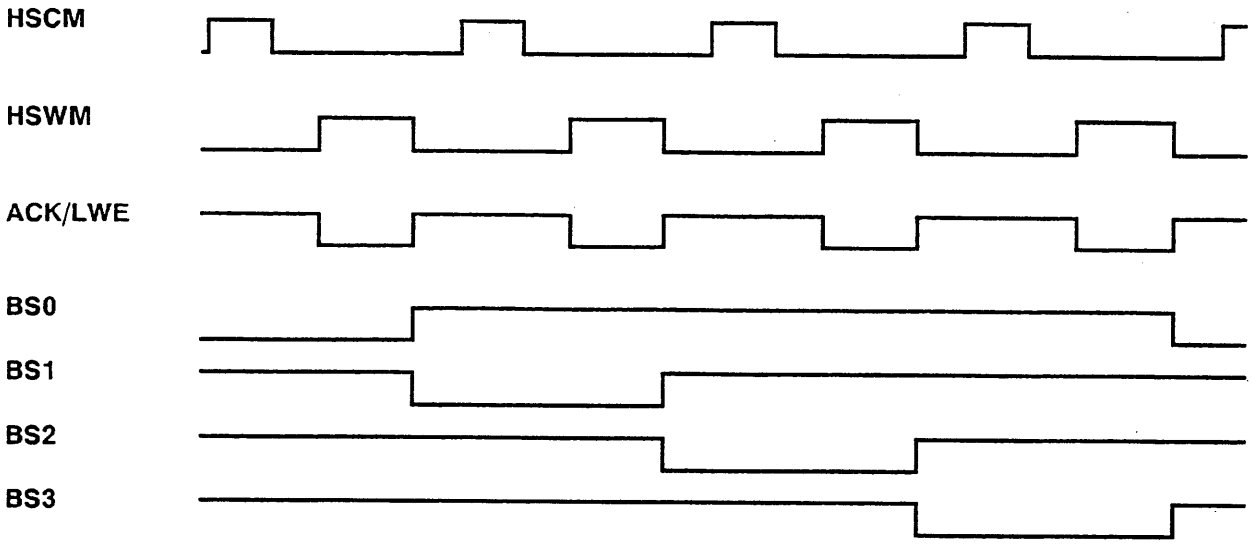


Figure 8D-9. Memory Write Waveforms--State Mode

8D-40. MACROCELL REMOVAL

a. Gently pry the socket retaining clip away from the heatsink.

b. Carefully pull the heatsink sideways away from the socket. The macrocell chip may come away with the heatsink.

c. Remove the macrocell chip if it is still in the socket.

8D-41. MACROCELL INSTALLATION

a. Place the macrocell chip (circuit side down) in the socket. The socket is keyed so that the macrocell chip will fit only one way.

b. Put a thin coating of thermal compound on the back of the macrocell chip.

c. Place the two small guide pins on the heatsink into the socket. The heatsink is keyed so it fits only one way.

d. Gently push down on the heatsink and flip the socket retaining clip up and over the large heatsink guide pins.

8D-42. MNEMONICS

The following signals, listed in alphabetical order, are used on the Timing Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing Master board are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8D-2. Mnemonics

Mnemonic	Description
A0-7	Address outputs from the memory address latches.
ACK	Memory Address counter clock. Increments the address counters.
CPUCK	CPU clock. Sample clock during Self-Test.
D0-7	Memory data outputs.
ENC0,1	Two-bit code pointing to the RAM where tracepoint is stored.
GS1	Ground sensing from the timing probe.
HA0-7	Motherboard address bus.
HABORT	Abort. Allows a user to stop a run.
HARMD	Arm drive. Timing arms State. When low, State arms Timing.
HBNCD	BNC drive. Enables pattern trigger to drive BNC output.
HD0-7	Motherboard data bus.
HGL	Glitch. Allows glitch detection and triggering on 4 channels.
LBRK	Break. Used in Self Test to break the Measurement Complete loop.
LAM LBM LCM LDM	State patterns from Timing Master to State.
HGM	Glitch trigger (master), from the macrocells.
HMACRD	Memory address counter read. Enables MAC read.
HMC	Measurement complete. Stops data sampling and storage.
HMSS	Macrocell State select. Puts macrocells in the State Mode--with HSSEL puts the Timing Master board in the state mode.
HOLD	Prevents data storage (MAC counting) until 16 sample clocks pass.

Table 8D-2. Mnemonics (Cont'd)

Mnemonic	Description
HPHA-D	Four timing clock phases for different analyzer functions.
HPVD	Prestore valid. Enables trigger to occur after minimum prestore.
HR/LW	High read/low write. The CPU either programs or reads analyzer.
HRST	Reset. Master reset derived from the CPU.
HSCM	State clock (master). State sample clock to the macrocells.
HSSEL	State select. With HMSS puts Timing in the State Mode.
HTPL	Tracepoint latched. Trigger + Delay Latched.
HTRIG	Latched trigger. From the ANDed glitch and pattern triggers.
HTSEL	Timing select. Selects Timing block select mode (all true).
ICK	Index clock. Increments the delay/poststore counter and the run-status latches.
LARM	ARM. Allows the valid timing pattern from the macrocells to pass on to the pattern duration filter.
SELCK	Select clock. Allows the CPU to select the sample rate.
TCK1-3	Timing sample clock.
THR1	Threshold to timing probe.
LE2	Macrocell programming enable.
LMACRST	Memory address counter reset derived from the CPU.
LMCI	Measurement complete interrupt to the CPU.
LMF	Memory full (at least once) from the Wrap-around FF.
LOADCK.	Load Clock. The CPU loads the delay/poststore counter.
LPE1,2	Poststore enables. Enable delay/poststore counter for loading.
LSTB	CPU strobe to read or write to the analyzer.
LTM	Valid timing pattern (master), from the macrocells.
LWE1,2	Write enables to acquisition RAM, from timing clock (phase D).

Table 8D-2. Mnemonics (Cont'd)

Mnemonic	Description
MA0-7	Memory address counter outputs.
MA7	Memory address counter output indicating count 128 to the Start/Center/End Selector.
MACTC1	Memory address counter terminal count (15) from first counter to the Start/Center/End Selector.
MACTC2	Memory address counter terminal count (255) from second counter to the Start/Center/End Selector.
PCK	Pattern clock. Clocks the pattern duration selector.
PS0,1	Selects poststore decoded states for Start/Center/End.
READCK	Read clock. Increments the memory address counter each time the CPU reads memory.
SCK	Stop clock. Allows the CPU to abort or break operation.

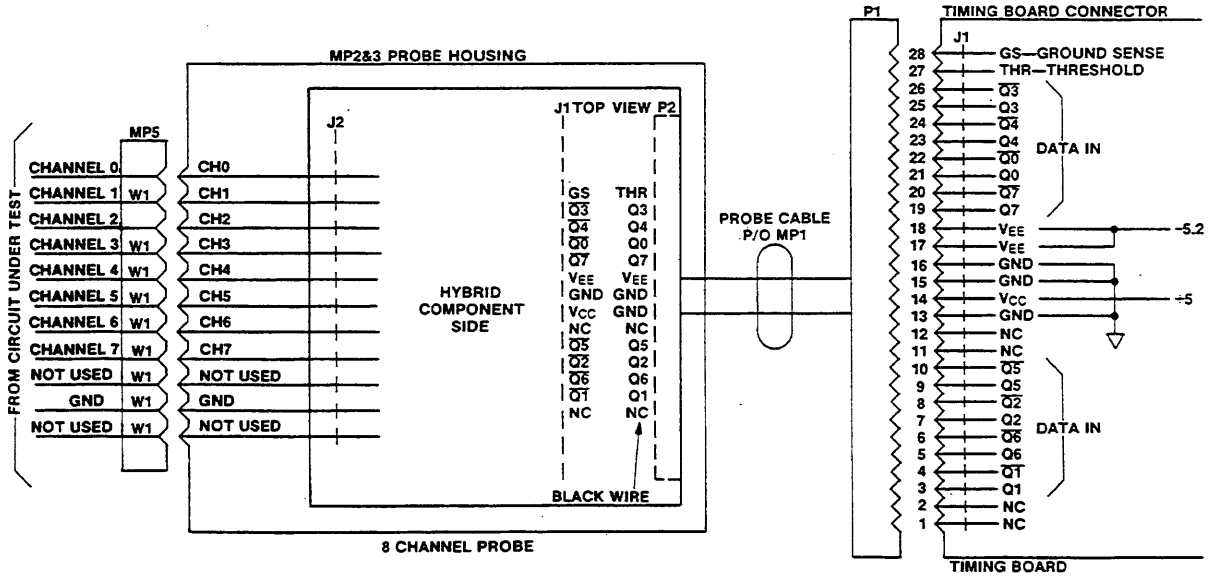
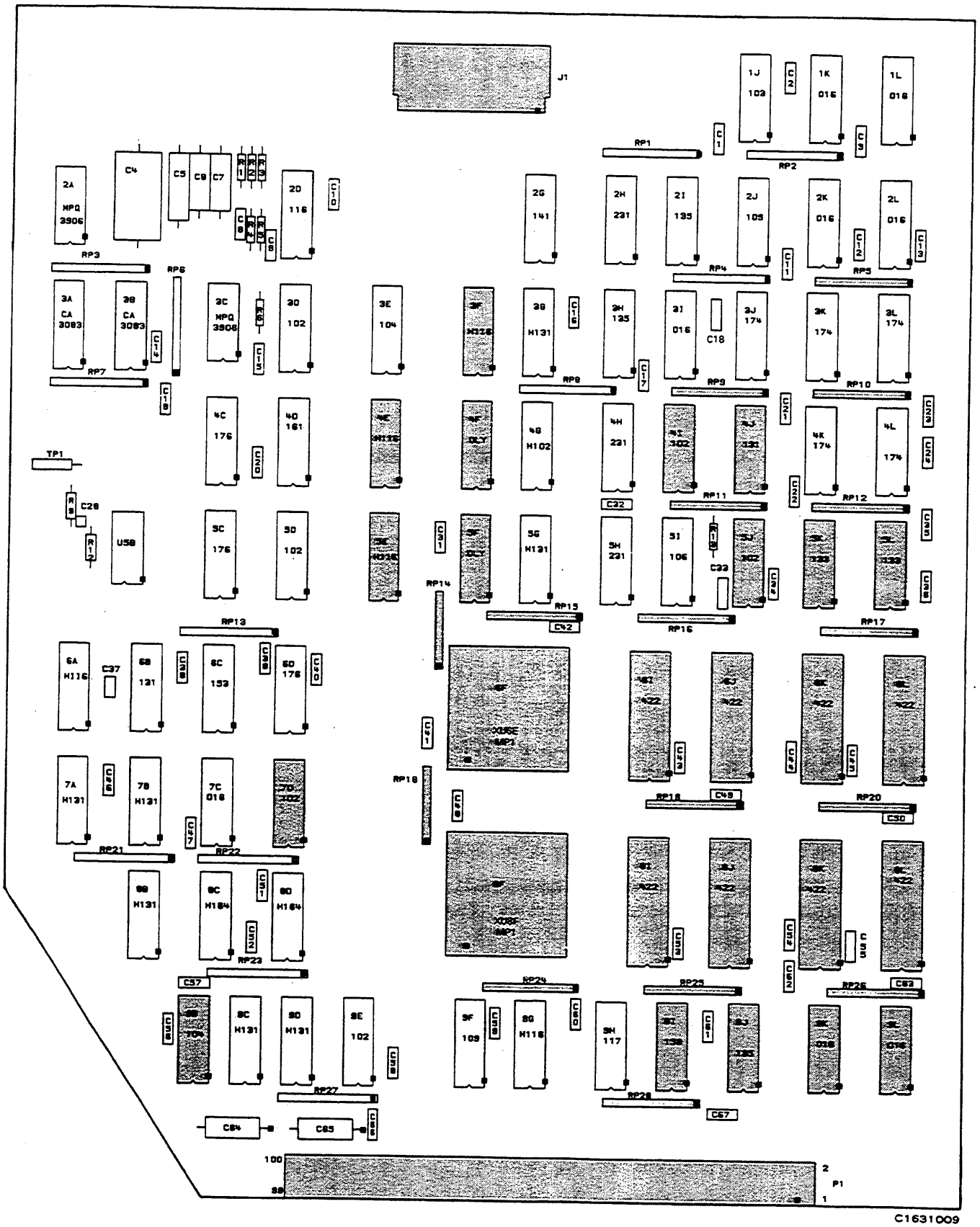
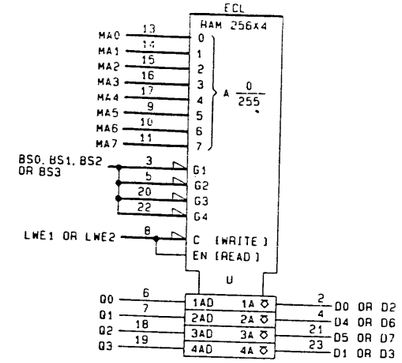


Figure 8D-10. Timing Pod

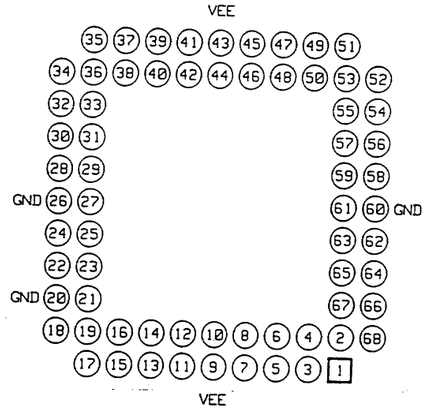


Component Locator for Schematic 8D-1

NOTE 1. RAM PINOUT



NOTE 2. MACROCELL PIN LOCATOR

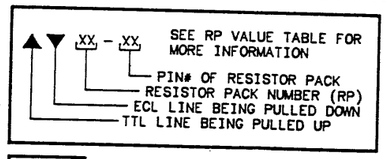


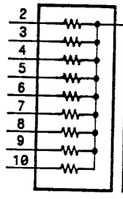
Macrocell Pin-out Diagram
(Circuit Side View)

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U3F,4E,4I,4J, 5E,5J-L,7D,9B, 9J-L
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 24 12	U6I-6L,8I-8L
Vcc(gnd) Vee(-5.2)	16 8	U9I
-5.2 GND	9,43 20,26,60	U6F,8F

RESISTOR PACK DESCRIPTIONS

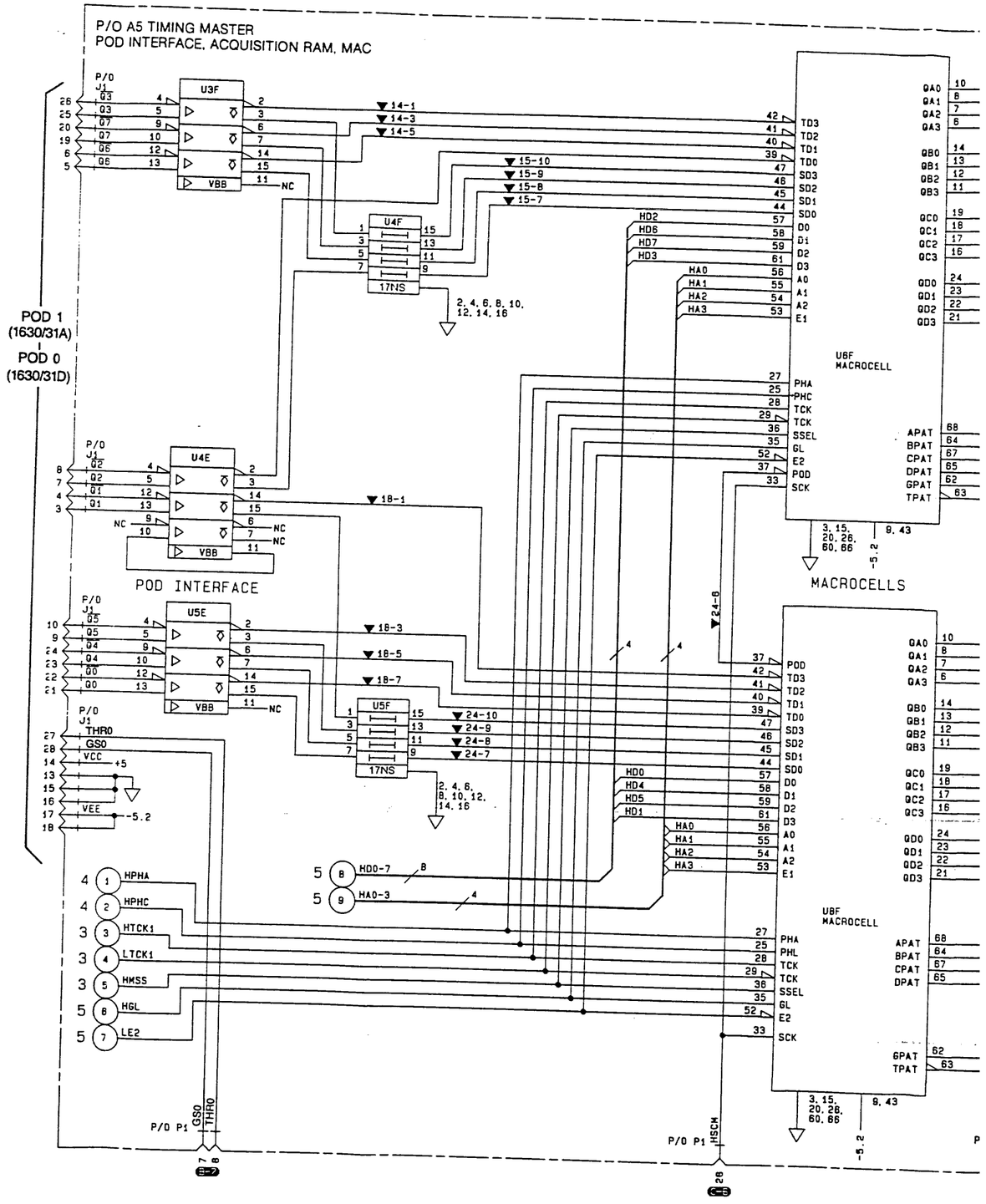




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2,4, 5,7-13 15-17, 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

J1 P1 RP5,9-12,14-20, 24-26,28 U3F,4E,F,4I,4J,5E, 5J-L,6F,6I-L,7D, 8F,8I-L,9B,I-L	



IC DEVICE
WER CONNECTIONS

PLY	PIN NO.	IC GROUP
d) d) 2)	1 16 8	U3F,4E,4I,4J, 5E,5J-L,7D,9B, 9J-L
d) d) 2)	1 24 12	U6I-6L,8I-8L
) 2)	16 8	U9I
	9,43 20,26,60	U6F,8F

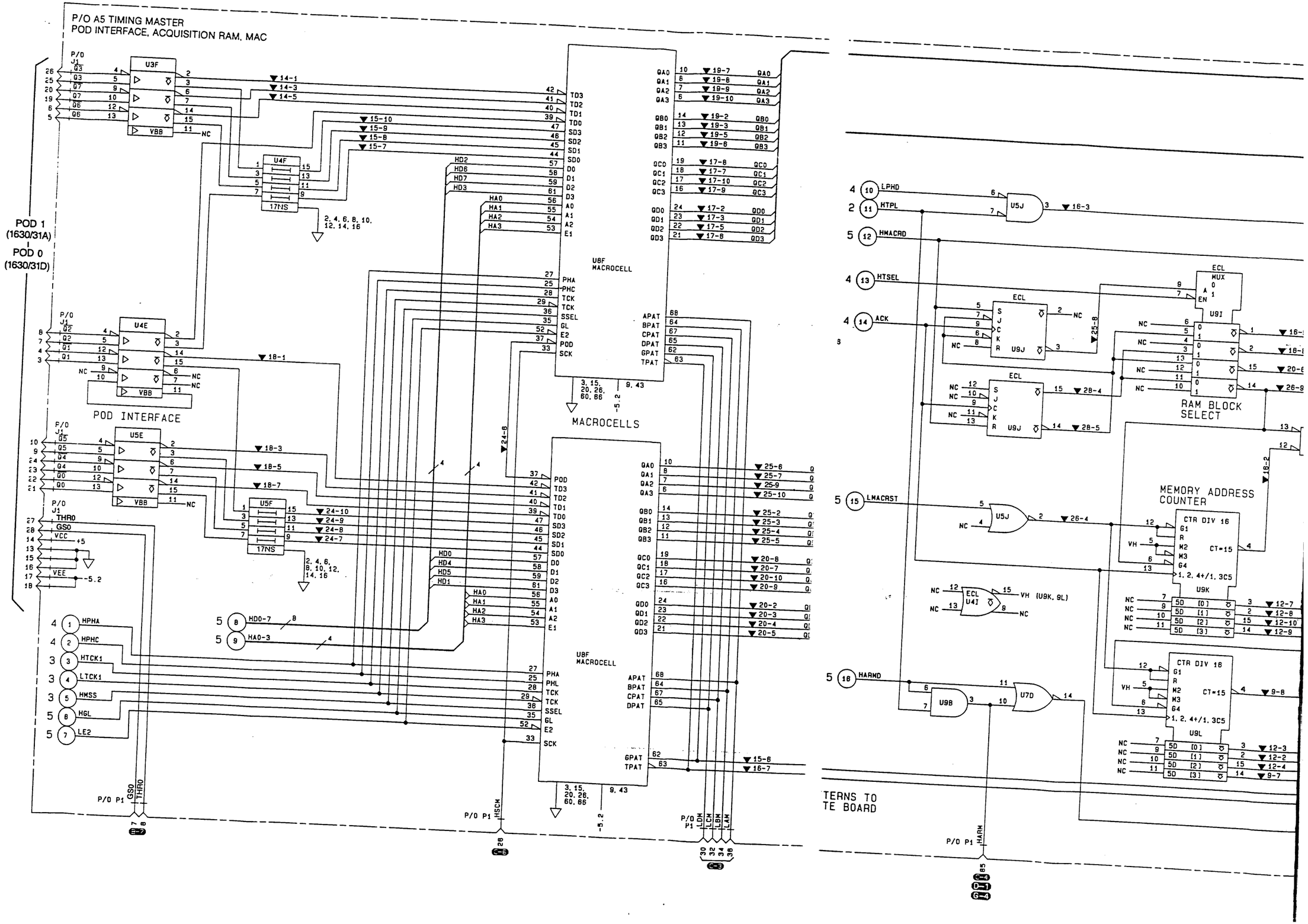
R PACK DESCRIPTIONS

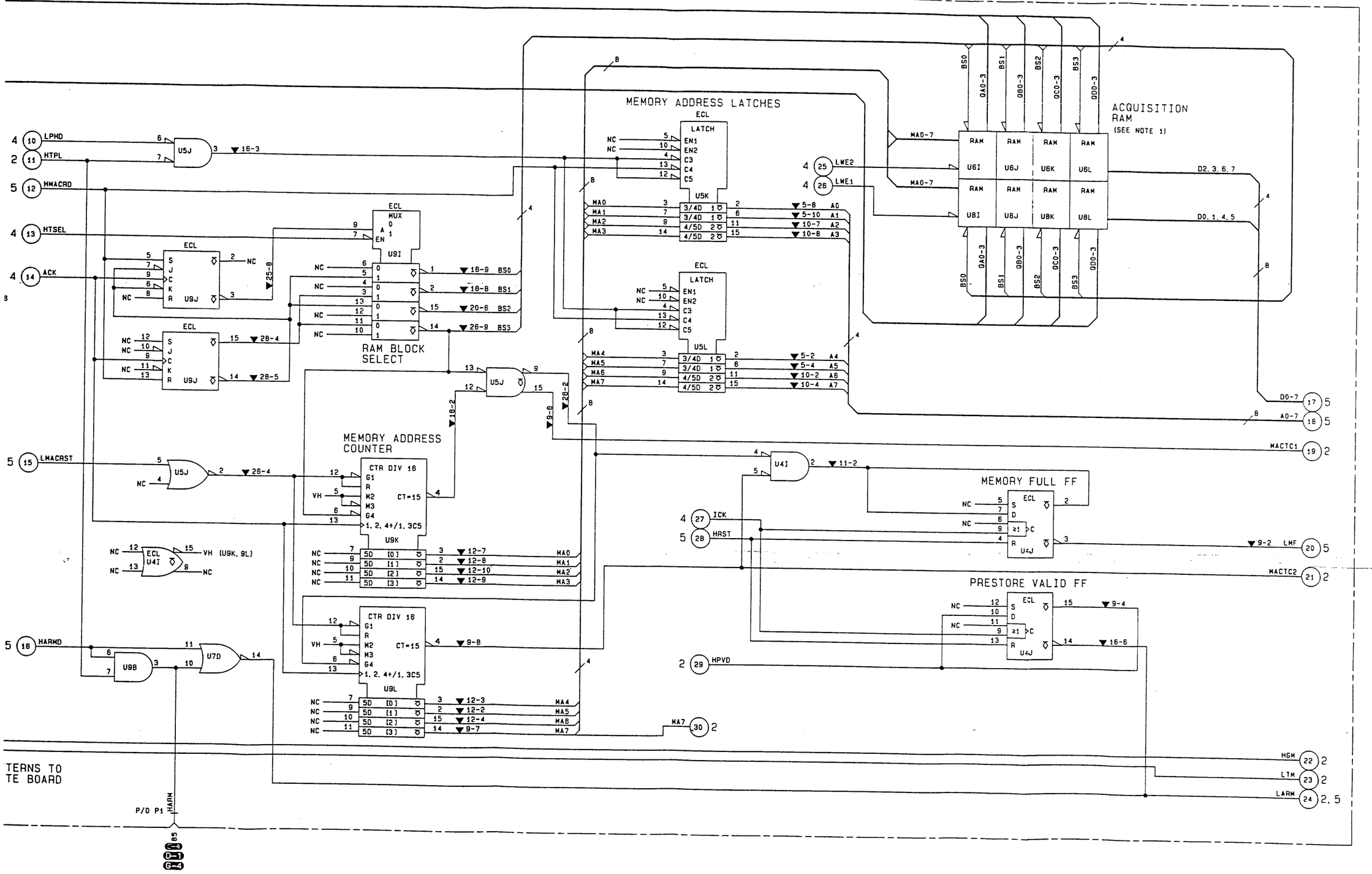
- XX SEE RP VALUE TABLE FOR MORE INFORMATION
  - PIN# OF RESISTOR PACK
  - RESISTOR PACK NUMBER (RP)
  - ECL LINE BEING PULLED DOWN
  - TTL LINE BEING PULLED UP

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
,2,4, ,7-13 5-17, 9-23 4,18	100 X 9	1	-2.4
	100 X 4	2,4,6,8	-2.4

N THIS SCHEMATIC

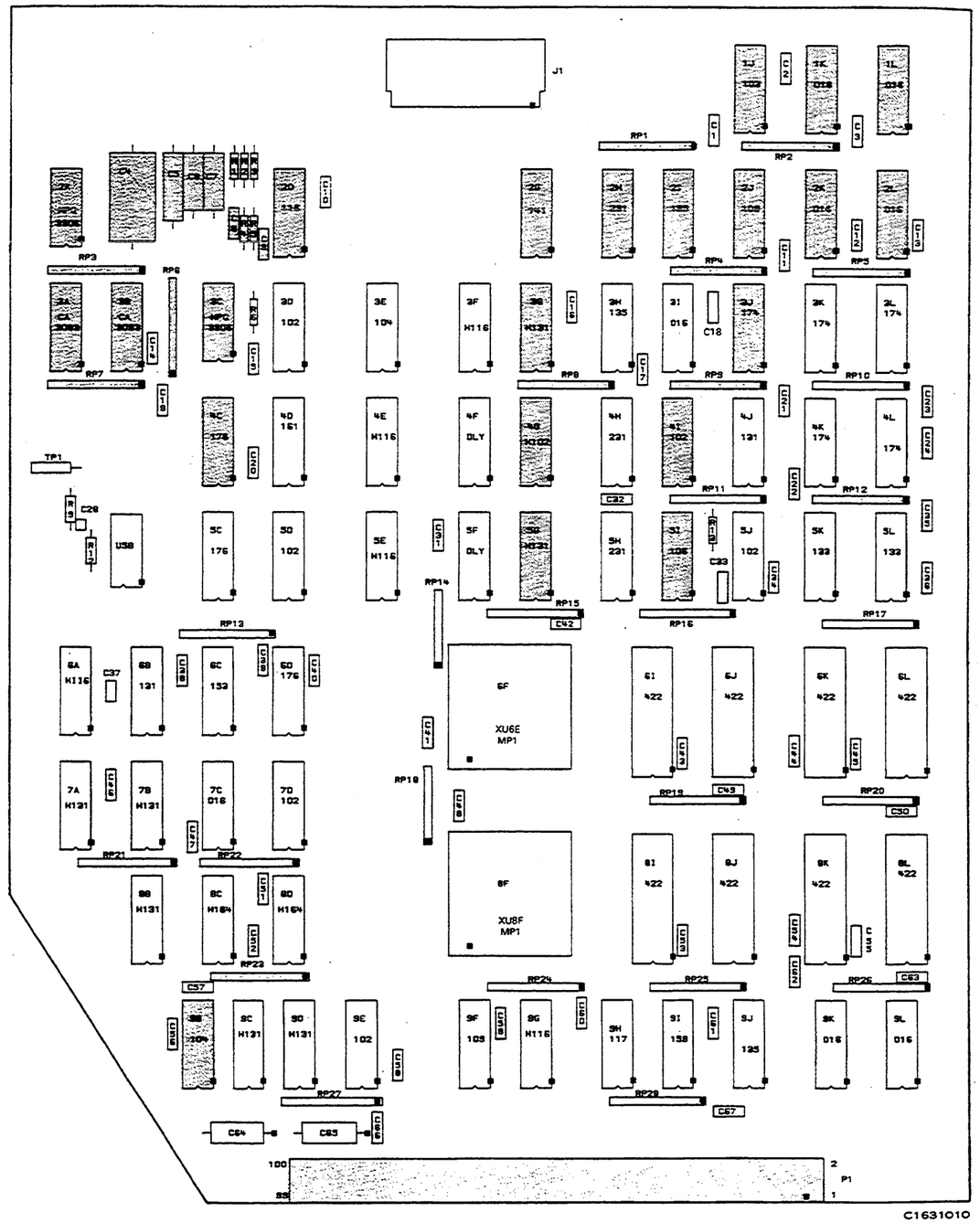
-20, ,4J,5E, ,7D, I-L	





8D-1

Schematic 8D-1
Pod Interface, Acquisition RAM, MAC

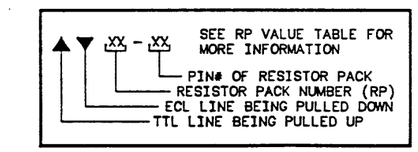


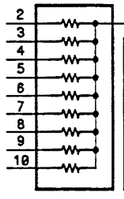
Component Locator for Schematic 8D-2

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1J-L,2G-L, 3G,3J,4C,4G, 4I,5G,5I,9B

RESISTOR PACK DESCRIPTIONS:



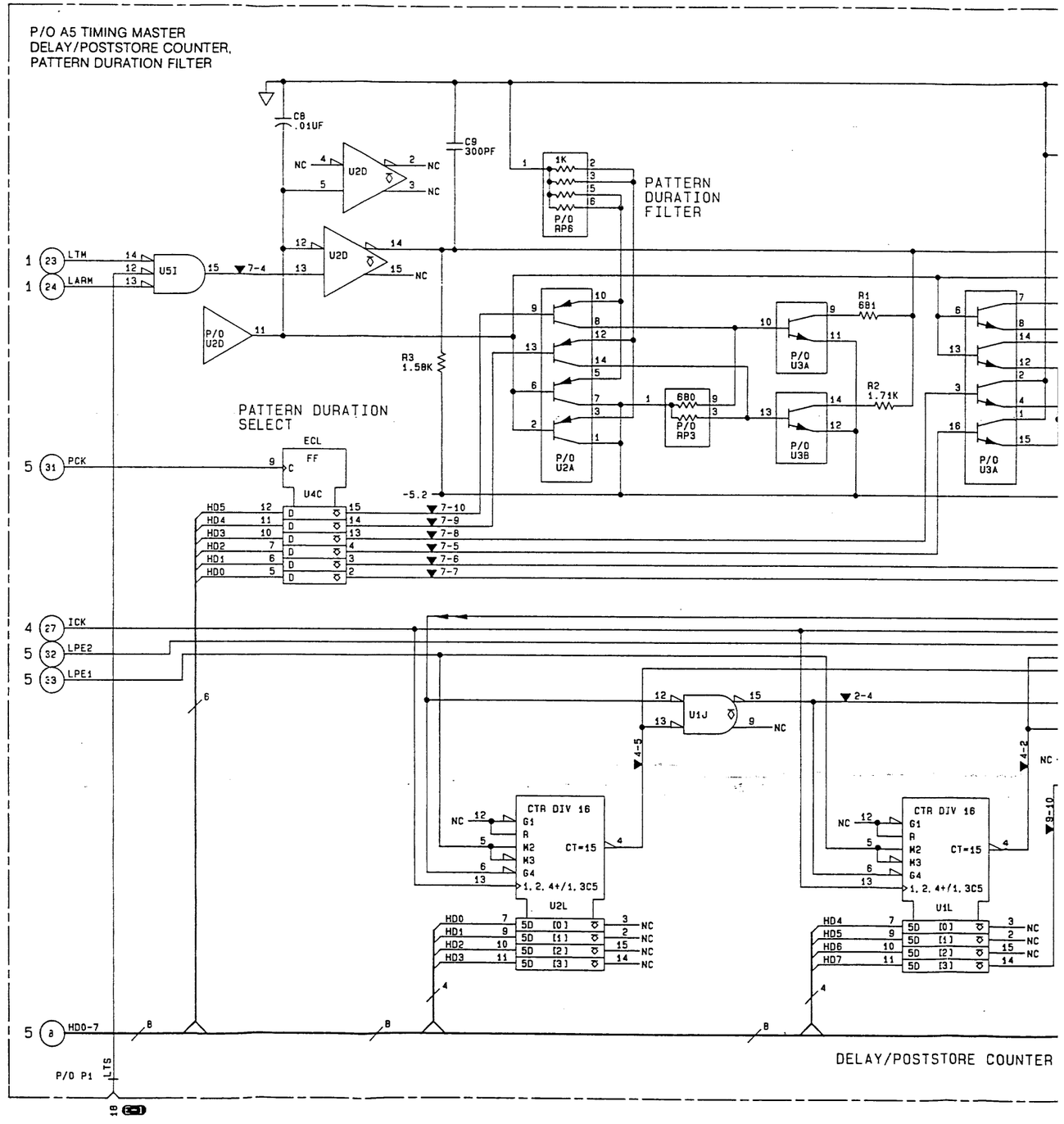


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

C4-9 P/O P1 R1-5 RP1-9,12,23 U1J-L,2A,2D,2C-L, U3A-C,3G,3J,4C, 4G,4I,5G,5I,9B	

P/O A5 TIMING MASTER
DELAY/POSTSTORE COUNTER,
PATTERN DURATION FILTER



E
TIONS

IC GROUP
U1J-L,2G-L, 3G,3J,4C,4G, 4I,5G,5I,9B

CRIPTIONS:

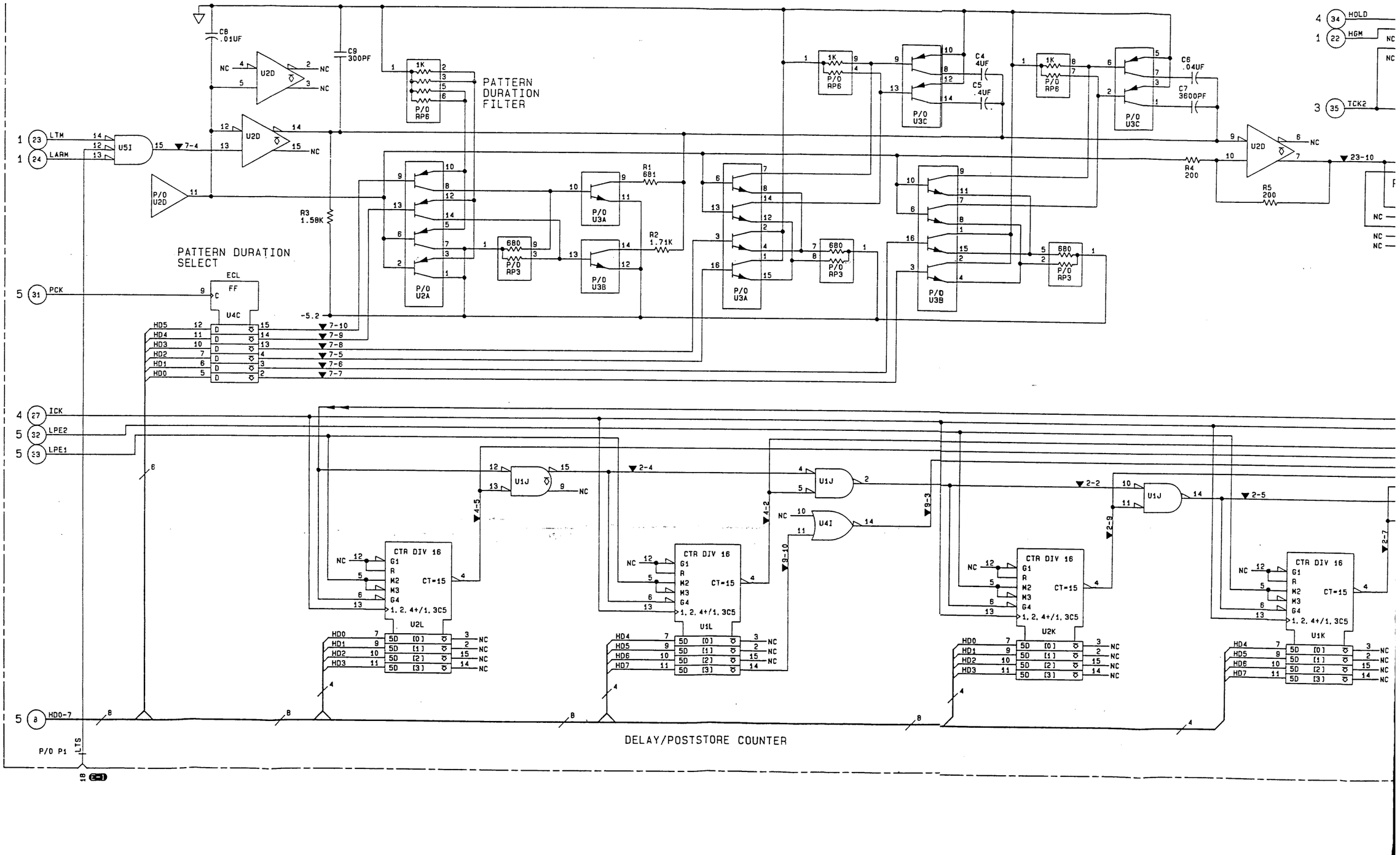
LUE TABLE FOR RMATION

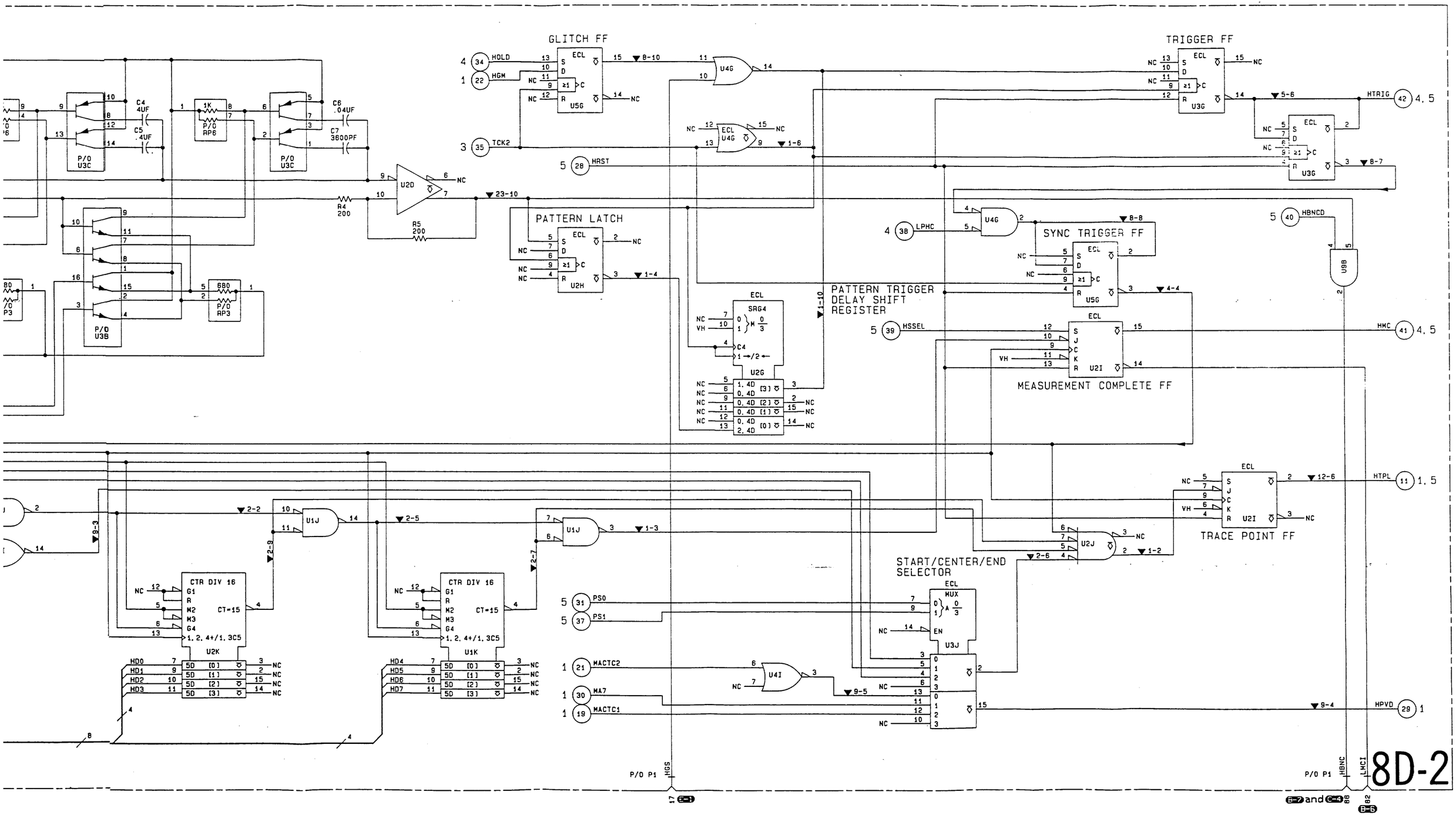
SISTOR PACK CK NUMBER (RP) IG PULLED DOWN PULLED UP

POWER PIN	VOLTAGE
1	-2.4
2,4,6,8	-2.4

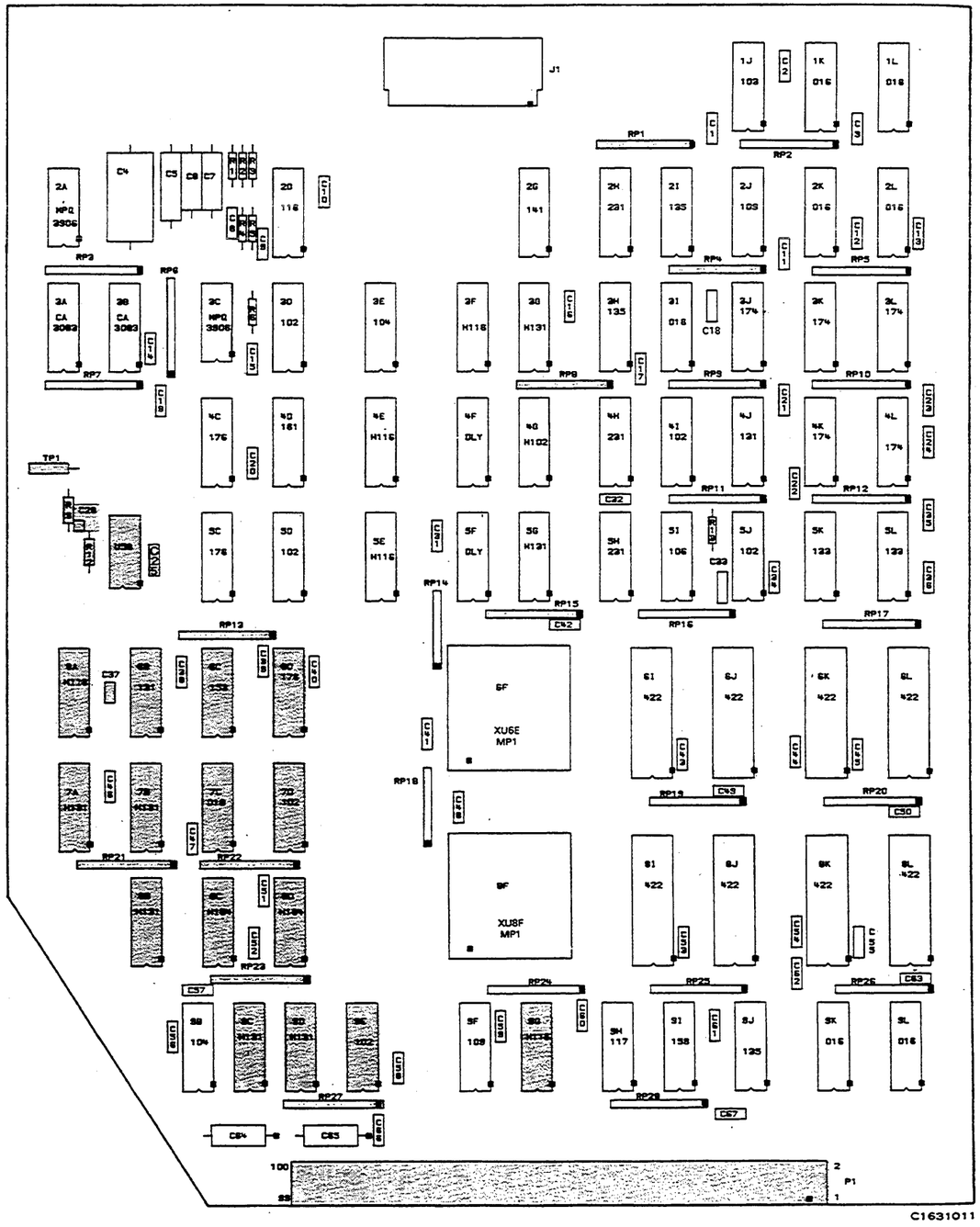
SCHEMATIC

P/O A5 TIMING MASTER
DELAY/POSTSTORE COUNTER,
PATTERN DURATION FILTER





Schematic 8D-2
Delay/Poststore Counter, Pattern Duration Filter
8D-23

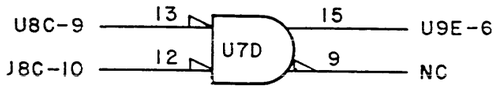


Component Locator for Schematic 8D-3

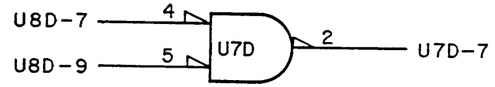
NOTES 1 & 2

ON TIMING MASTER BOARD 01630-66506, GATES U7D-A AND U7D-D ARE SWAPPED. FOLLOWING ARE THE IC CONNECTIONS.

NOTE 1

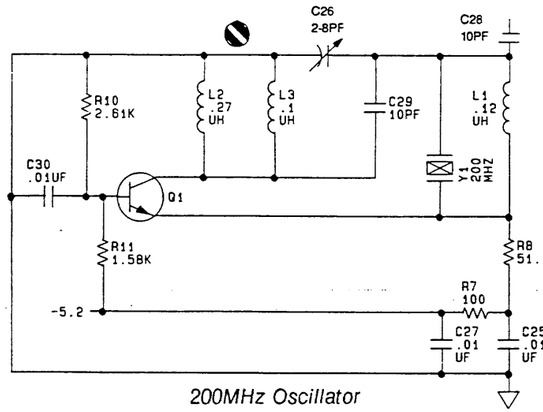


NOTE 2

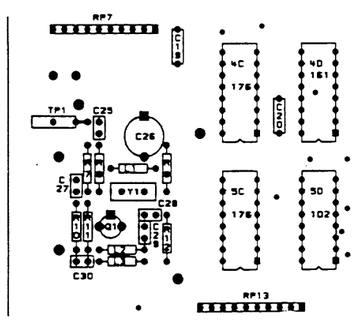


NOTE 3

OSCILLATOR CIRCUIT AND COMPONENT LOCATOR FOR TIMING MASTER BOARDS 01630-66506 AND 66510 WITH DISCRETE COMPONENT OSCILLATOR. C26 IS 5.5-18PF ON OLDER BOARDS. SEE SERVICE NOTE 1630A/D-2.



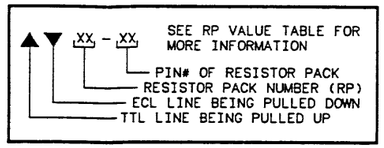
200MHz Oscillator

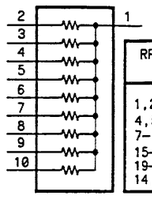


IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U6A-6D,7A-7D, 8B-8D,9C-9E,9G

RESISTOR PACK DESCRIPTIONS

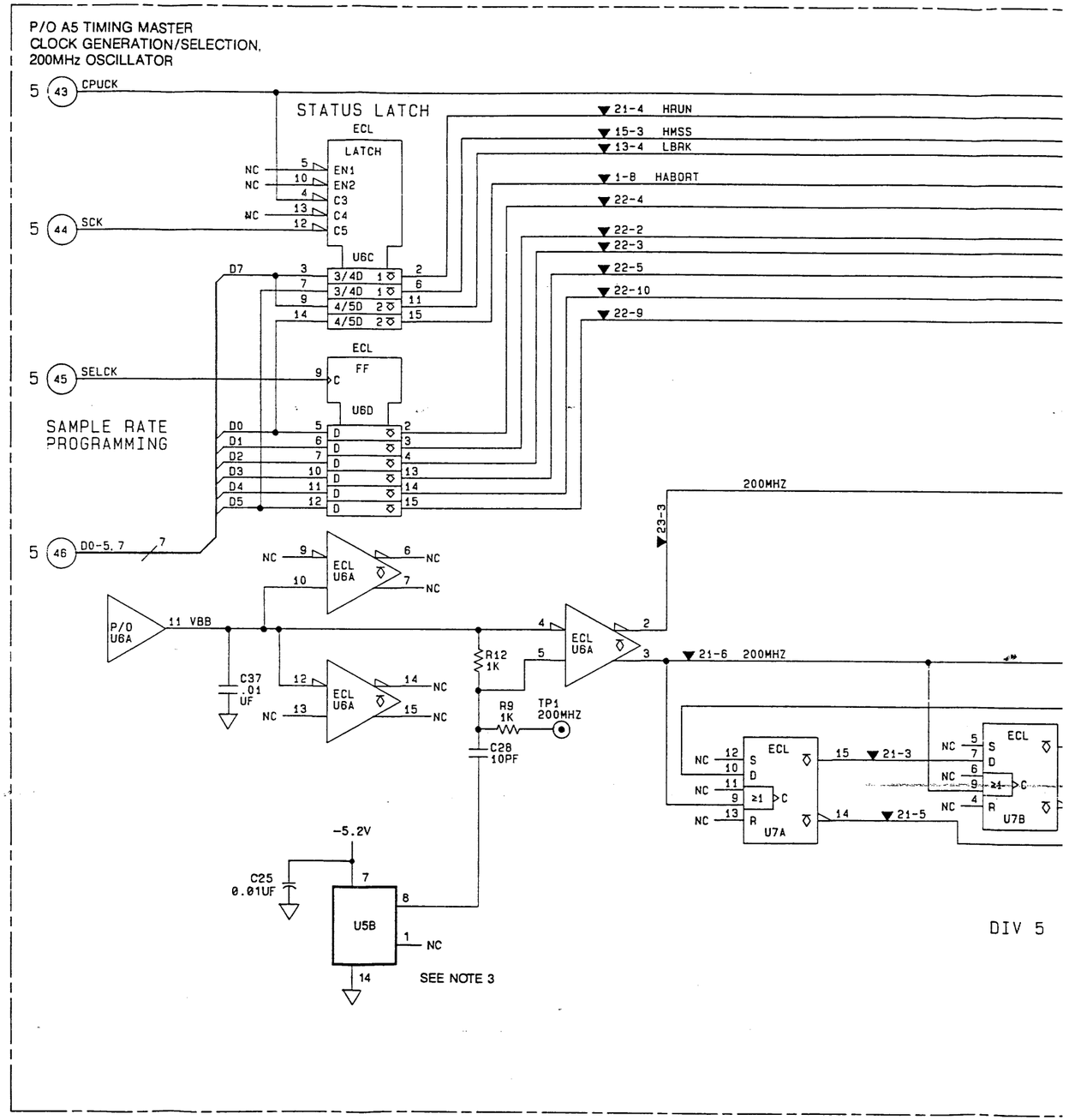




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23 14,18	100 X 9	1	-2.4
	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

C28,37 P1 R9,12 RP1,4,8,13,15, 21-23,27 TP1	U5B,6A-6D,7A-7D, U8B-8D,9C-9E,9G



IC DEVICE
ER CONNECTIONS

	PIN NO.	IC GROUP
	1 16 8	U6A–6D,7A–7D, 8B–8D,9C–9E,9G

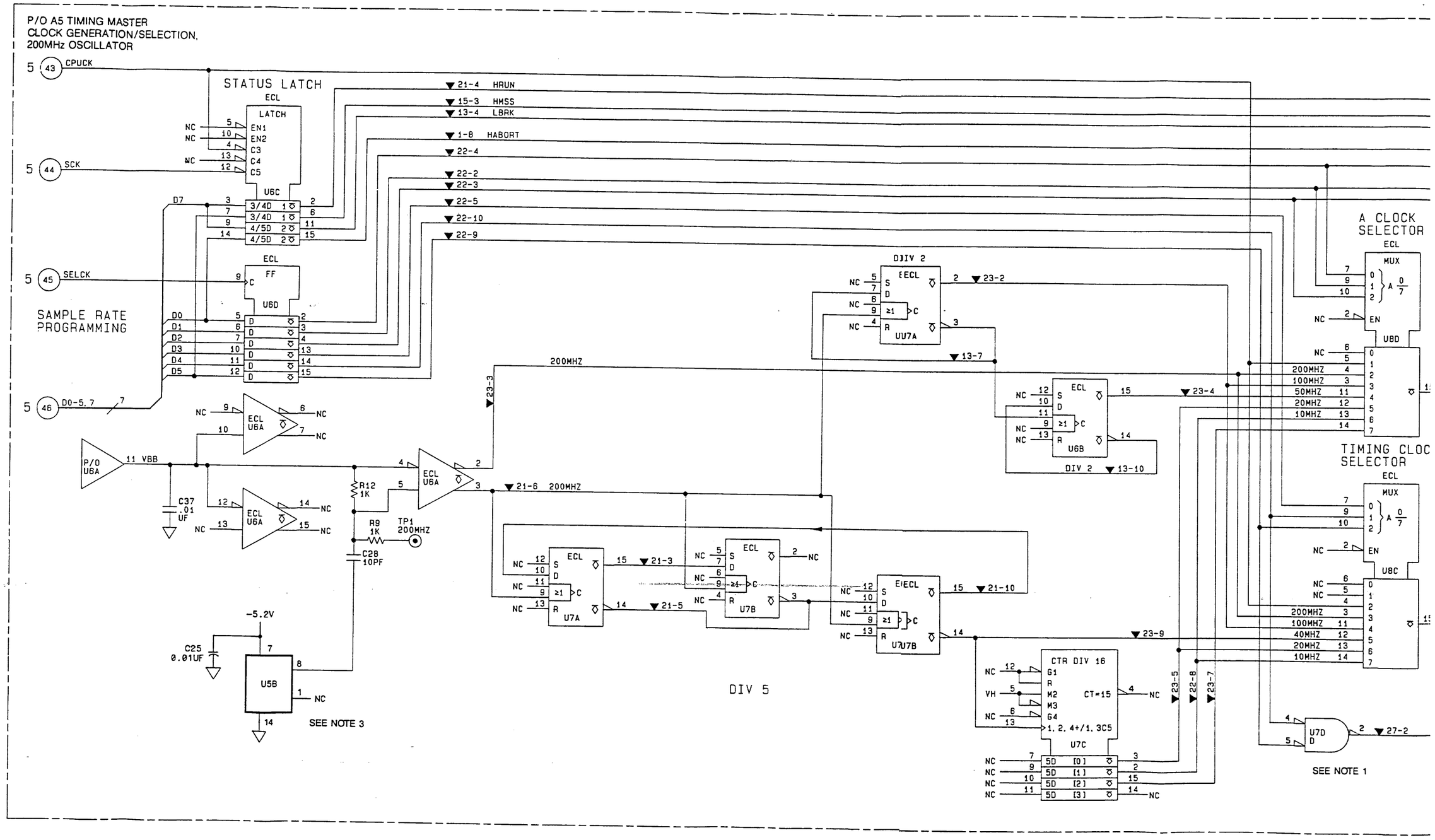
PACK DESCRIPTIONS

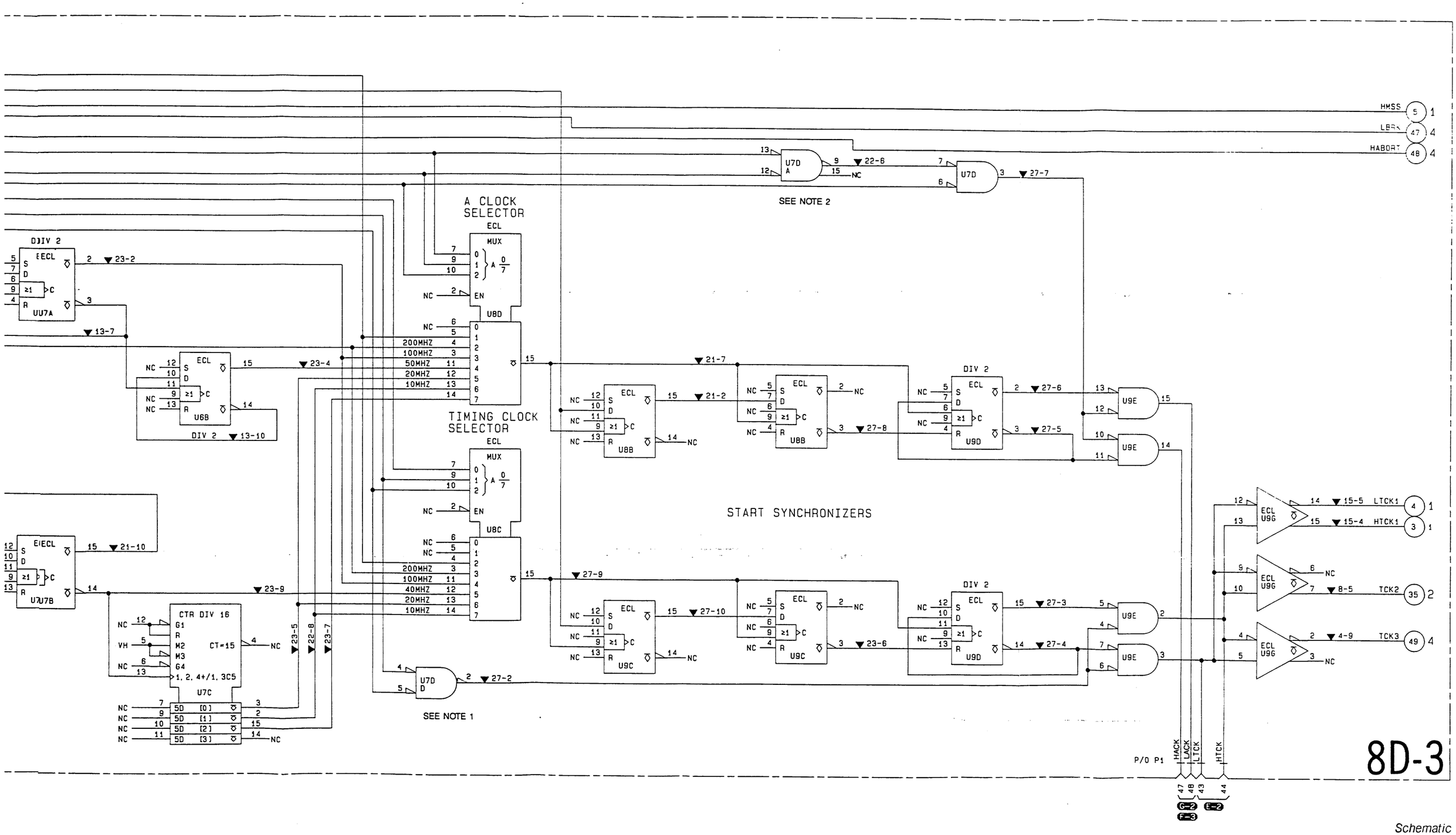
XX SEE RP VALUE TABLE FOR MORE INFORMATION
PIN# OF RESISTOR PACK
RESISTOR PACK NUMBER (RP)
ECL LINE BEING PULLED DOWN
TTL LINE BEING PULLED UP

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
,2, ,5, –13, 5–17 9–23 4,18	100 X 9	1	–2.4
	100 X 4	2,4,6,8	–2.4

N THIS SCHEMATIC

,15,	U5B,6A–6D,7A–7D, U8B–8D,9C–9E,9G





Schematic 8D-3
Clock Generation/Selection, 200MHz Oscillator

Component Locator for Schematic 8D-4

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2H,3E,3H,3I, 4H,5H,5I,5J, 9H

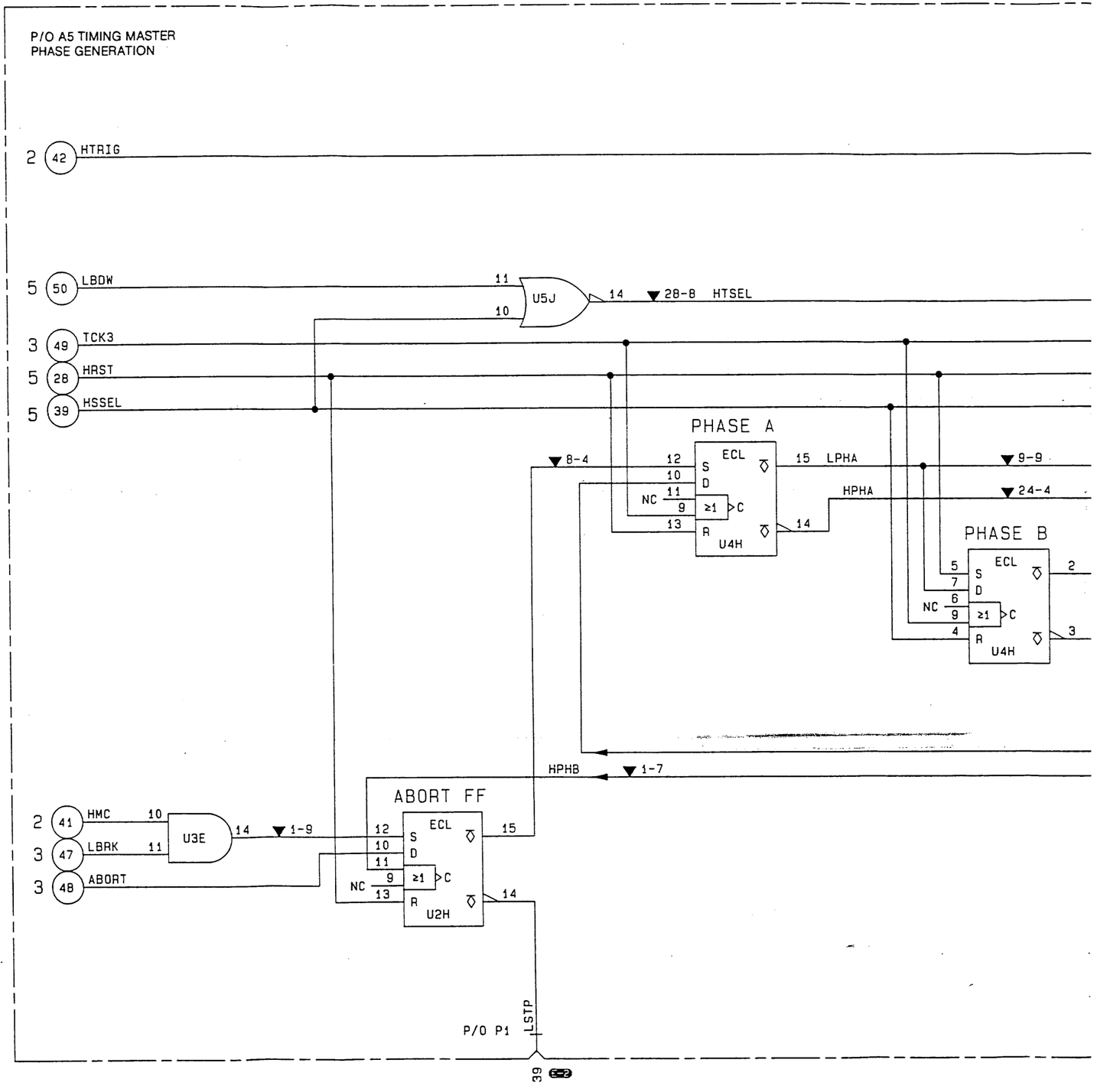
RESISTOR PACK DESCRIPTIONS:

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7–13, 15–17 19–23 14,18	100 X 9 100 X 4	1 2,4,6,8	–2.4 –2.4

PARTS ON THIS SCHEMATIC

P1 RP1,2,4,7–11,16, 17,24,26,28 U2H,3E,3H,3I,4H, U5H–J,9H	

P/O A5 TIMING MASTER
PHASE GENERATION



P/O A5 TIMING MASTER
PHASE GENERATION

HOLD/ENCODER STATE COUNTER

CTR DIV 16
G1
R
M2
M3
G4
1, 2, 4+/1, 3C5
CT=15
U3I

2 (42) HTRIG
5 (50) LBDW
3 (49) TCK3
5 (28) HRST
5 (39) HSSEL

U5J
11
10
14 ▼28-8 HTSEL

PHASE A
PHASE B
PHASE C
PHASE D
PHASE GENERATION

ECL
S
D
R
C
≥1
U4H
U5H
U2H

▼8-4
▼9-9
▼24-4
▼8-6
▼24-3
▼11-8
▼11-3
▼28-7
▼1-7
▼1-9

LPHA
HPHA
LPHB
HPHB
LPHC
HPHC
LPHD
HPHD

HTSEL
TCK3
HRST
HSSEL

ABORT FF
2 (41) HMC
3 (47) LBRK
3 (48) ABORT
U3E

P/O P1 LSTP 39 (C-2)
HSWM 22 (C-7)

HOLD/ENCODER STATE COUNTER

CTR DIV 16
G1
R
M2 CT=15
M3
G4
1, 2, 4+/1, 3C5
U3I

VH
NC
NC
NC
NC
5D [0]
5D [1]
5D [2]
5D [3]
▼ 8-2
▼ 4-8
▼ 10-9
NC
NC

ECL
S
J
C
K
R U3H
VH
NC
▼ 11-9
HOLD FF

HTSEL
TCK3
HRST
HSSEL

HOLD 34 2
ENC0 54 5
ENC1 55 5
HTSEL 13 1

LPHA 53 5
HPHA 1 1

PHASE C
ECL
S
D
≥1 C
R U5H
NC
NC
▼ 11-8
LPHC
HPHC
PHASE GENERATION

▼ 8-6
▼ 24-3
ECL
S
D
≥1 C
R U5H
NC
HSSEL
▼ 11-3
▼ 28-7
LPHD
HPHD

LPHC 38 2
HPHC 2 1
LPHD 10 1

PHASE D

WRITE ENABLE SELECT
U9H
NC
NC
▼ 26-3
NC

LWE1 26 1
LWE2 25 1

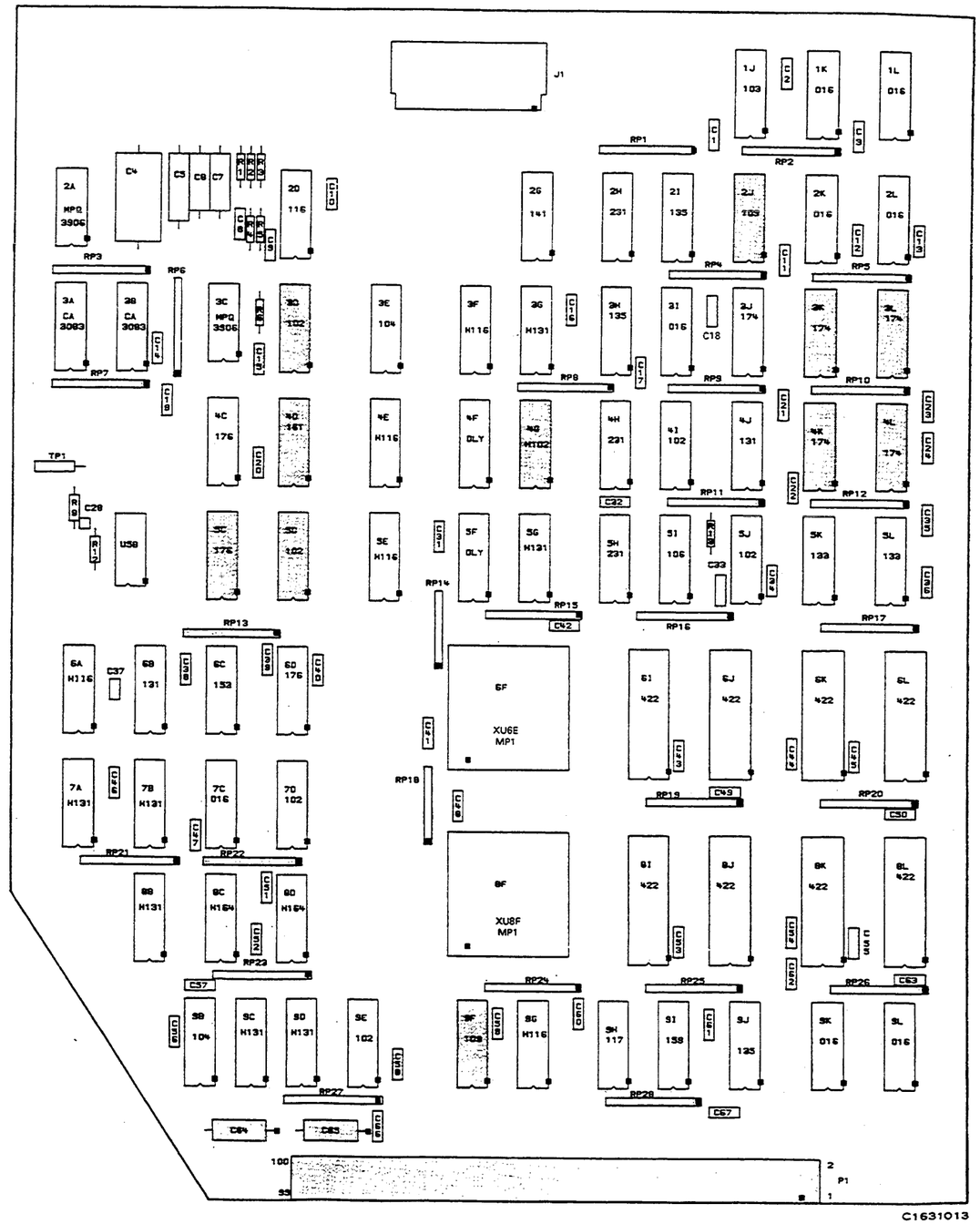
OR PHD STATE
U9H
NC
NC
▼ 28-6
▼ 17-4
▼ 7-3
U3E
▼ 16-5
U5I
▼ 26-6 ACK
14 1

5 51 READ-CK
5 52 LOAD-CK
LPHB
U5I
▼ 2-8 ICK
27 1, 2

HSWM
22 C-7

8D-4

Schematic 8D-4
Phase Generation

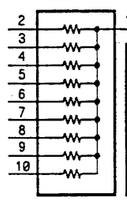


Component Locator for Schematic 8D-5

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U2J,3D,3K,3L, 4D,4G,4K,4L, 5C,5D,9F

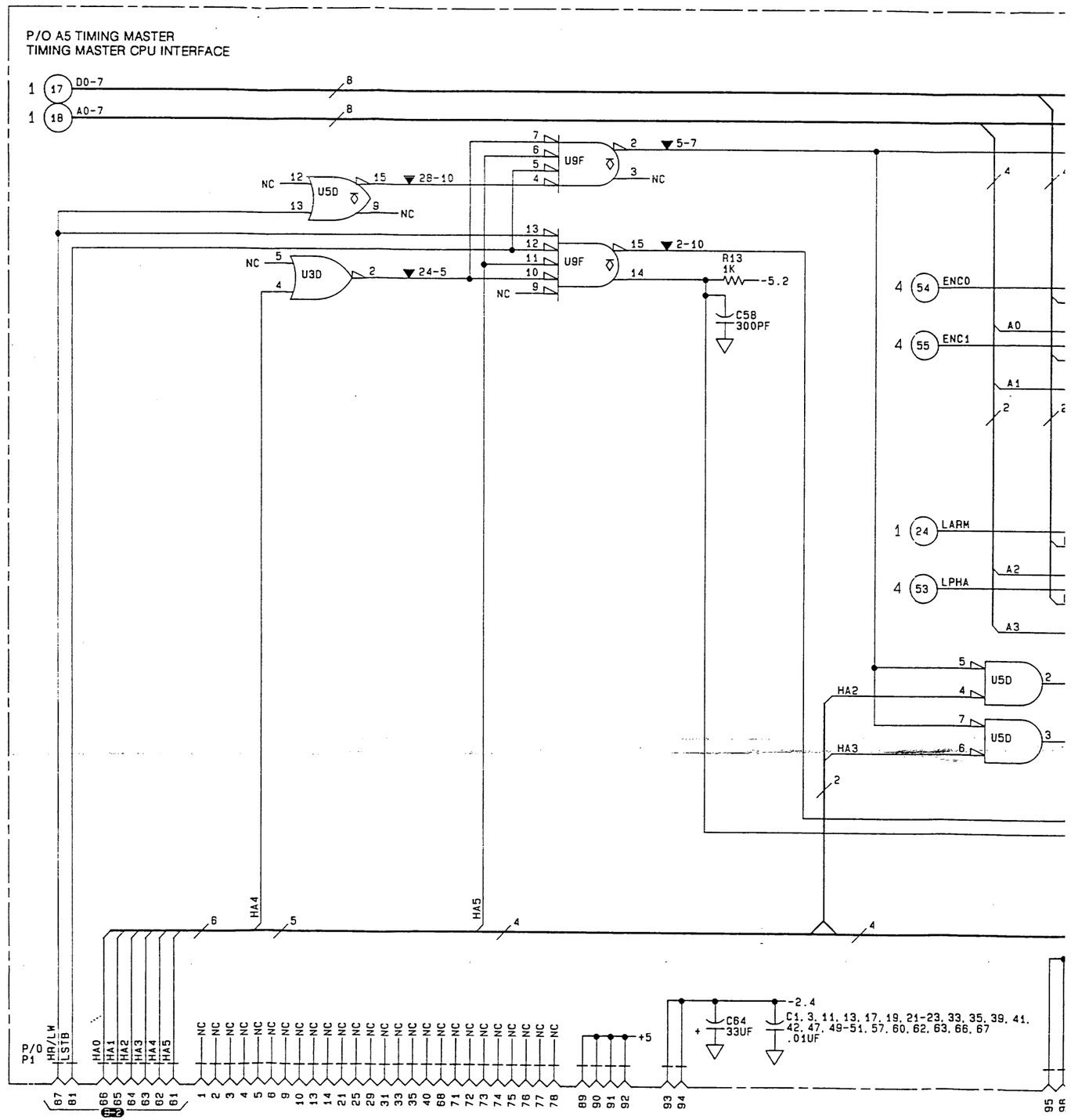
RESISTOR PACK DESCRIPTIONS:

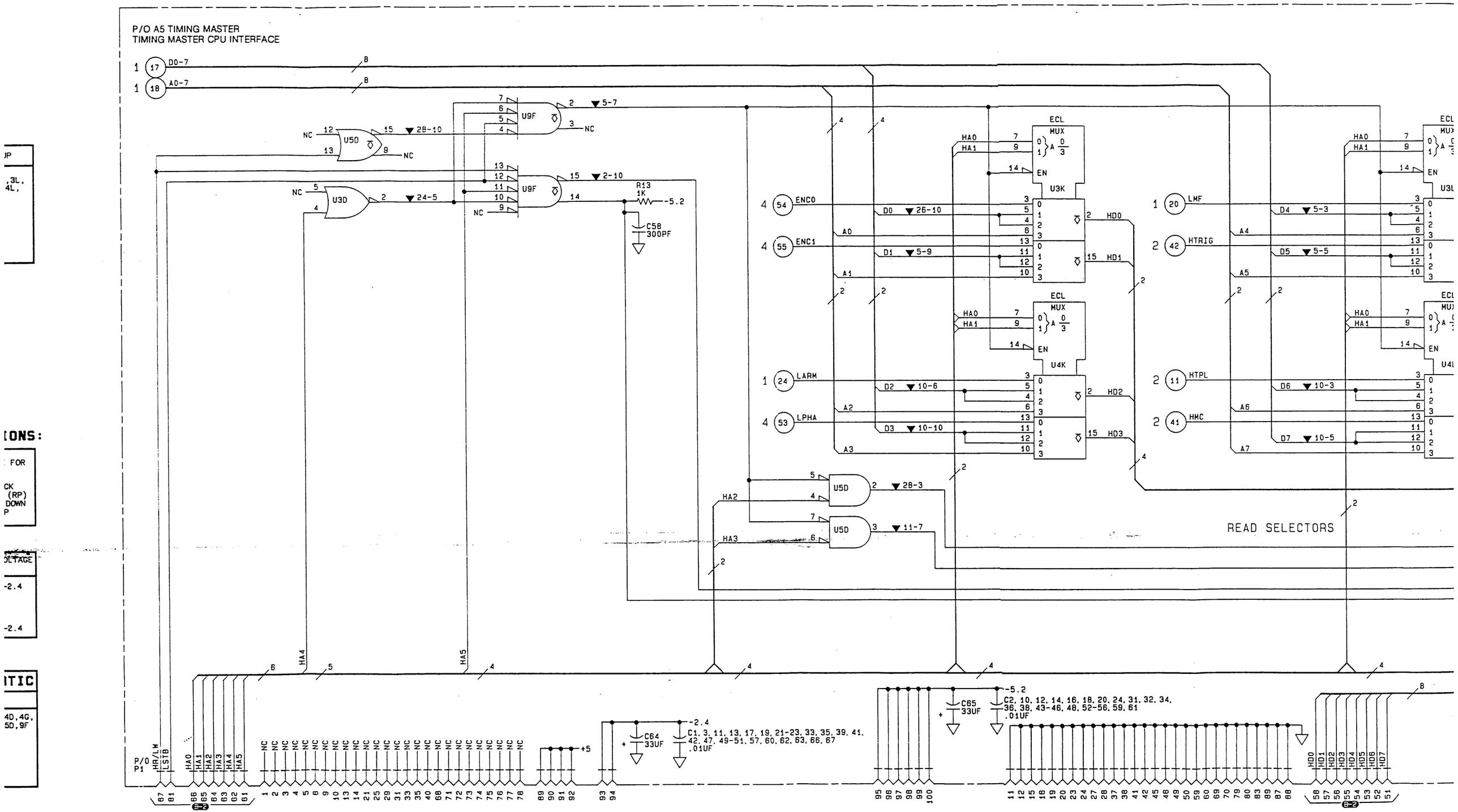


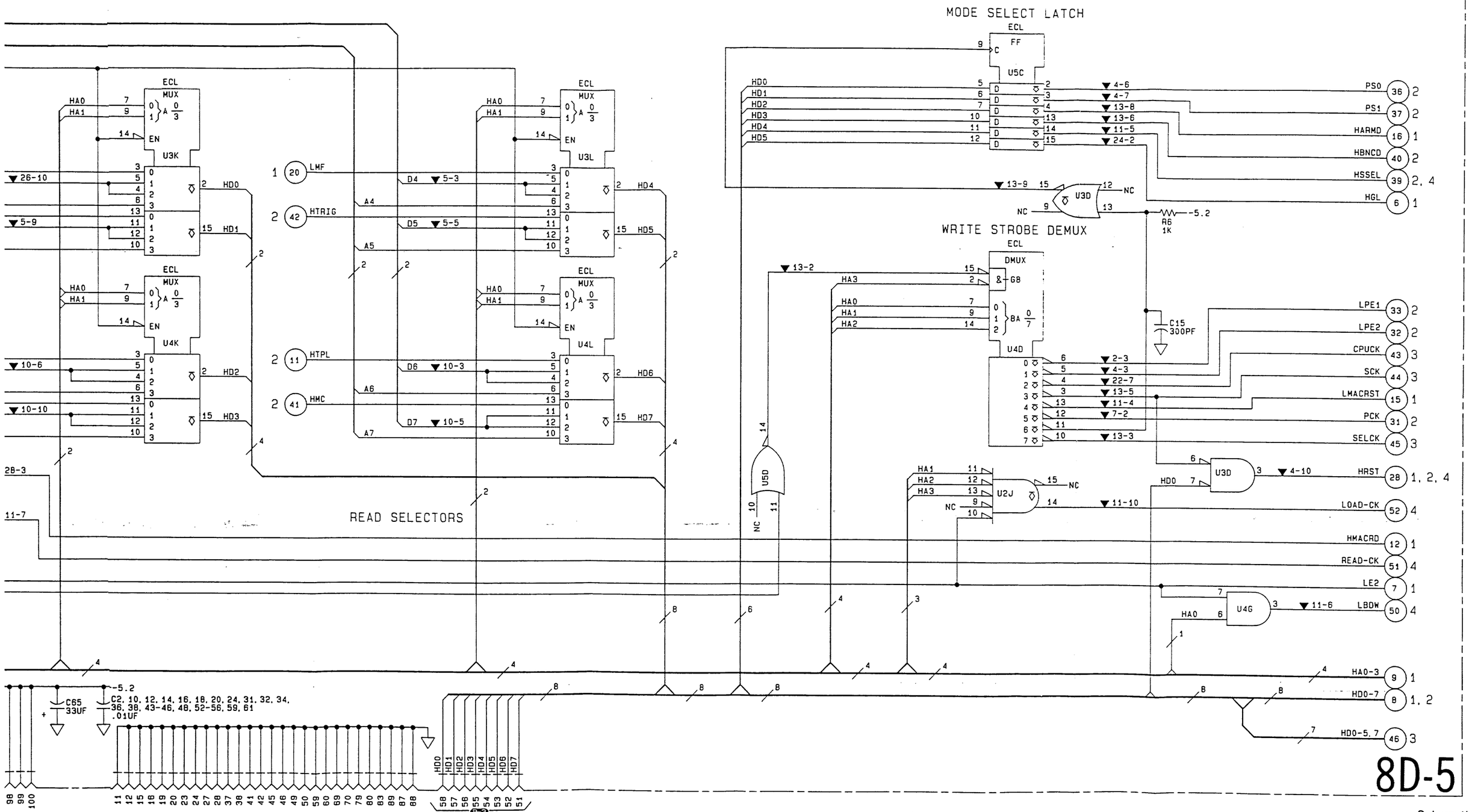
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1,2, 4,5, 7-13, 15-17 19-23	100 X 9	1	-2.4
14,18	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

C1-3,8,10-24,31-36, 38-67 P/O P1 R6,13 RP2,4,5,7,10,11, 13,22,24,26,28	U2J,3D,3K,3L,4D,4G, U4I,4K,4L,5C,5D,9F




P/O A5 TIMING MASTER
TIMING MASTER CPU INTERFACE
D0-7
A0-7
U5D
U3D
U9F
R13
1K
-5.2
C58
300PF
ENC0
ENC1
LARM
LPHA
LMF
HTRIG
HTPL
HMC
ECL
MUX
U3K
U4K
HA0
HA1
HA2
HA3
HD0
HD1
HD2
HD3
READ SELECTORS
C64
33UF
C1, 3, 11, 13, 17, 19, 21-23, 33, 35, 39, 41, 42, 47, 49-51, 57, 60, 62, 63, 66, 67
.01UF
C65
33UF
C2, 10, 12, 14, 16, 18, 20, 24, 31, 32, 34, 36, 38, 43-46, 48, 52-56, 59, 61
.01UF
P/O
P1
HR/LW
LSTB
HA0
HA1
HA2
HA3
HA4
HA5
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7



Schematic 8D-5
Timing Master CPU Interface
8D-29/(8D-30 blank)

Service Group 8E Table of Contents

Paragraph		Page
8E-1.	Introduction	8E-1
8E-2.	General	8E-1
8E-3.	State Mode	8E-1
8E-4.	Memory Address Counter	8E-1
8E-5.	Glitch Mode	8E-2
8E-6.	Clock Phasing	8E-2
8E-7.	Macrocell Removal	8E-2
8E-8.	Macrocell Installation	8E-3
8E-9.	Mnemonics	

List of Illustrations

Figure		Page
8E-1.	Timing Pod	8E-5

List of Tables

Table		Page
8E-1.	Timing Master and Slave Board Comparisons	8E-1
8E-2.	Mnemonics	8E-3

List of Schematics

Schematic		Page
8E-1.	Pod Interface, Macrocells, RAM	8E-7
8E-2.	Mode and Phasing	8E-9

NOTES

SERVICE GROUP 8E
TIMING SLAVE

8E-1. INTRODUCTION

8E-2. GENERAL. The optional Timing Slave board is similar to the Timing Master board in that it contains two macrocells, 1K x 8 RAM, a memory address counter, and clock phasing circuitry. Unlike the master board it does not contain a clock generator, and must receive its clock from either the Timing Master or State Master.

The valid timing or glitch pattern signals from the slave macrocells go to the Timing Master, where they are ANDed with timing and glitch pattern signals from the master macrocells. In the State Mode, the pattern signals from the timing boards are ANDed on the state board with the state pattern signals.

Table 8E-1. Timing Master and Slave Board Comparisons

TIMING MASTER BOARD	TIMING SLAVE BOARD
Pod Interface (8-bit)	Pod Interface (8-bit)
Macrocells (2)	Macrocells (2)
Acquisition RAM (1K x 8)	Acquisition RAM (1K x 8)
Pattern Duration Filter	
Delay/Poststore Counter	
Clock Generation	
Clock Selection	
Clock Phasing	Clock Phasing

8E-3. STATE MODE. With the optional slave board and its pod, timing width is increased to 16 channels. The timing slave board may also be used with the master timing board in the State Mode as an extension to the state analyzer, effectively increasing the width of state analysis to 43 bits.

When the 35-bit State/8-bit Timing combination is chosen in the format specification, only the timing slave board can be used with the state board for 35-bit state analysis. This is because only the timing master board has the pattern duration and clock circuitry needed for timing analysis.

In the State Mode the macrocells perform the same function as pattern recognition circuitry on the state board: both the master and slave board send a pattern bit for each of the four possible patterns that can be specified in state analysis. The two bits from master and slave for each pattern are ANDed on the state board.

8E-4. MEMORY ADDRESS COUNTER. The slave board's memory address counter is the same as that on the timing master board: An 8-bit counter selects one of 256 8-bit locations in a block of RAM; and a Block Selector chooses one of four 256-blocks.

8E-5. GLITCH MODE. As with master timing, glitches may be specified for detection or triggering on four of the eight timing slave board channels.

8E-6. CLOCK PHASING. A ring counter driven by the master timing board clock generates the four phases needed to synchronize the different functions on the board. For example, write-enable pulses for the memory are synchronized to phase "D" of the generator when the timing analyzer is in the timing mode. When the timing analyzer is being run as an adjunct of the state analyzer, the write-enable pulses are synchronized to a state control signal. The memory address clock is derived from Phase B. Phases A and C are sent to the macrocells.

8-7. MACROCELL REMOVAL

a. Gently pry the socket retaining clip away from the heatsink.

b. Carefully pull the heatsink sideways away from the socket. The macrocell chip may come away with the heatsink.

c. Remove the macrocell chip if it is still in the socket.

8-8. MACROCELL INSTALLATION

a. Place the macrocell chip (circuit side down) in the socket. The socket is keyed so that the macrocell chip will fit only one way.

b. Put a thin coating of thermal compound on the back of the macrocell chip.

c. Place the two small guide pins on the heatsink into the socket. The heatsink is keyed so it fits only one way.

d. Gently push down on the heatsink and flip the socket retaining clip up and over the large heatsink guide pins.

8E-9. MNEMONICS.

The following signals, listed in alphabetical order, are used on the State Board. Active high signals have "H" as the first letter; active low signals have "L". All signals on the Timing and State boards are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8E-2. Mnemonics

Mnemonic	Description
ACK	Address Clock. Increments memory address counter.
BS0-3	Block Select. Selects a block of RAM for reads or writes.
GS1	Ground Sense. Reference ground from user system.
HA0-5	Motherboard address bus.
HBRS	Break Reset. Sets BS0 high and other Block Selects low.
HD0-7	Motherboard data bus.
HGL	Glitch. Sets the glitch mode on four slave channels.
HGS	Glitch Slave. Glitch trigger from slave board to master.
HMSS	Macrocell State Select. Selects the State mode for slave.
HOLD	Prevents data storage (MAC counting) until after 16 clocks.
HPHA-D	Four timing clock phases for different analyzer functions.
HR/LW	High read/low write. The CPU programs or reads status.
HRST	Reset. Resets the memory address counter.
HSCS	State Clock Slave. State clock to macrocells in State Mode.
HSWS	State Write Slave. State write enable to RAM in State Mode.
HTSEL	Timing Select. Enables the block selector.
LAS LBS LCS LDS	Patterns from the macrocells when in the State Mode.
LE2	Enable line to the macrocells.
LSTB	Strobe. CPU strobe for reading and writing to timing slave.

Table 8E-2. Mnemonics (Cont'd)

Mnemonic	Description
LTS	Valid Timing Pattern. From slave macrocells to master board.
LWE1-2	Write Enable. Write enables to acquisition RAM.
MA0-7	Memory Address. Memory Address Counter lines to RAM.
LTCK, HTCK	Timing Clock. From motherboard.
TCK1, TCK2, TCK3	Timing Clocks derived from LTCK and HTCK.
THR1	Threshold to the pod from the CPU board

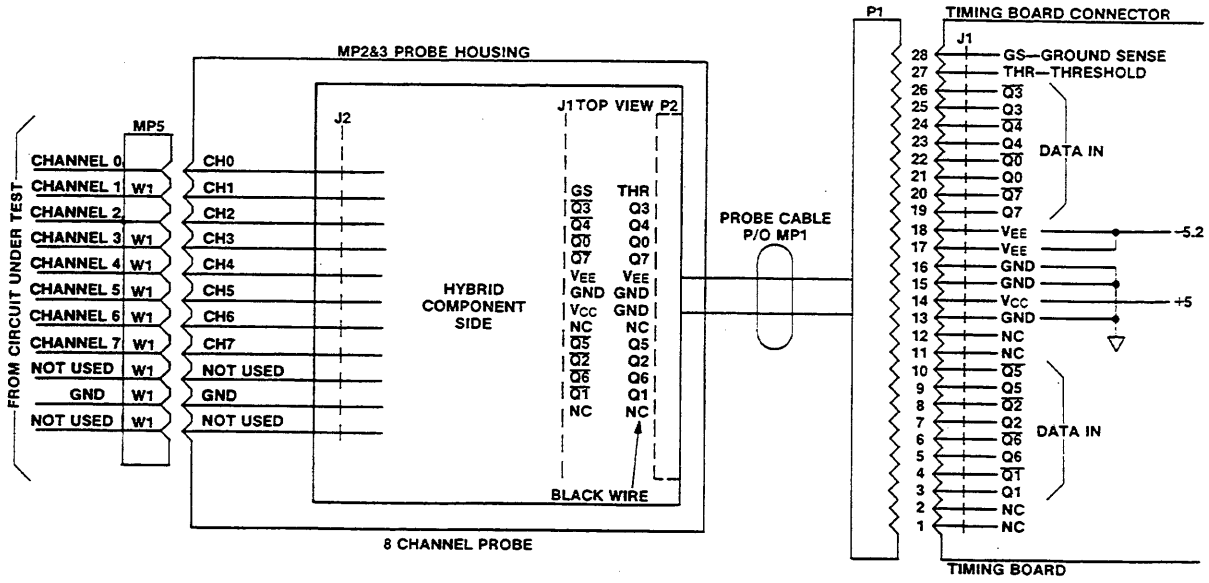
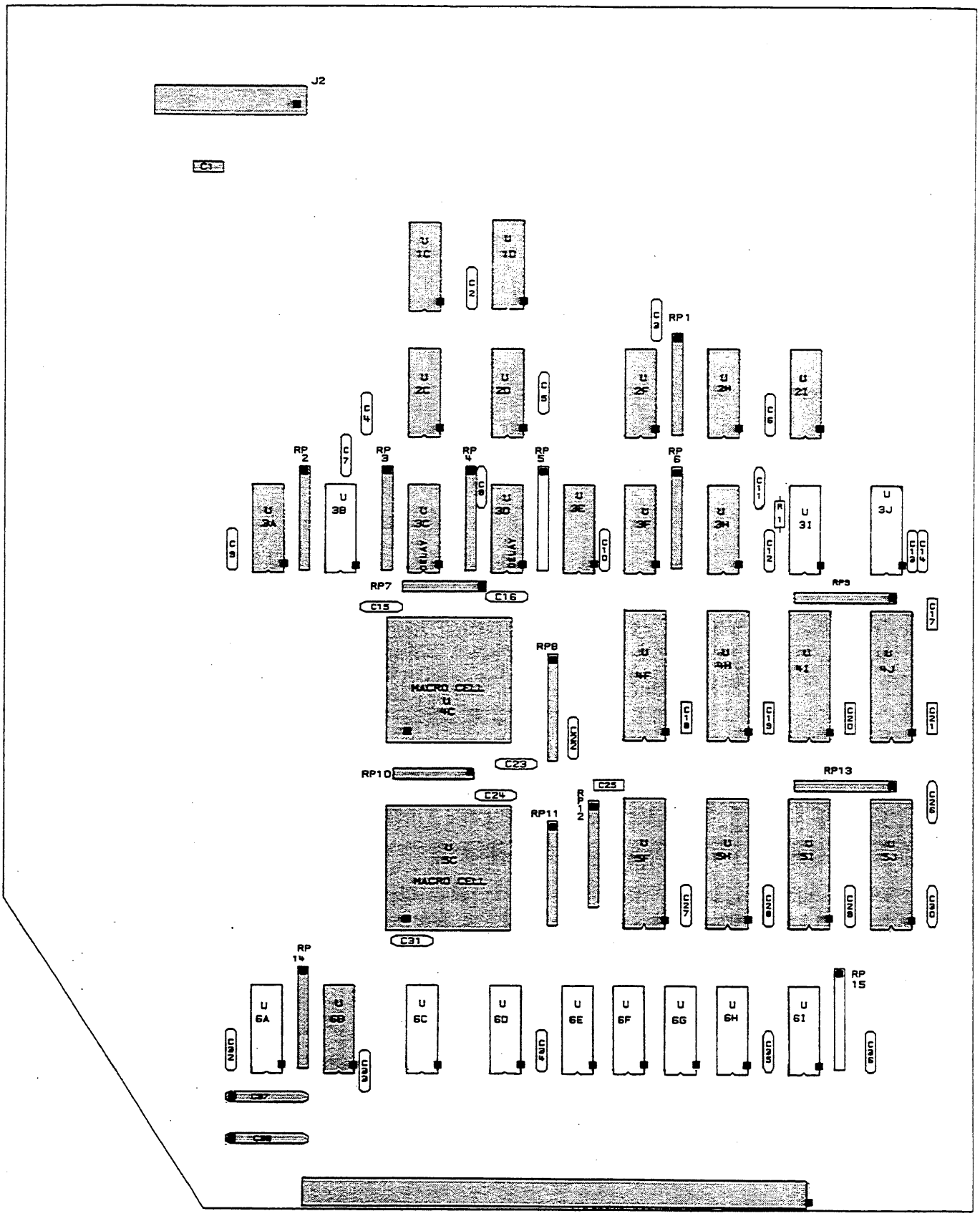
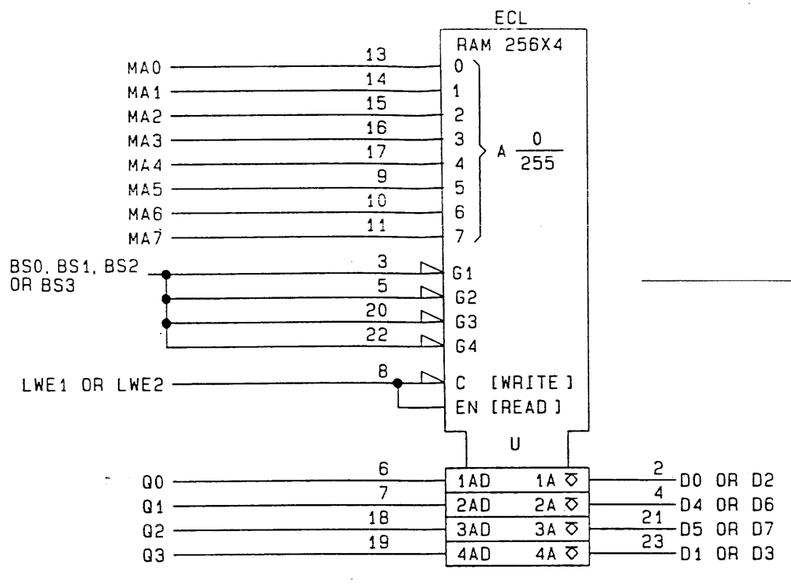


Figure 8E-1. Timing Pod

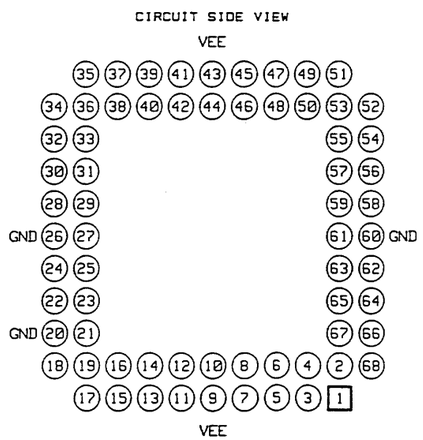


Component Locator for Schematic 8E-1

NOTE 1. RAM PINOUT



NOTE 2. MACROCELL PIN LOCATOR

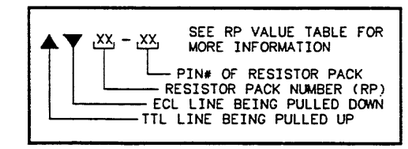


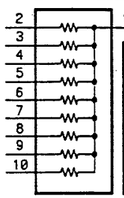
Macrocell Pin-out Diagram.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1C,D,2C,F,H, U2I,3A,F,H,6B
Vcc(gnd) Vee(-5.2)	16 8	U2D
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 24 12	U4F,H,I,J, U5F,H,I,J
-5.2 GND	9,43 20,26,60	U4C,5C

RESISTOR PACK DESCRIPTIONS

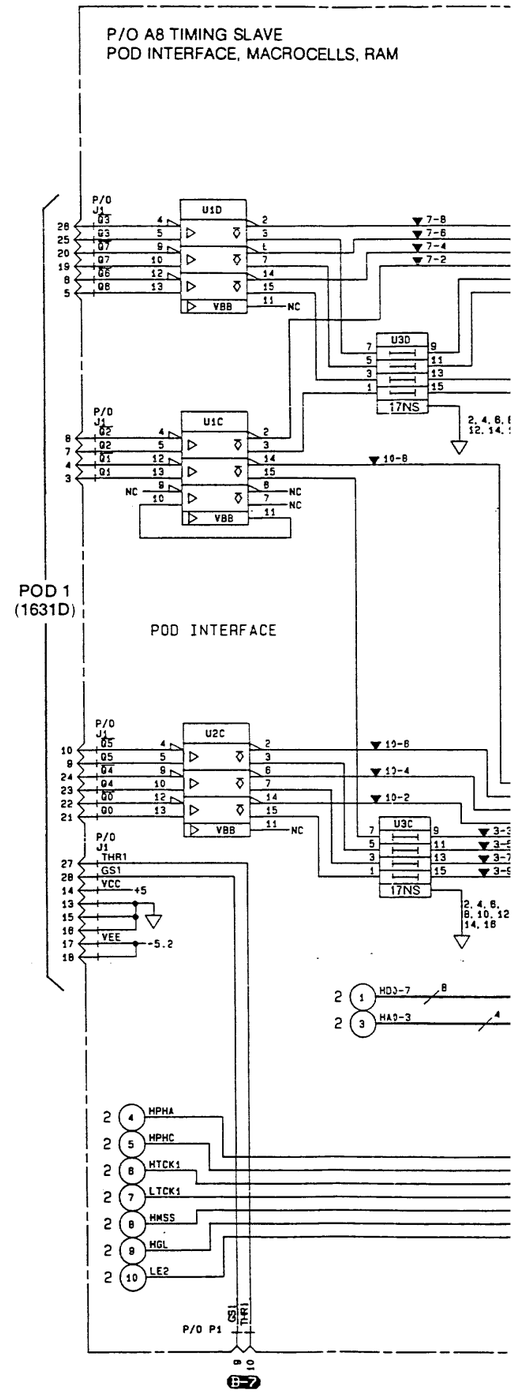


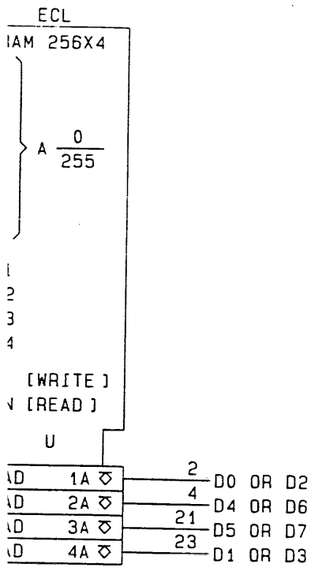


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 8,9 11-15	100 X 9	1	-2.4
7,10	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

C1-12,14-38 J1 RP1-4,6-15 U1C,D,2C,D,F,H,I U3A,C,D,E,F,H, U4C,F,H,I,J, U5C,F,H,I,J, U6B	



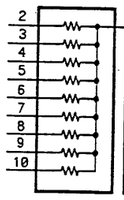


IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U1C,D,2C,F,H, U2I,3A,F,H,6B
Vcc(gnd) Vee(-5.2)	16 8	U2D
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 24 12	U4F,H,I,J, U5F,H,I,J
-5.2 GND	9,43 20,26,60	U4C,5C

RESISTOR PACK DESCRIPTIONS

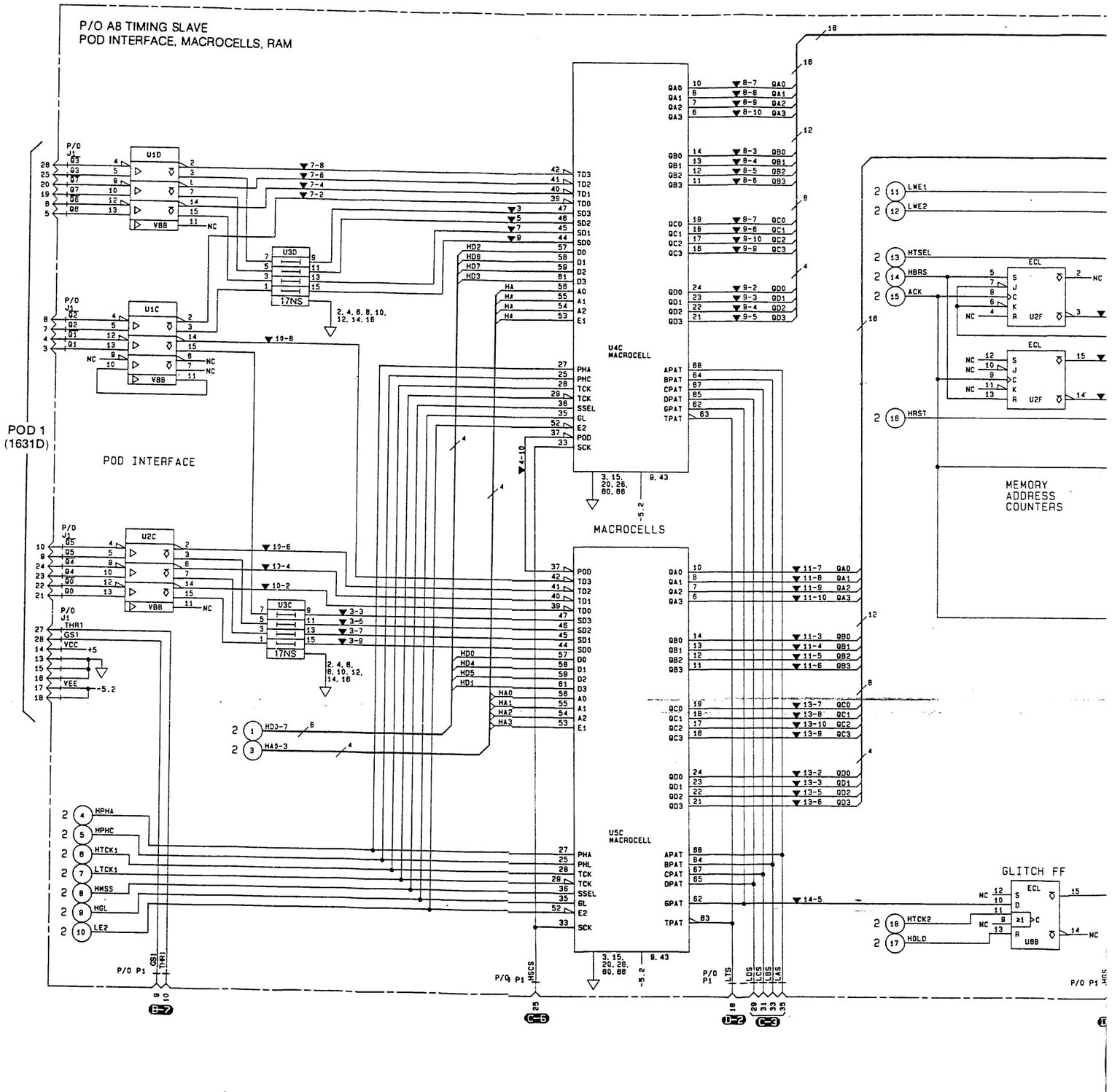
XX - XX
- SEE RP VALUE TABLE FOR MORE INFORMATION
- PIN# OF RESISTOR PACK
- RESISTOR PACK NUMBER (RP)
- ECL LINE BEING PULLED DOWN
- TTL LINE BEING PULLED UP

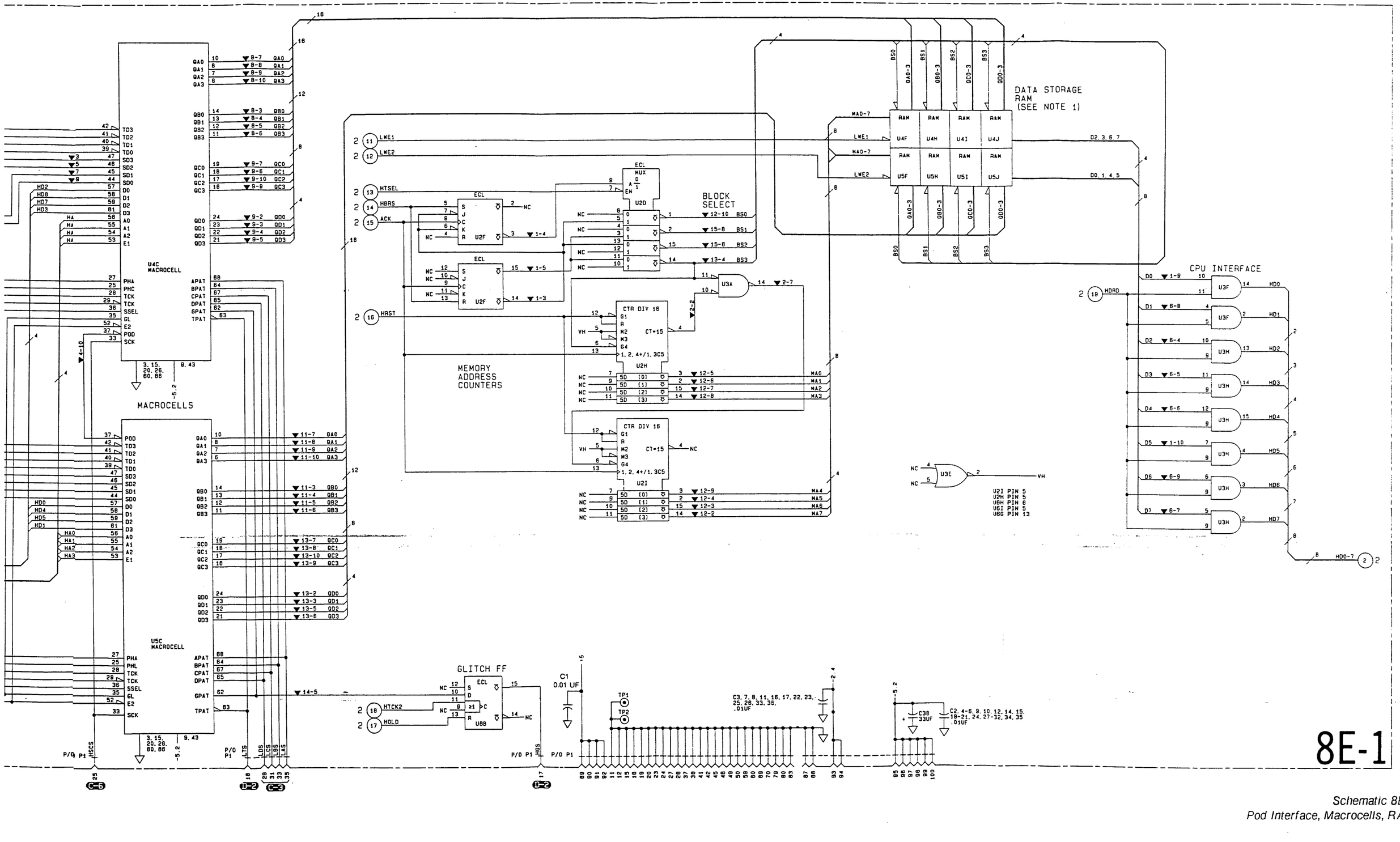


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6 8,9 11-15	100 X 9	1	-2.4
7,10	100 X 4	2,4,6,8	-2.4

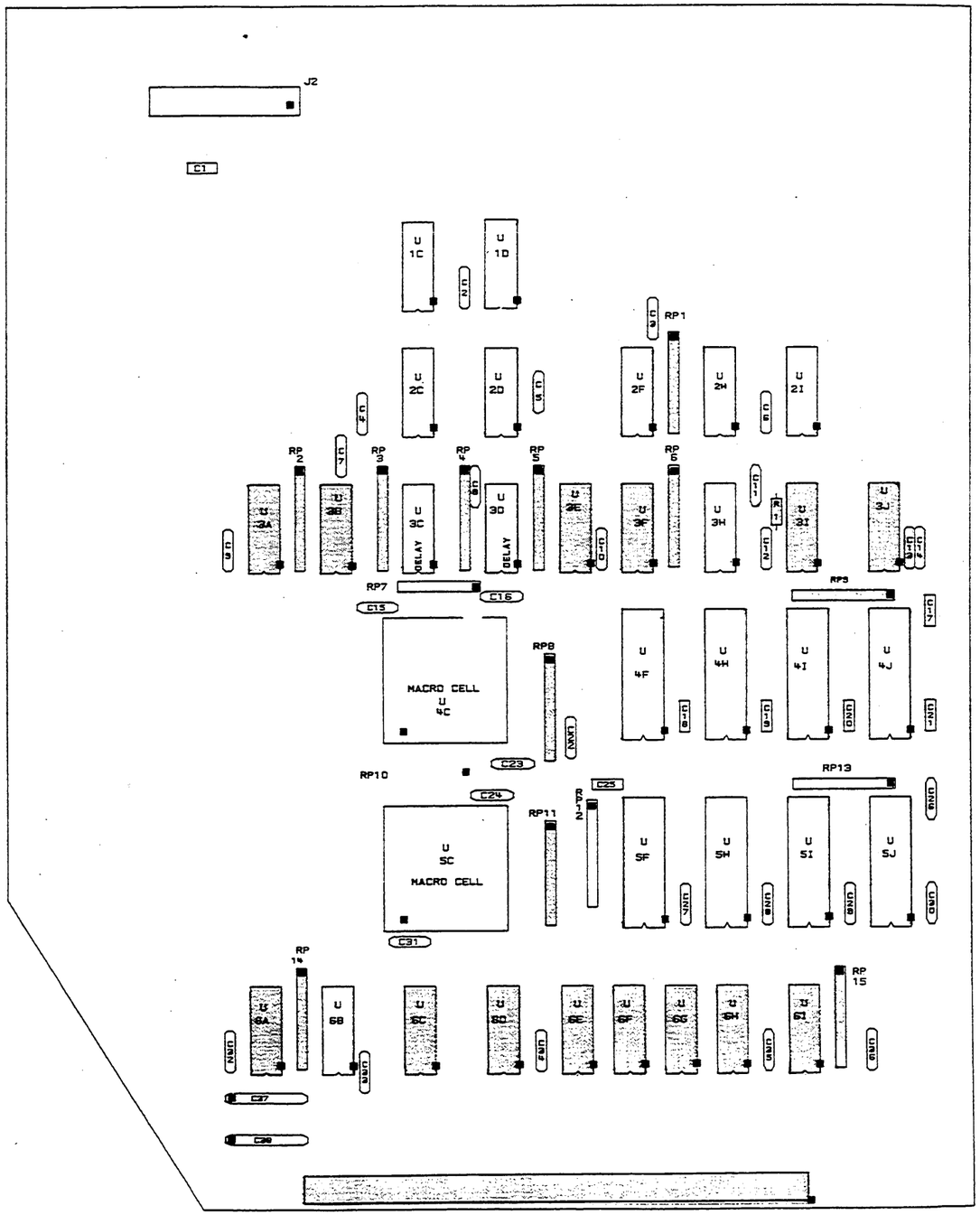
PARTS ON THIS SCHEMATIC

C1-12,14-38 J1 RP1-4,6-15 U1C,D,2C,D,F,H,I U3A,C,D,E,F,H, U4C,F,H,I,J, U5C,F,H,I,J, U6B	





Schematic 8E-1
Pod Interface, Macrocells, RAM
8E-7

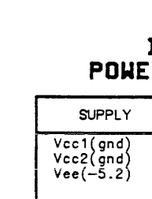


Component Locator for Schematic 8E-2

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
Vcc1(gnd) Vcc2(gnd) Vee(-5.2)	1 16 8	U3A,B,E,F,I,J, U6A,C-I

RESISTOR PACK DESCRIPTIONS:

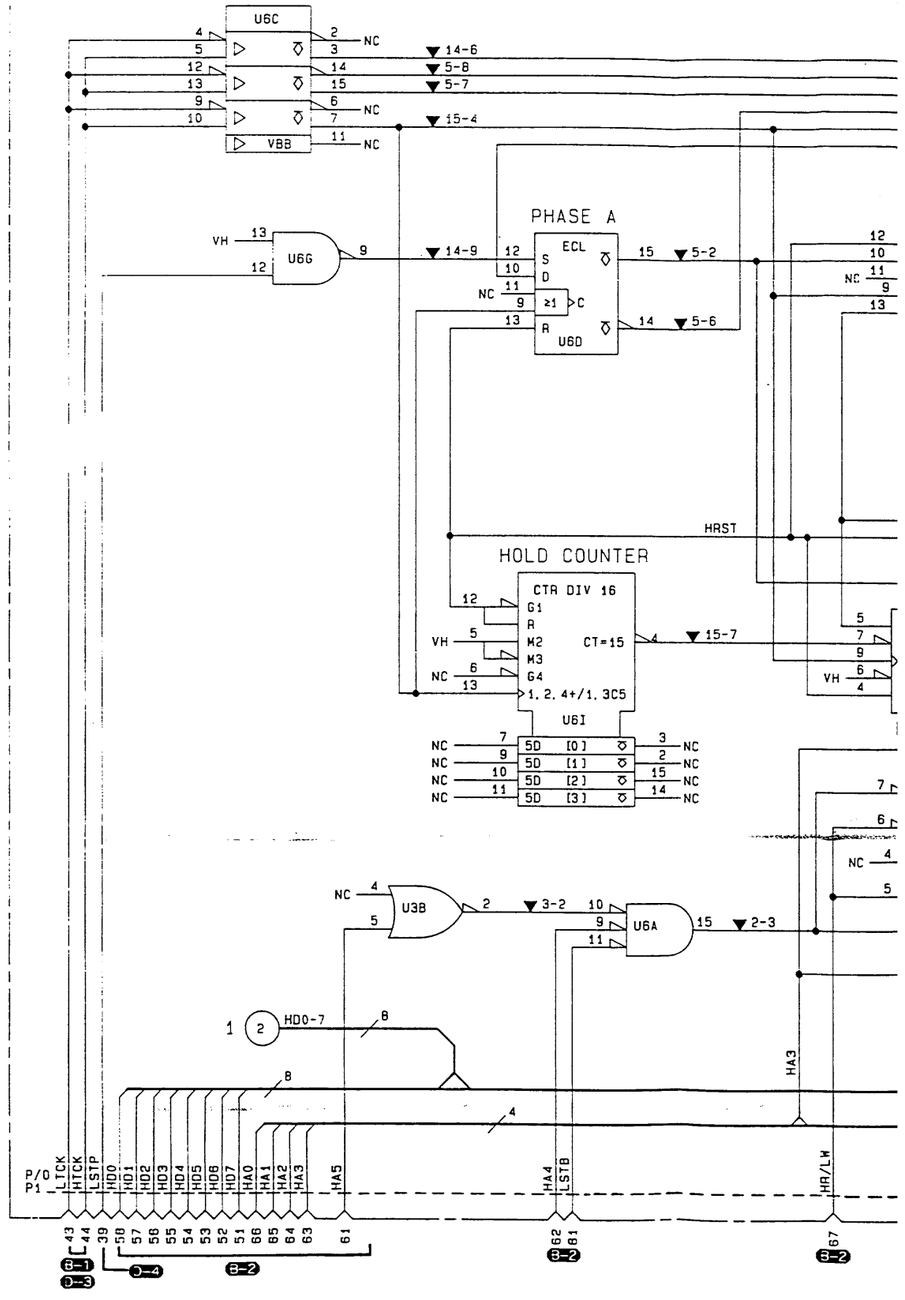


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-6, 8,9, 11-15	100 X 9	1	-2.4
7,10	100 X 4	2,4,6,8	-2.4

PARTS ON THIS SCHEMATIC

C13 R1 RP1-6,8,11,14,15 U3A,B,E,F,I,J,6A, U6C-I	

P/O A8 TIMING SLAVE
MODE AND PHASING



IC DEVICE
NER CONNECTIONS

	PIN NO.	IC GROUP
)	1	U3A,B,E,F,I,J,
)	16	U6A,C-I
)	8	

PACK DESCRIPTIONS:

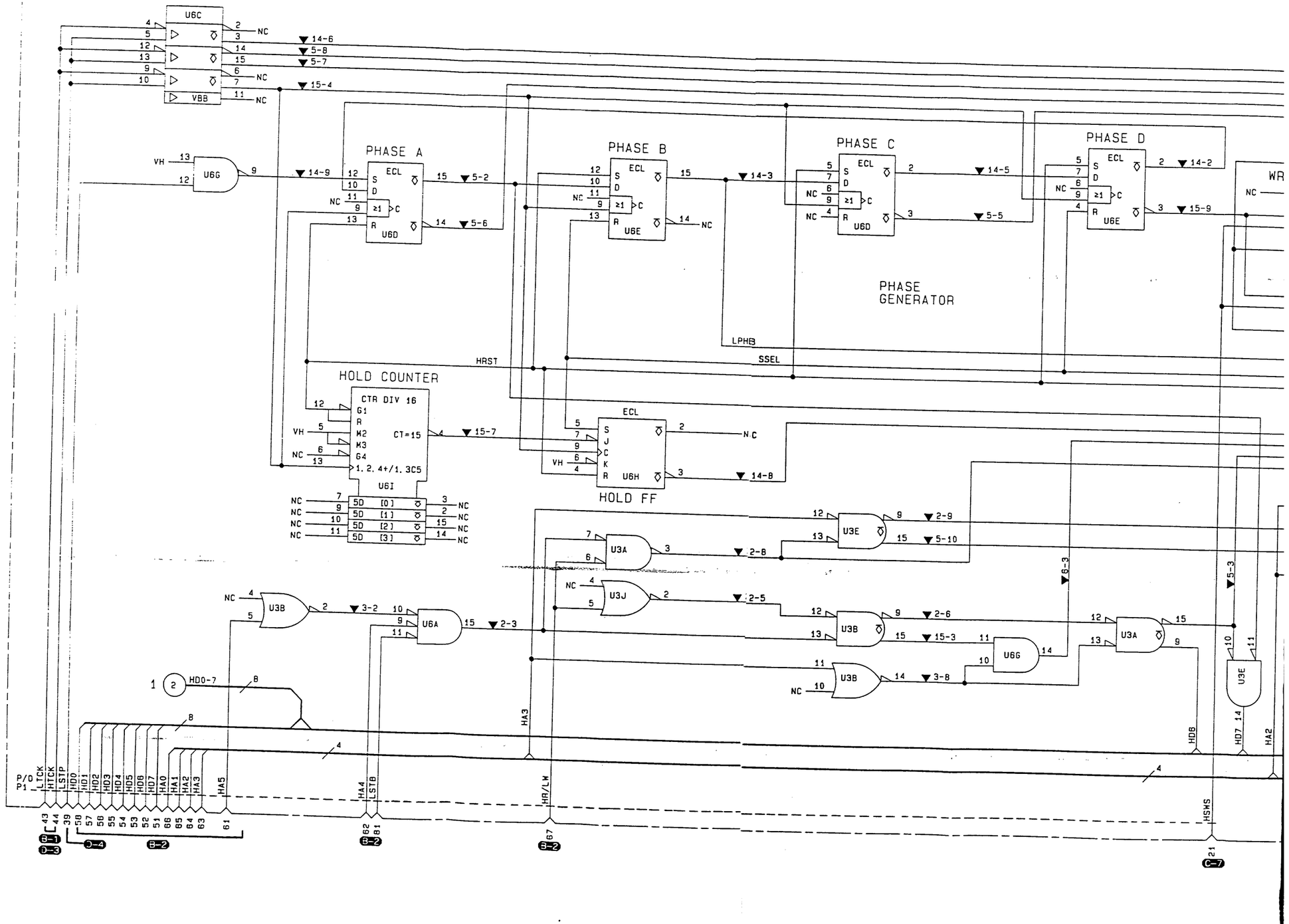
- XX
  - SEE RP VALUE TABLE FOR MORE INFORMATION
  - PIN# OF RESISTOR PACK
  - RESISTOR PACK NUMBER (RP)
  - ECL LINE BEING PULLED DOWN
  - TTL LINE BEING PULLED UP

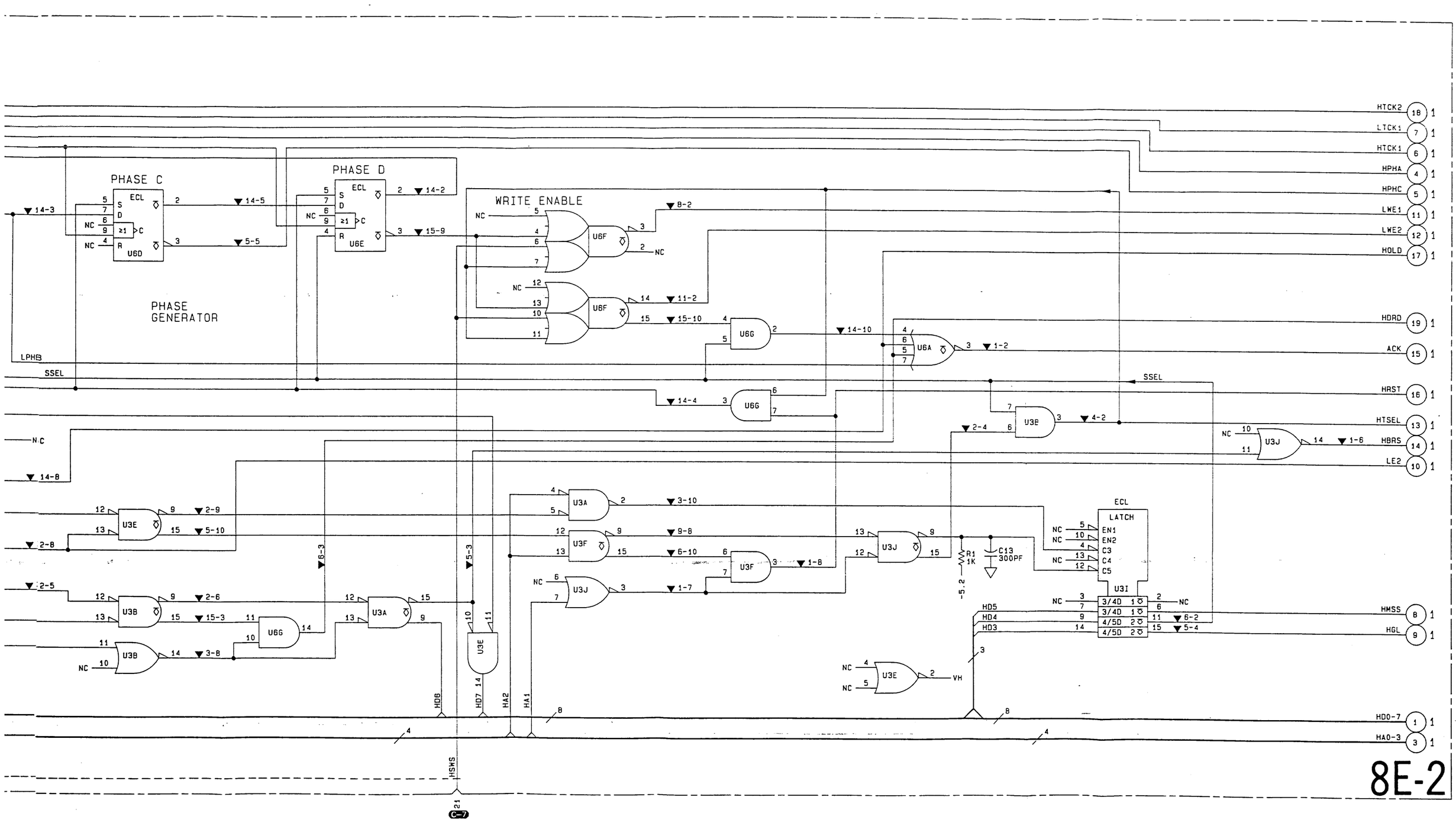
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
-6, 3,9, 1-15	100 X 9	1	-2.4
,10	100 X 4	2,4,6,8	-2.4

ON THIS SCHEMATIC

,14,15 I,J,6A,	

P/O A8 TIMING SLAVE
MODE AND PHASING





8E-2

Schematic 8E-2
Mode and Phasing
8E-9/(8E-10 blank)

Service Group 8F Table of Contents

Paragraph		Page
8F-1.	Introduction	8F-1
8F-2.	State Slave Block Diagram	8F-1
8F-3.	Theory of Operation	8F-4
8F-4.	Data Acquisition Interface	8F-4
8F-5.	Acquisition and Pattern Memory	8F-4
8F-6.	Acquisition Memory	8F-4
8F-7.	Memory Address Counter	8F-4
8F-8.	Pattern Recognition RAM	8F-4
8F-9.	Acquisition and Counter Control	8F-5
8F-10.	Address Decoders	8F-5
8F-11.	Control Data Latches	8F-5
8F-12.	25 MHz Oscillator	8F-5
8F-13.	Time Count Clocking	8F-5
8F-14.	State Count Clocking	8F-5
8F-15.	Gray Code Counter Reset	8F-5
8F-16.	Gray Code Counter and Memory	8F-5
8F-17.	Gray Code Counter	8F-5
8F-18.	Counter RAM	8F-5
8F-19.	EEPROM and Threshold Circuitry	8F-6
8F-20.	Address Decoder	8F-6
8F-21.	Electrically Erasable PROM	8F-6
8F-22.	Address Counter	8F-6
8F-23.	Master Reset	8F-6
8F-24.	Threshold circuitry	8F-6
8F-25.	Mnemonics	8F-7

List of Illustrations

Figure		Page
8F-1.	State Slave System Block Diagram	8F-3
8F-2.	State Slave Pod	8F-9

List of Tables

Table		Page
8F-1.	Master and Slave State Board Comparison	8F-1
8F-2.	Mnemonics	8F-7

List of Schematics

Schematic		Page
8F-1.	Data Line Receivers, Sample Latches/Pattern Programming Counters	8F-11
8F-2.	Memory Address Counter and RAM	8F-13
8F-3.	25MHz Oscillator, Address Decoders, Counter Control	8F-15
8F-4.	+5V Reference, Grey Code Counter, Counter RAM	8F-17
8F-5.	EEPROM Control, EEPROM, Threshold Circuitry	8F-19

SERVICE GROUP 8F
STATE SLAVE

8F-1. INTRODUCTION

The optional state slave board adds thirty channels of state data to the 1630A. A 1630D can be upgraded to replace eight timing/state channels with thirty state channels. The 1630G thus provides fifty-seven state channels and eight timing/state channels.

The State Slave board adds state count and time count for state listings. It also provides non-volatile memory for storing instrument setup and microprocessor program disassemblers.

Table 8F-1. Master and Slave State Board Comparison

STATE MASTER BOARD	STATE SLAVE BOARD
Three Data Clock Inputs	
27 Data Inputs	30 Data Inputs
Acquisition RAM (1K x 28)	Acquisition RAM (1K x 32)
Pattern RAM	Pattern RAM
Measurement Control Circuitry	
Data Clock Processing	
	State and Time Counter
	Two Threshold Circuits
	EEPROM Memory for CPU

8F-2. STATE SLAVE BLOCK DIAGRAM

(see Figure 8-1)

POD INTERFACE. Input data from up to three 10-bit pods is taken at the user's sample rate.

ACQUISITION MEMORY. The width of the acquisition memory is 32 bits. Thirty bits are used for data from the system under test and two bits are used to send the condition of two flags to the 1630 microprocessor.

MEMORY ADDRESS COUNTER. Holds the address of the next location in acquisition memory to be filled. This counter also addresses the time interval RAM.

PATTERN RECOGNITION RAM. Input width is 32 bits and output width is 4 bits. Two of the input bits are unused. The CPU pre-loads the RAM, so that a particular 30-bit data pattern will address a 4-bit word corresponding to one of the four specified patterns.

GRAY CODE COUNTER. The Gray Code Counter is a 20-bit counter used to count stored states, time intervals, or the number of occurrences of a particular event over a period of time. It has a 20-bit gray code output.

COUNTER RAM. This RAM stores the output of the Gray Code Counter. Both time counts and state counts are stored, depending on the instrument setup.

ADDRESS DECODERS. The address decoders, two in the control circuitry and one in the EEPROM circuitry, split the available addressing into two sections, one for the primarily ECL control circuitry and the other for the primarily TTL EEPROM circuitry. Further decoding controls latching of data onto and off of the microprocessor data bus.

25 MHZ OSCILLATOR. The 25 MHz oscillator clocks the Gray Code Counter. The 25 MHz signal is also used to synchronize other control signals for the counter.

CONTROL CIRCUITRY. The control circuitry provides the various control lines and clocks.

THRESHOLD CIRCUITRY. The threshold circuitry provides threshold to pods 6 and 7. Ground sense lines provide the ground level of the system under test.

EEPROM CIRCUITRY. EEPROM memory is used to store the inverse assembler data loaded from tape or disc. It is also used to store instrument setups. Only the microprocessor has access to EEPROM. None of the storage space is used for data from this board.

EEPROM is a non-volitile memory that operates on TTL levels, therefore requires the accompanying buffers and translators. An address counter is also included.

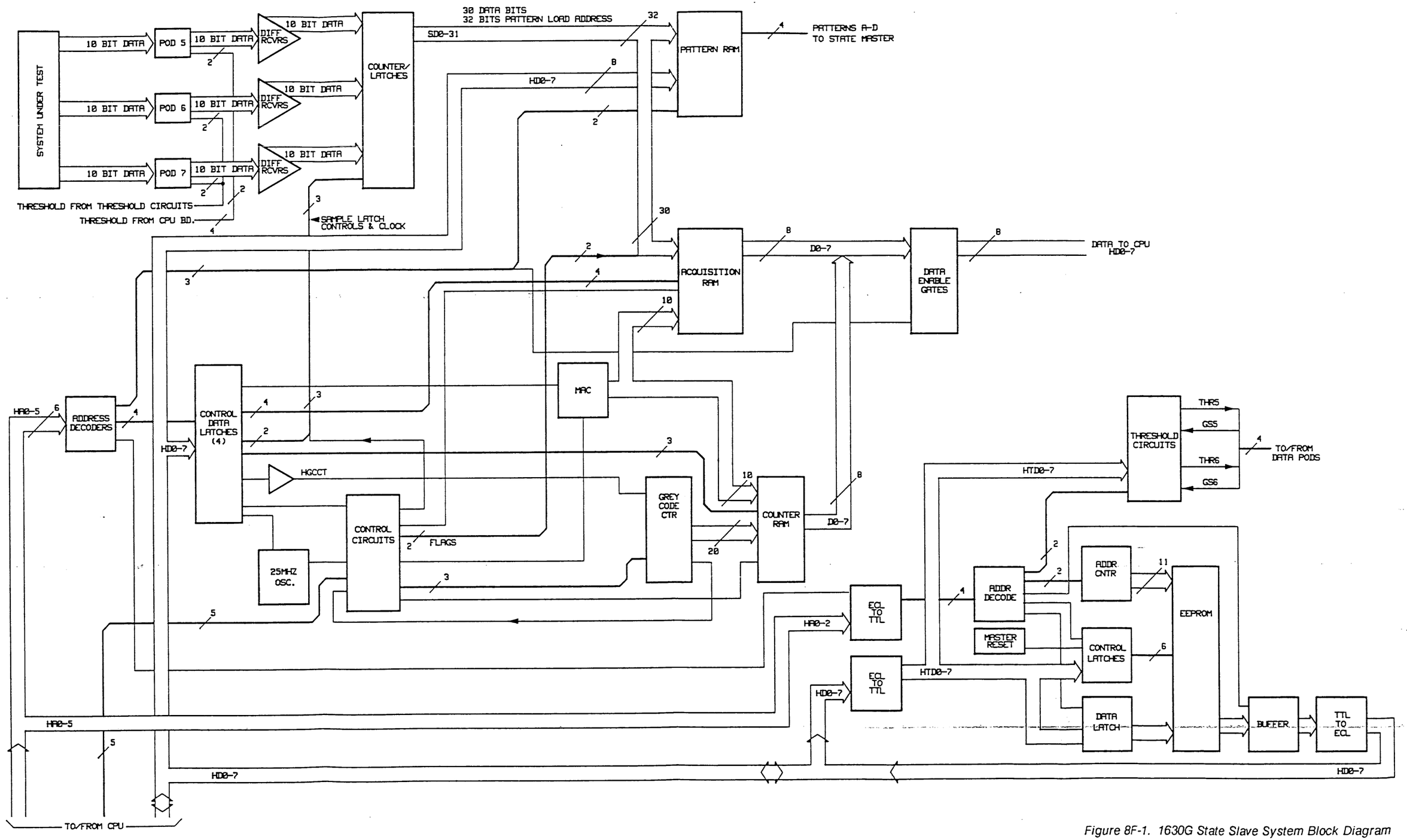


Figure 8F-1. 1630G State Slave System Block Diagram

8F-3. THEORY OF OPERATION

8F-4. Data Acquisition Interface (see schematic 8F-1)

Three pods (5, 6, 7) each supply ten channels to the line receivers. The ten channels from each pod go from line receivers into 4-bit counters, (U2B-U2I). The counters work as data sample latches during a run and as address counters for programming Pattern Recognition RAM before a run. SLM selects either the latch mode or counter mode. It is low in the latch mode. SLCLK clocks data through the latches in the run mode and toggles the counters to address the pattern rams when the microprocessor is loading patterns. HSLR resets the counter/latch with a high.

The CPU board supplies ground sensing and precision threshold for pod 5. Pods 6 and 7 thresholds are provided by circuitry on this board (schematic 8F-5).

8F-5. Acquisition and Pattern Memory (see schematic 8F-2)

8F-6. ACQUISITION MEMORY. The acquisition RAM is organized as 32 bits wide by 1024 words deep--30 bits for data storage, with 2 bits used to send the condition of two flags to the microprocessor. The 30 data channels are written into memory in parallel. During an acquisition cycle all four select lines (LARS1-4) are pulled low. The write enble line (LARWE) is also pulled low. When a qualified state is present on the data lines LARWE is put high, the memory address counter is incremented and LARWE put low again.

To read data from RAM, LARWE is put high and the select lines select RAM pairs to output eight-bit data on to the bus.

8F-7. MEMORY ADDRESS COUNTER. The Memory Address Counter consists of three 4-bit counters, of which ten bits are used. It addresses both the acquisition RAM and the counter RAM (schematic 8F-4). HMACR is the reset line and MACCLK is the clock.

8F-8. PATTERN RECOGNITION RAM. Pattern Recognition RAM consists of four 256 x 4 ECL RAM ICs connected in parallel, allowing an addressing width of 32 bits. Input width is 30 bits--two of the address lines do not carry data. Output width is 4 bits. The 30-bit incoming sample from the data pods addresses Pattern Recognition RAM. The four bits from each RAM location go out over the pattern lines, LAS-LDS, to the State Master board where they are ANDed with pattern lines from the State Master board and Timing board.

Before a run, the CPU pre-loads each 4-bit RAM location. The locations are addressed by the sample latches working in the counter mode. During a run, when a RAM location is addressed by the incoming sample, its four bits are output on the four pattern lines A-D. When one or more of these four bits is low, the corresponding pattern line may be driven low. A 30-bit incoming data sample that forms a pre-specified pattern of highs, lows, and don't-cares will address one of those RAM locations that was pre-loaded with at least one low.

For example, if the eight input sample bits to a single RAM chip are 00000000, then the first location will be addressed. If the four bits stored in that location are 1100, then pattern output lines A and B--corresponding to the two lows--from that RAM will try to go low.

However, each of the four output bits from each pattern RAM are ECL wire-ANDed. (ECL outputs may be connected together like open-collector TTL outputs.) Thus, a pattern line can be active only when all four RAMs have a low on the same output.

As shown in figure 8C-3, four pattern lines also come into the State Master board from the Timing Master board. (The State Slave board takes the place of the Timing Slave board.) When the Timing Master board is in the state mode, the macrocells act like pattern recognition RAM. The pattern lines from the Timing Master and State Slave boards are gate-ANDed, then wire-ANDed with the four State Master pattern lines. Thus, for a single pattern line to be driven low, the Timing Master and State Slave boards and all four RAM chips on the State Master board must agree. (When the timing board is not in the state mode, its pattern lines will be low).

If more than one of the pattern lines is low at the same time, the sequencer will select the one required for the next analyzer state, according to the trace specification.

8F-9. Acquisition and Counter Control (see schematic 8F-3)

This circuitry provides control for most of the ECL circuitry on the board. the Address Decoders and Control Data Latches allow the CPU to control measurements. A 25 MHz oscillator is used as a time reference for timing measurements. The Reset Flip-Flops are used to reset the Gray Code Counter.

8F-10. ADDRESS DECODERS. The Address Decoders (here and on schematic 8F-5) split the 16 available addresses into two groups of eight, one group for ECL control and one for TTL control. The eight low order addresses of the two groups are decoded here by U8N and U8M. LTTL, from U8N pin 11, is used to select the TTL group on schematic 8F-5. The outputs of U8M control output of acquisition data onto the bus (HADE), writing of data into pattern RAM (LPRWE1,2), and latching of data into the control circuitry.

8F-11. CONTROL DATA LATCHES. These latches control configuration of the circuitry for making the specific measurements. Performance and operation verification signals are also outputs into the control circuitry.

8F-12. 25 MHZ OSCILLATOR. The 25 MHz Oscillator clocks the Gray Code Counter (schematic 8F-4) in the time count mode. The oscillator is also used to synchronize part of the counter reset circuit.

8F-13. TIME COUNT CLOCKING. The 25 MHz path through the control circuitry is from U8I pin 6, through U7I pins 7 and 3, and U8I pins 5 and 3 onto the GCCCLK line. A high at U5M pin 14 will disable the oscillator so that the CPU can clock the counter for test purposes.

The 25 MHz signal is gated by U8K pin 2. A high on the set input, pin 5, inhibits the 25 MHz with the resulting low at pin 2. When the set is removed, the clock signal at pin 6 will synchronize the return of pin 2 to a high level so that only complete clock pulses will be gated.

8F-14. STATE COUNT CLOCKING. When the counter is used to count states the 25 MHz line, GCCCLK, is put high by U5L pin 13. The GCCSI line, which must be high for 25 MHz clocking, is now used as a clock. The source of the clock is HSCS which is derived on the State Master board. Forms of it are used there to clock data and address counters.

8F-15. GRAY CODE COUNTER RESET. Five flip-flops synchronize the reset of the Gray Code Counter. U7KA catches the overflow from the MSB of the counter when the count has reached about 350K. U7LA synchronizes the output of U7KA with the control system The output from pin 2 is also used to flag the CPU that the counter is resetting (HCRF). U7LB resets the counter after a qualified state has been stored. U7MA/B sequence the reset of the counter. The output of U7MA is also used to reset the reset flip-flops.

8F-16. Gray Code Counter and Memory (see schematic 8F-4)

8F-17. GRAY CODE COUNTER. The Gray Code Counter is a 20-bit counter with a 17-bit mantissa (bits 0-16) and 3-bit exponent (bits 17-19). The CPU uses algorithms to convert the gray code to the count figure.

U4M and Q1 are a power supply which provides -3.25V ±3%. U8L is part of the reset circuit. The reset signal HGCCR resets the counter. U8L provides a complementary signal that is delayed by C64. The delayed signal terminates reset at pins 33 and 34.

8F-18. COUNTER RAM. The Counter RAM is addressed by the Memory Address Counter (schematic 8F-2). A count can be stored for each valid state stored. LCRS1-3 gate the RAMs and allow them to be read onto the data bus eight bits at a time. LCRWE is the write enable. It goes high at the termination of write when the valid state has been stored.

8F-19. EEPROM and Threshold Circuitry (see schematic 8F-5)

The Electrically Erasable PROM is used by the CPU for storage of one instrument setup and storage of inverse assemblers written to the 1630G from disc or tape.

8F-20. ADDRESS DECODER. The address decoder decodes the eight high order addresses alloted to the state slave board. The LTTL signal, decoded in U8N (schematic 8F-3), allows decoding of HA0-2 by U7C. The decoded signals primarily control latching of data into and out of EEPROM and latching of data into the Threshold DACs. Two lines clock and reset the Address Counter.

U6L is part of a board identifier. The CPU does a read from address hex 10 which outputs, through U6L, a hex 20 onto the data bus. That identifies this board as a state slave. The CPU therefore knows the configuration of the instrument.

8F-21. ELECTRICALLY ERASABLE PROM. The EEPROM is controlled very much like a comparable CMOS RAM. However, it is nonvolitile but can be erased by writing over data previously stored. CPU data is converted to TTL from the ECL on the data bus. It is latched onto a bus connecting all EEPROMS. The EEPROMs have inputs that also serve as outputs but are shown separately on the schematic.

When the EEPROMS are read, the data is gated onto the data bus by U7G. The pull-ups on the output of U7G provide additional drive to the TTL-ECL converters. This ensures that when the data buffer is disabled and has high outputs the TTL-ECL inputs will be high enough to ensure low outputs. This allows other devices to drive the bus.

8F-22. ADDRESS COUNTER. The Address Counter consists of three 4-bit counters of which 11 bits are used. A fourth counter is connected but not used. The counter is clocked and reset by the CPU.

8F-23. MASTER RESET. The Master Reset holds off the write circuitry from the EEPROMS when the power supply voltage is out of tolerance. All outputs of U7E are low in the reset mode. U7D functions only as an inverter to keep the control inputs of the EEPROMS high to prevent writing erroneous data upon power-up.

8F-24. THRESHOLD CIRCUITRY. The Threshold DACs are programmed by the data bus to provide a current level proportionate to the threshold level required. The current level is converted to a voltage level by U6B. The ground sense lines compensate the threshold for differences in ground level in the target system.

8F-25. MNEMONICS

The following signals, listed in alphabetical order, are used on the State Slave Board. Active high signals have "H" as the first letter; active low signals have "L". Most signals on the State Slave board are ECL. Worst case voltage levels are as follows: LOW = less than -1.50V; HIGH = greater than -1.10V.

Table 8F-2. Mnemonics

Mnemonic	Description
D0-7	Data from counter RAM.
GCCCLK	GRAY CODE COUNTER CLOCK/Enable. Clocks the Gray Code Counter in the time count mode. Must be high to enable state count clock, GCCSI.
GCCSI	GRAY CODE COUNTER STATE INCREMENT/Enable. Clocks the Gray Code Counter in the state count mode. Must be high to enable time count.
GS5,6	GROUND SENSE. Ground level voltage sense from target system.
HA0-5	CPU Address Bus from 1630 CPU board.
H/LACK	Address Clock. Increments memory address counter.
HADE	ACQUISITION DATA ENABLE. Enable for acquisition RAM data onto system data bus.
HCRF	COUNTER RESET FLAG. Flags the 1630 CPU when the Gray Code Counter is resetting.
HD0-7	1630 System Data B to CPU board.
HGCCOF	GRAY CODE COUNTER OVERFLOW.
HGCCR	GRAY CODE COUNTER RESET. Positive edge initiates counter reset.
HGCCT	GRAY CODE COUNTER TEST. During performance verification is used to divide the counter into two 10-bit sections for faster testing.
HMACR	MEMORY ADDRESS COUNTER RESET.
HSCS	State Clock Slave. State clock for State Mode.
HSLR	SAMPLE LATCH RESET. Resets the Data Sample Latch/Pattern Programming Counters.
HSWS	State Write Slave. State write enable to RAM in State Mode.
LARS1-4	ACQUISITION RAM SELECT. Select acquisition RAM pairs. All lines go low during data run. Enables RAM pairs during reads onto the system data bus.

Table 8F-2. Mnemonics (Cont'd)

Mnemonic	Description
LAS LBS LCS LDS	Patterns from the Pattern Recognition RAM.
LARWE	ACQUISITION RAM WRITE ENABLE. Low during an acquisition run. Goes high when data on input lines is valid so data is stored. Put low to read data onto system data bus.
LCRS1-3	COUNTER RAM SELECT. Selects Counter RAM pairs to read data onto the system data bus.
LCRWE	COUNTER RAM WRITE ENABLE. Enables write to Counter RAM. Low-to-high edge terminates write when counter data is valid.
LCRZF	COUNTER RAM ZERO FLAG. When set, tells the CPU that the contents of the Counter RAM is to be interpreted as zero.
LPRWE1,2	PATTERN RAM WRITE ENABLE. Allows writing of pattern data from CPU into Pattern RAM.
LSTB	Strobe. CPU strobe for reading and writing to slave boards.
LTTL	Decoded address that selects TTL circuitry for addressing.
MA0-9	MEMORY ADDRESS. Addressing bus for Acquisition RAM and Counter RAM.
MACCLK	MEMORY ADDRESS COUNTER CLOCK. Clocks Memory Address Counter during acquisition using clock derived from target system. CPU clocks counter during read from RAM.
SD0-31	SAMPLE DATA. Data from target system that has been latched for use by Acquisition RAM and Pattern RAM.
SLCLK	SAMPLE LATCH CLOCK. Clock derived from target system during run mode. CPU clocks latch/counters during programming mode for Pattern RAM.
SLM	SAMPLE LATCH MODE. Selects latch or count mode for latch/counters.
THR5,6	THRESHOLD. Threshold voltage for Pods 6 and 7.

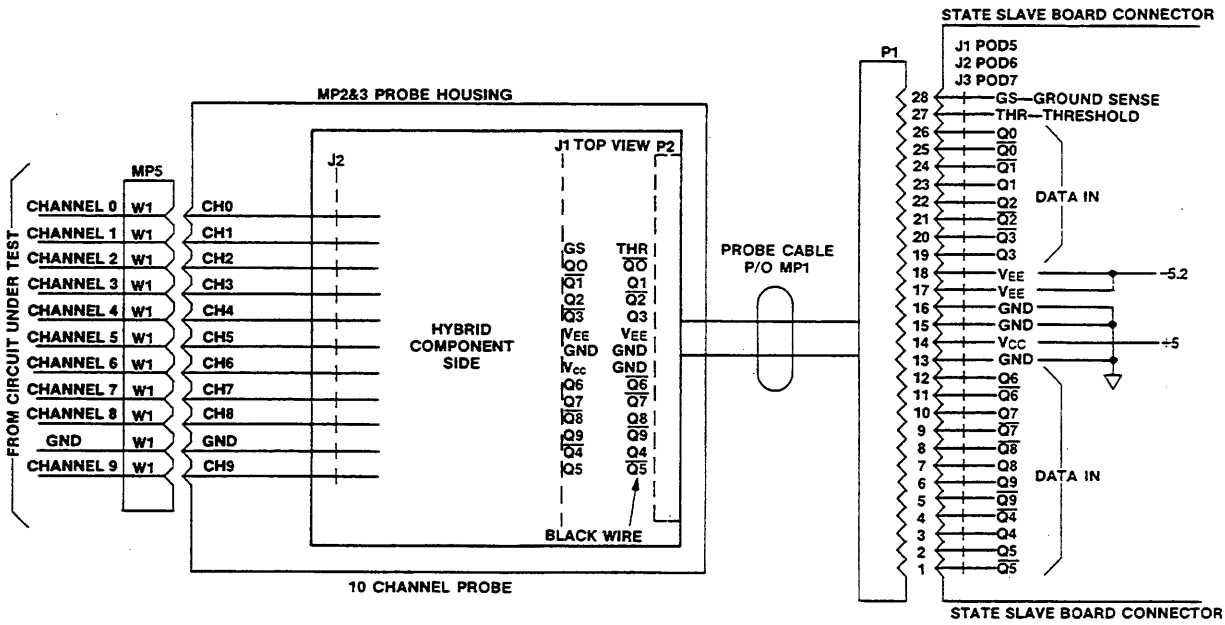
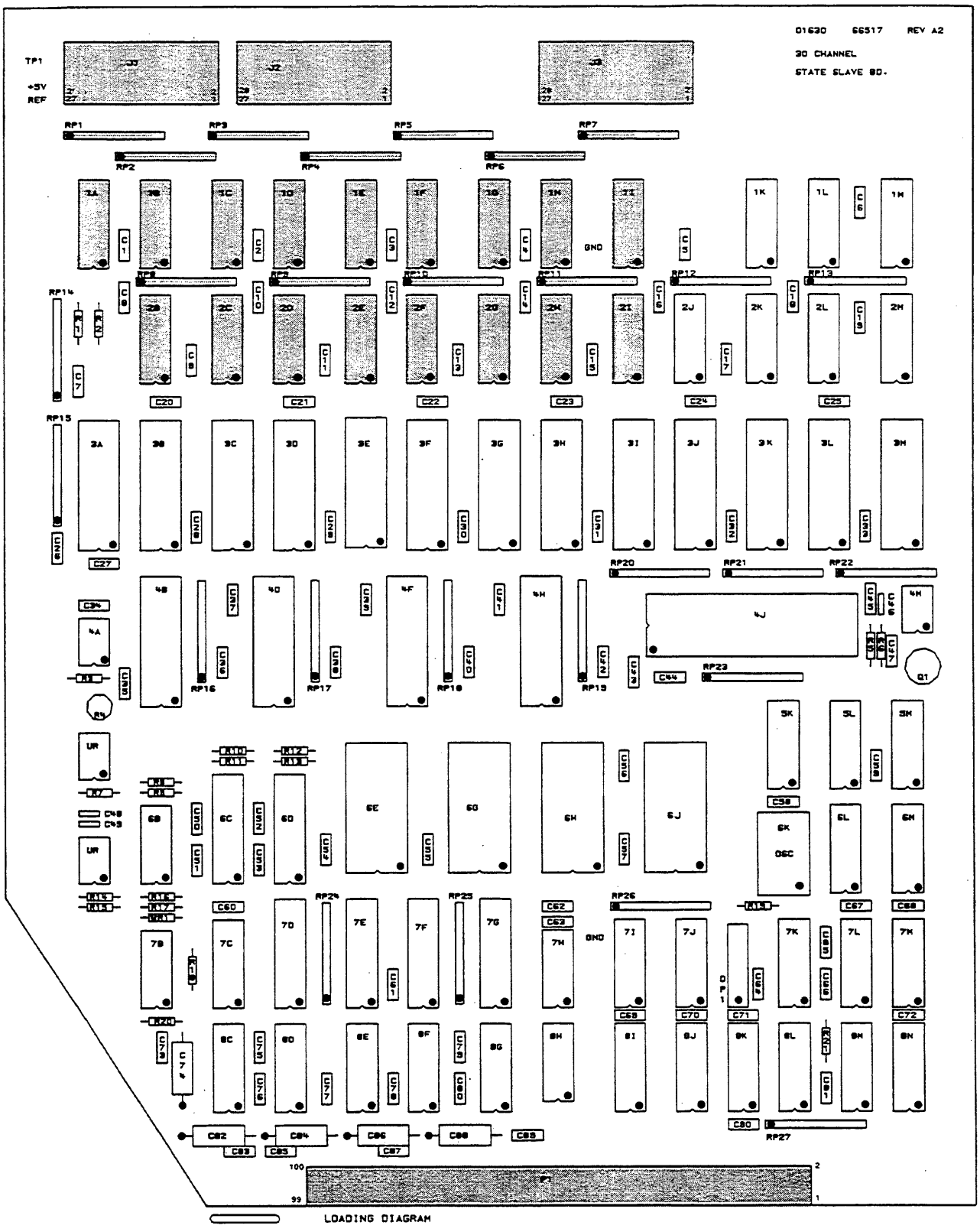


Figure 8F-2. State Slave Pod

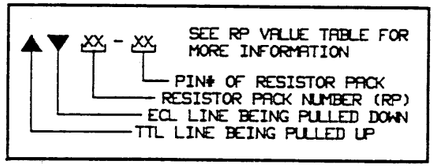


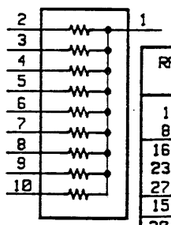
Component Locator for Schematic 8F-1

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:



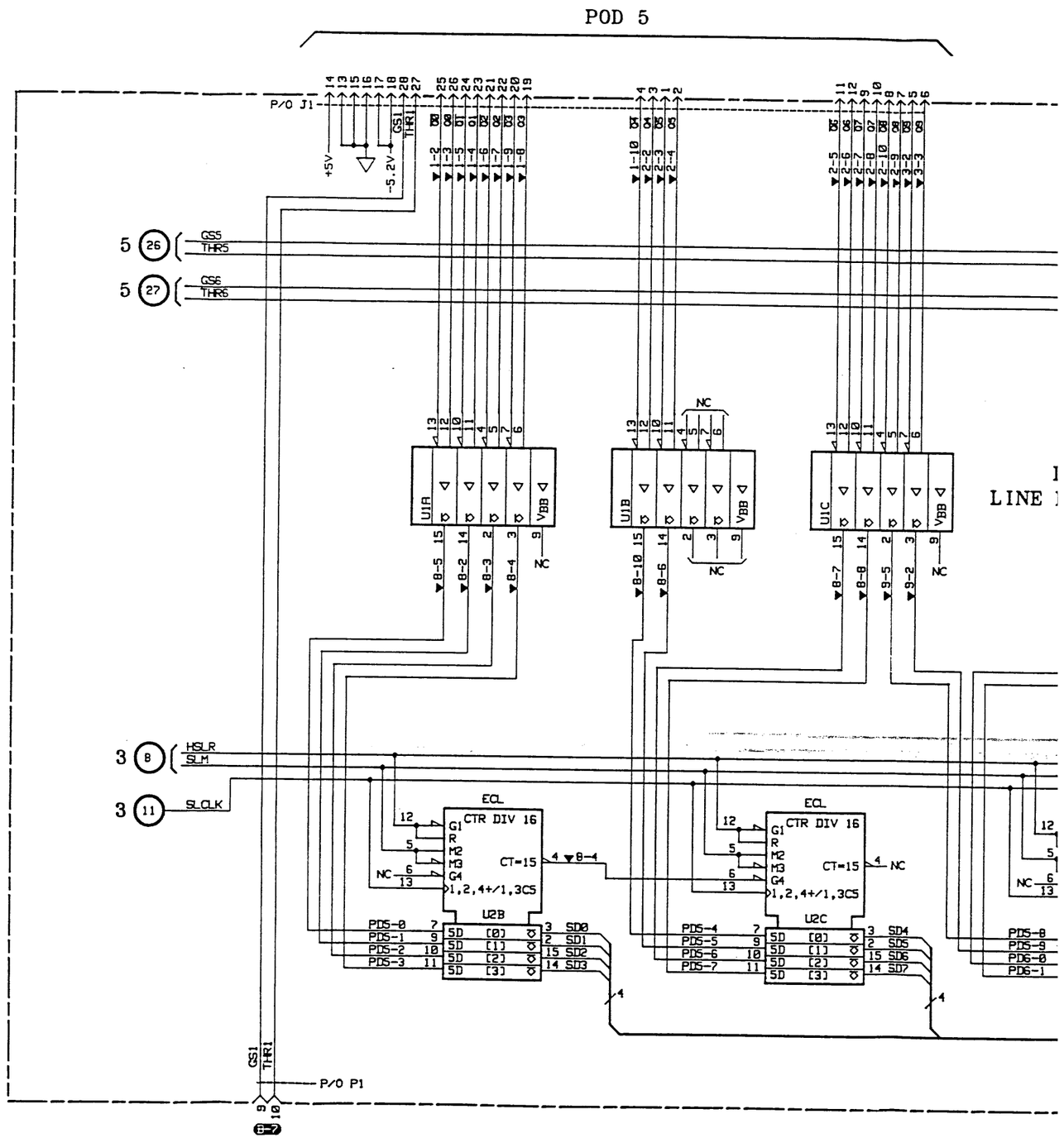


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

J1-3 P/O P1 RP1-11 U1A-I U2B-I	

DATA AQUISITION INTERFACE



DATA AQUISITION INTERFACE

VICE NECTIONS

O.	IC GROUP
	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
	U3A-M U4B,D,F,H
	U6E,G,H,I
	U6L,M U8C-G
	U7C
	U7D-G
	U7H U8H
	U7J

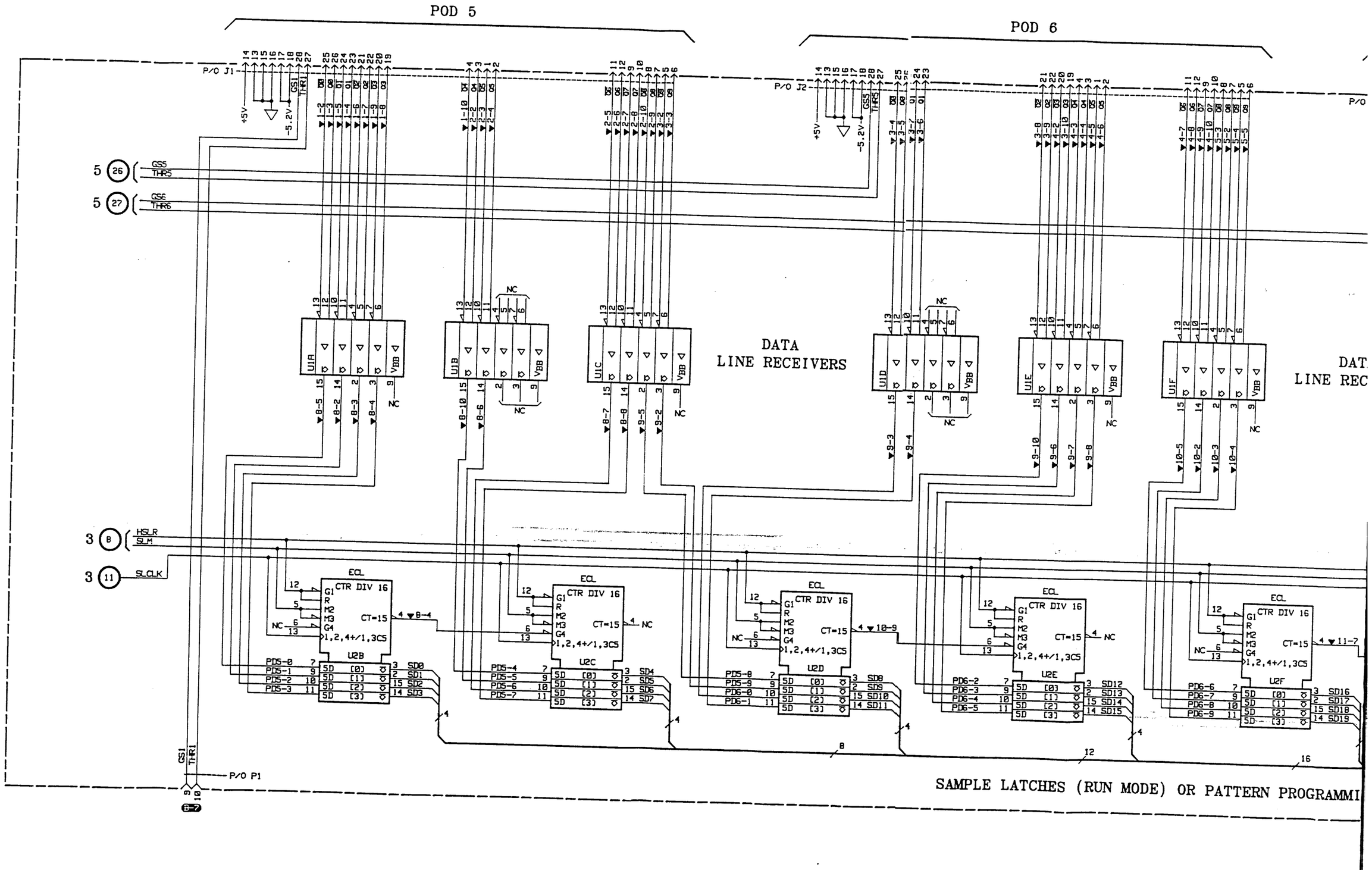
ESCRIPTIONS:

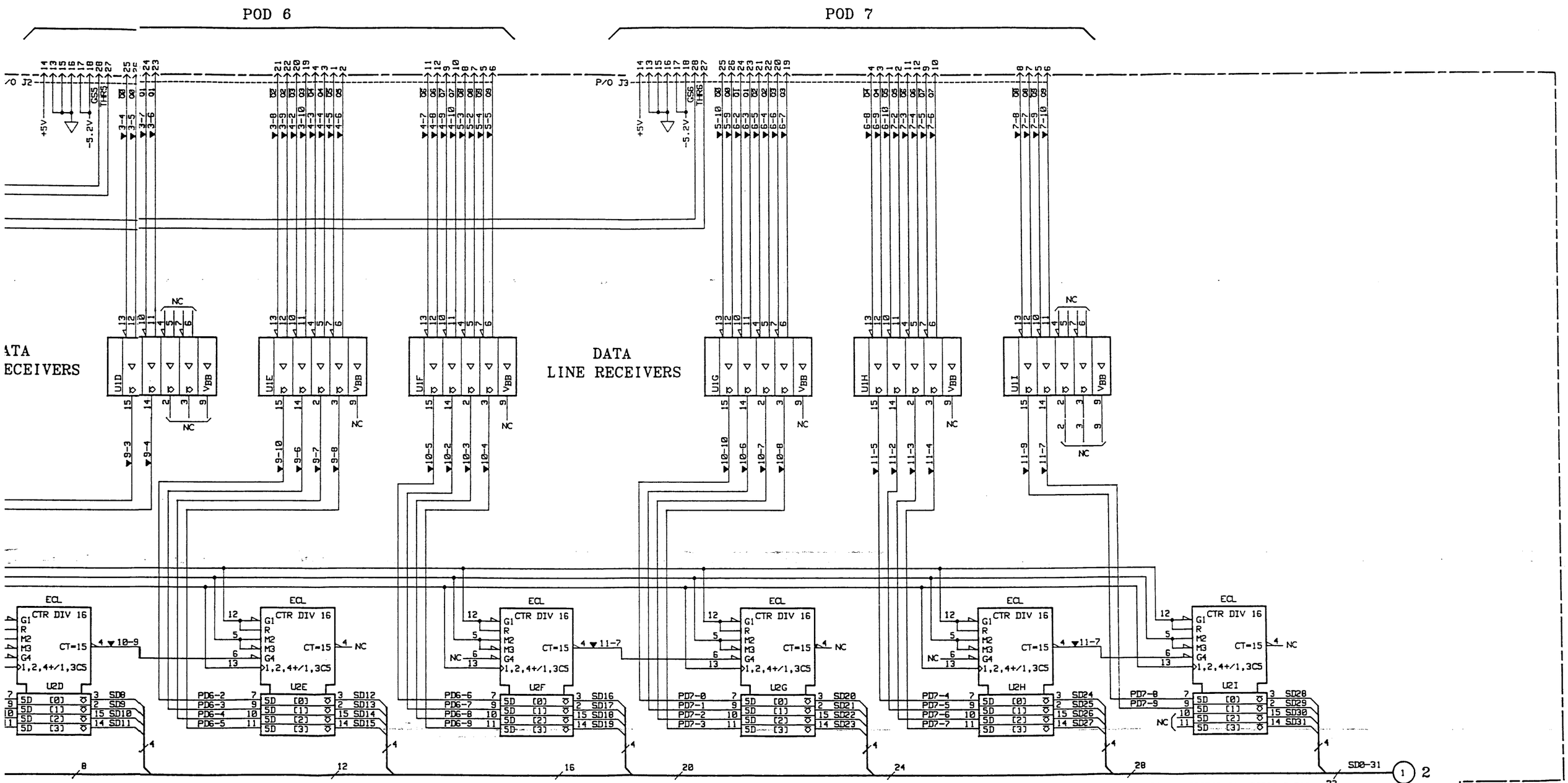
' VALUE TABLE FOR NFORMATION

RESISTOR PACK PACK NUMBER (RP) EING PULLED DOWN ING PULLED UP

R	POWER PIN	VOLTAGE
	1	-5.2V
	1	-2.4V
	1	-2.4V
	1	-5.2V
	1	+5V

SCHEMATIC



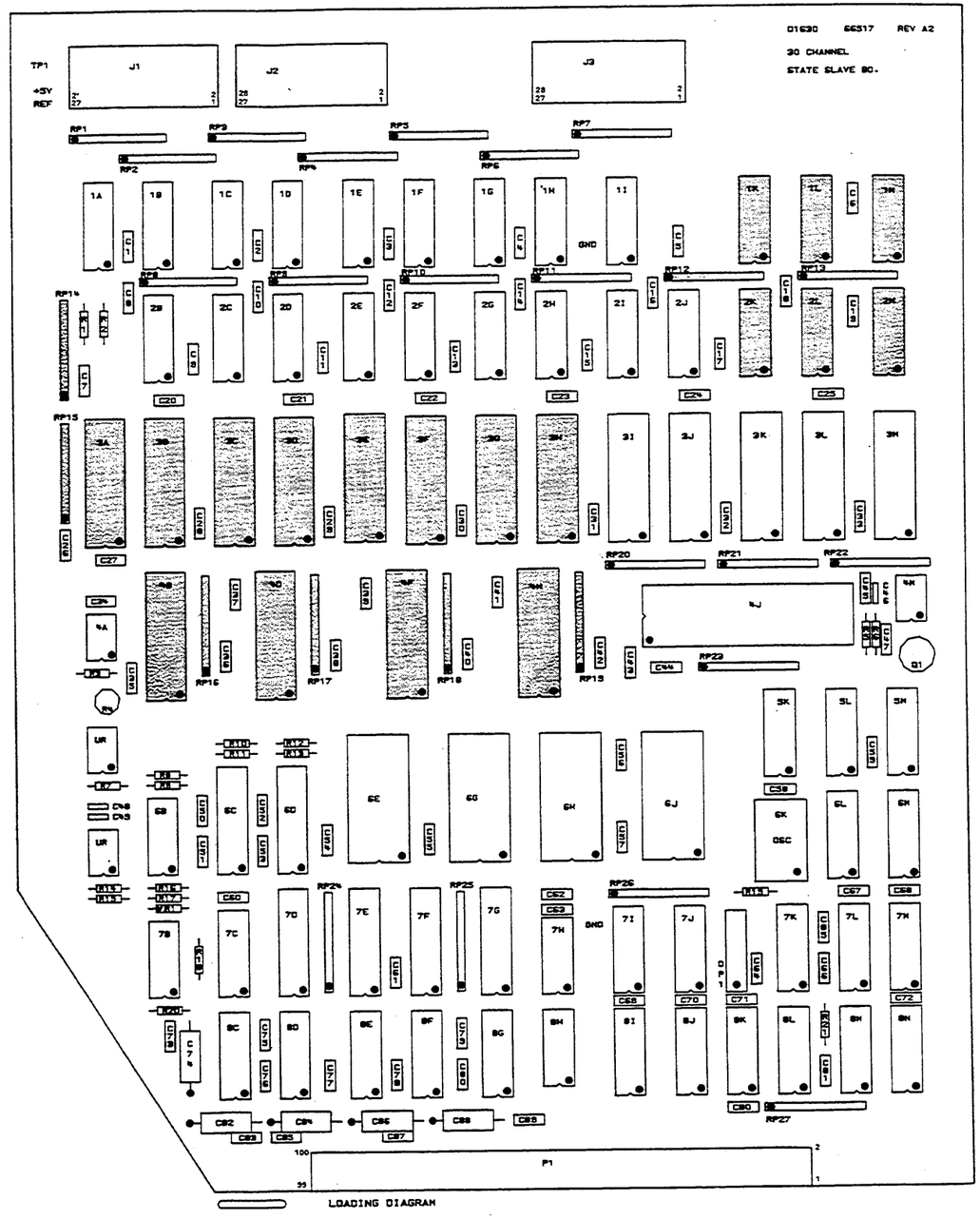


SAMPLE LATCHES (RUN MODE) OR PATTERN PROGRAMMING COUNTERS (HALT MODE)

PULLDOWN RESISTOR CONNECTIONS FOR U2B THROUGH U2I ARE SHOWN ON THE FOLLOWING SCHEMATIC.

8F-1

Schematic 8F-1
Data Line Receivers and Sample Latches/Pattern Programming Counters

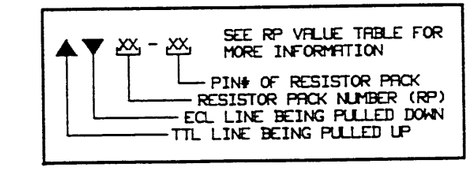


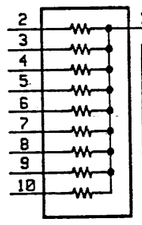
Component Locator for Schematic 8F-2

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:





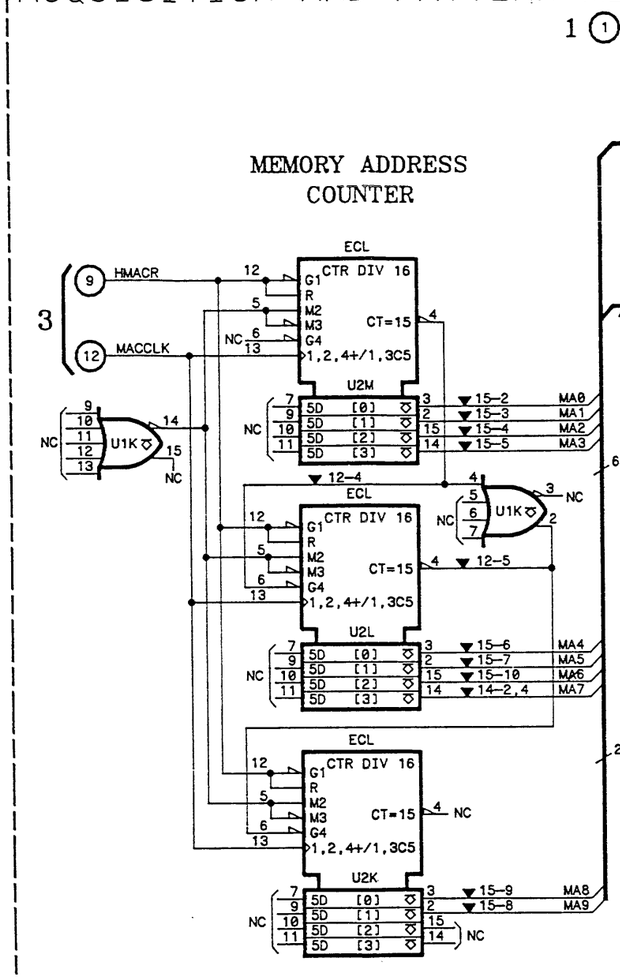
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

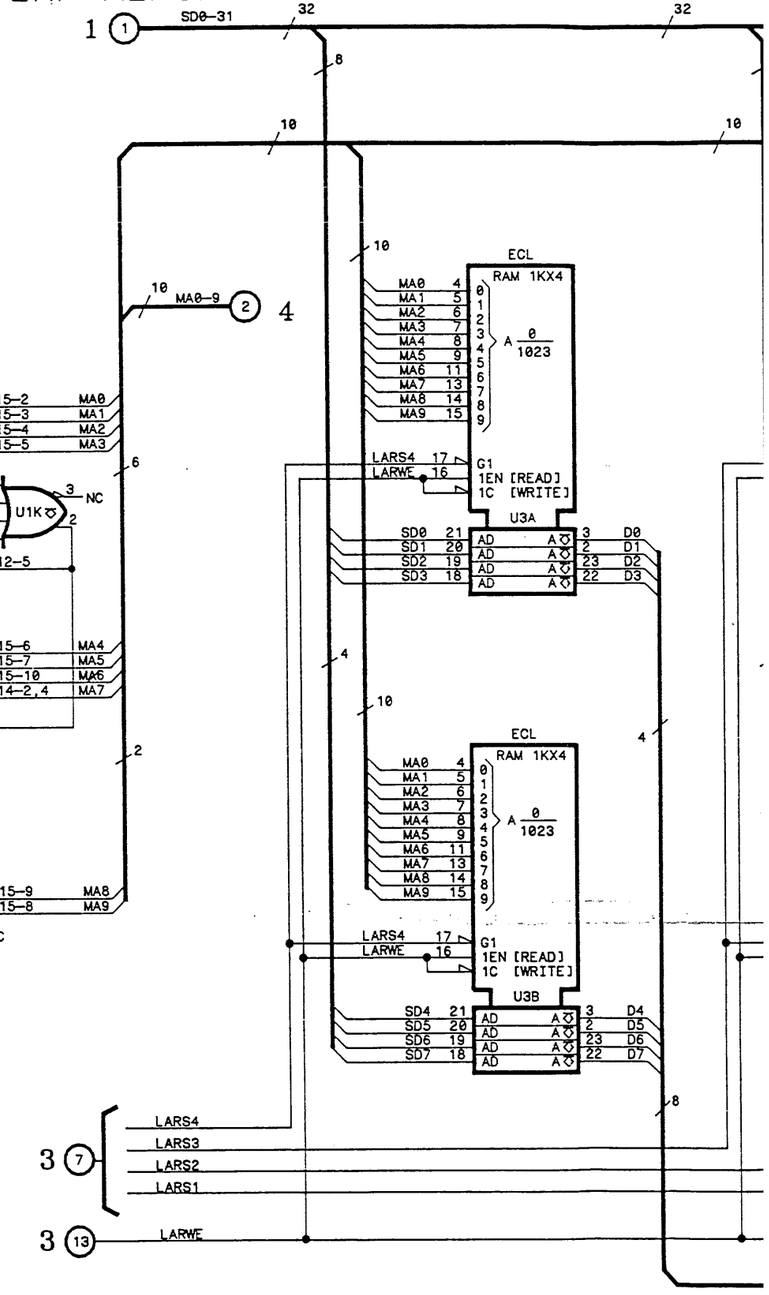
PARTS ON THIS SCHEMATIC

P/O P1 RP12,14,15,16-19 U1K-M,U2K-M,U3A-H, U4B-H	

ACQUISITION AND PATTERN MEMORY

MEMORY ADDRESS COUNTER





CE
ECTIONS

IC GROUP
U1A–I,K–M, U2B–M,U5K–M, U7I,K–M,U8I–N
U3A–M U4B,D,F,H
U6E,G,H,I
U6L,M U8C–G
U7C
U7D–G
U7H U8H
U7J

SCRIPTIONS:

VALUE TABLE FOR
NFORMATION

RESISTOR PACK
PACK NUMBER (RP)
EING PULLED DOWN
ING PULLED UP

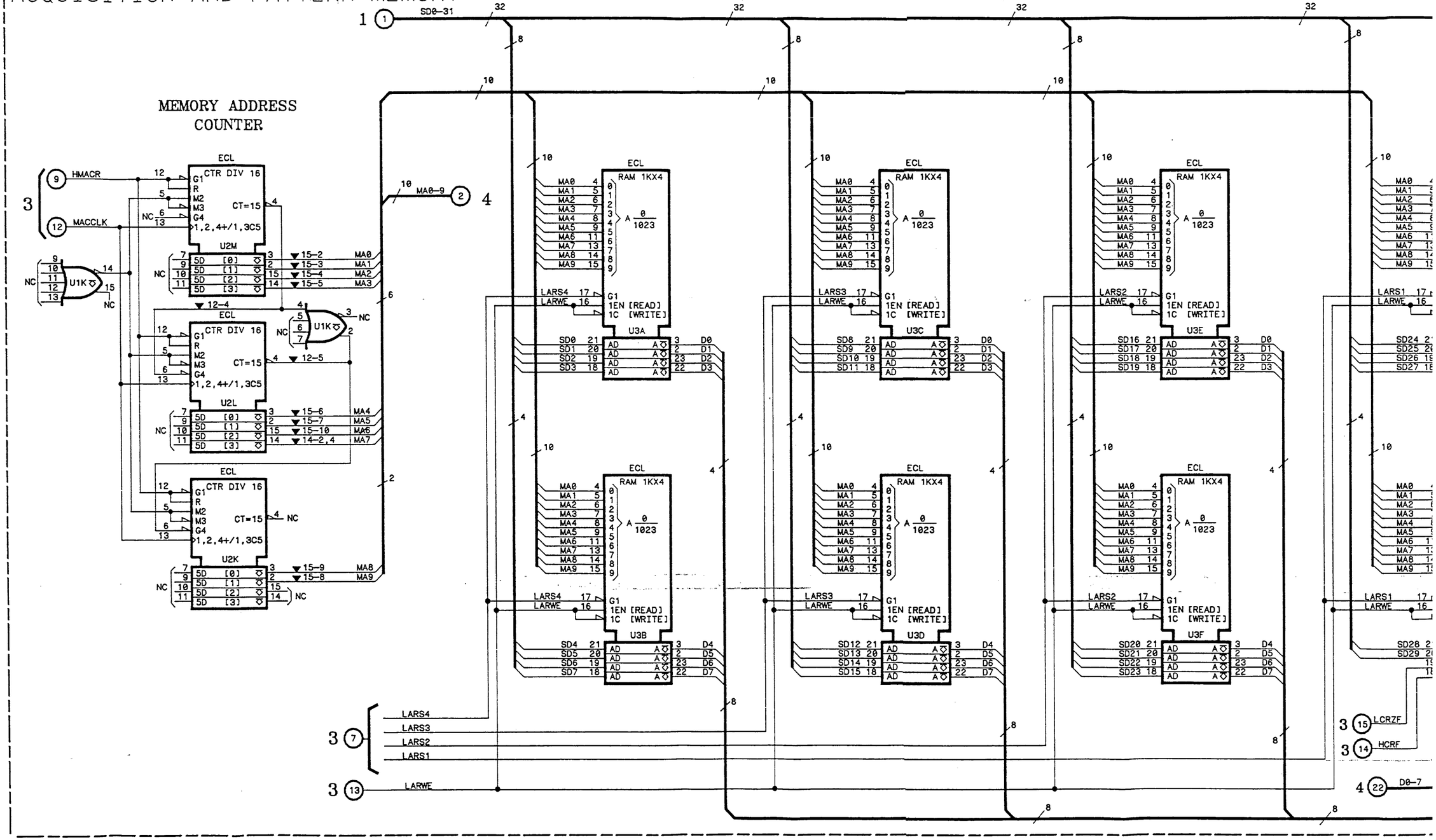
OR	POWER PIN	VOLTAGE
	1	-5.2V
	1	-2.4V
	1	-2.4V
	1	-5.2V
5	1	+5V

SCHEMATIC

ACQUISITION AND PATTERN MEMORY

MEMORY ADDRESS COUNTER

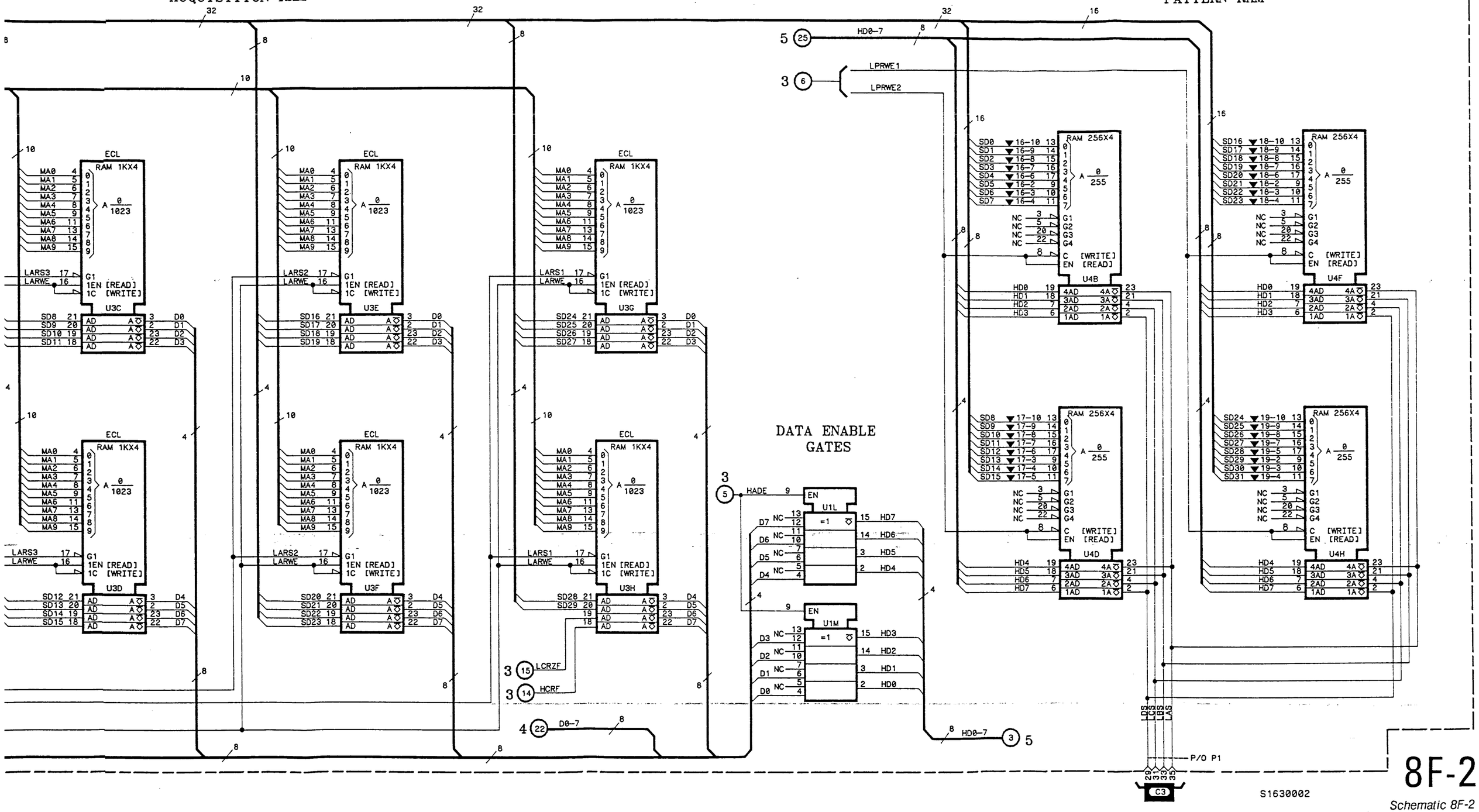
ACQUISITION RAM



ACQUISITION RAM

PATTERN RAM

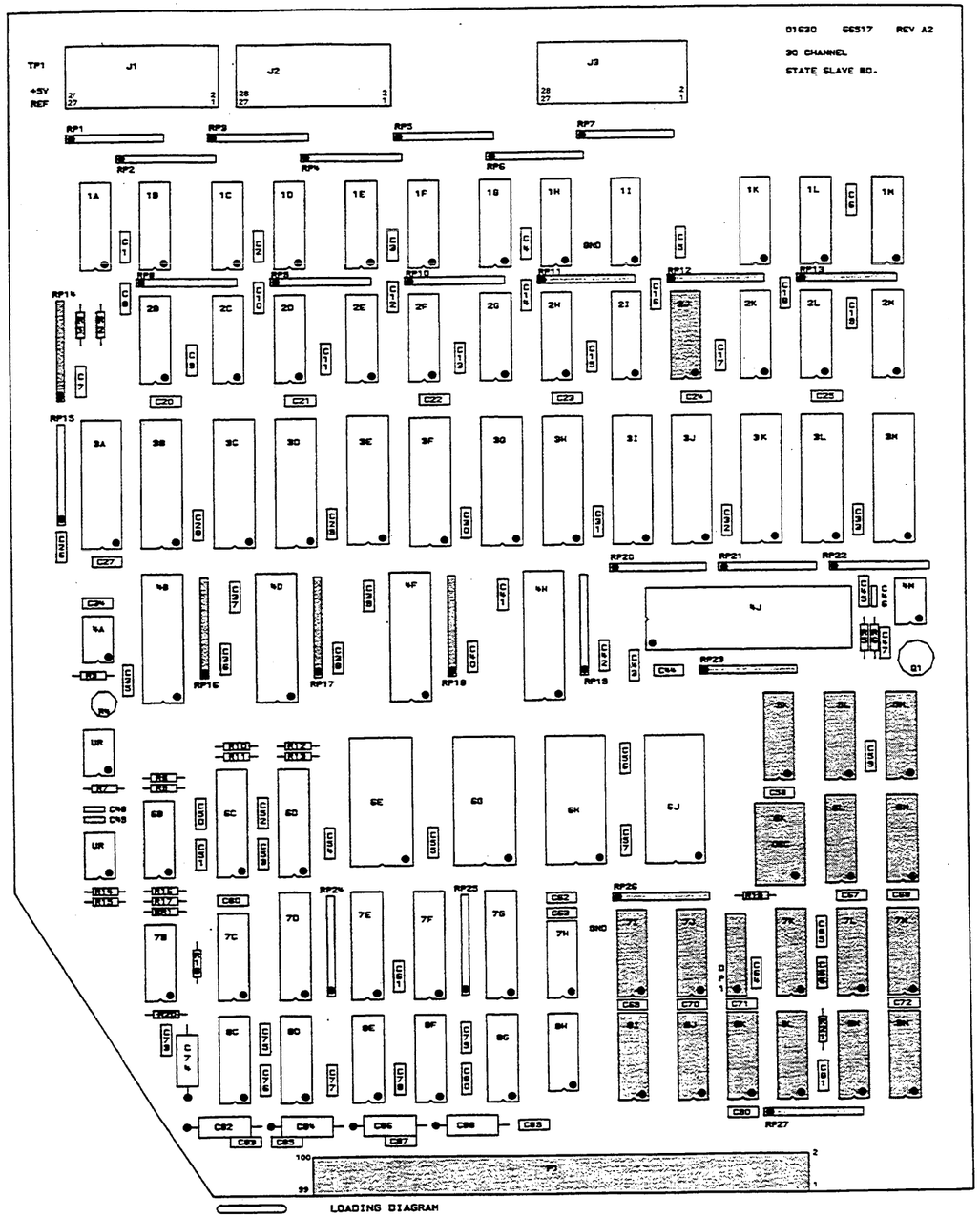
DATA ENABLE GATES



S1630002

8F-2

Schematic 8F-2
Memory Address Counter and RAM
8F-13

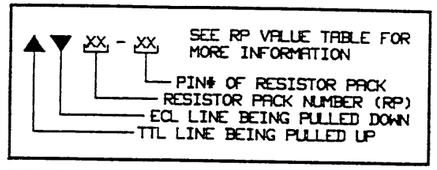


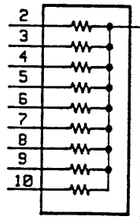
Component Locator for Schematic 8F-3

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U5E,G,H,I
+5V -5.2V GND	9 8 16	U5L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:

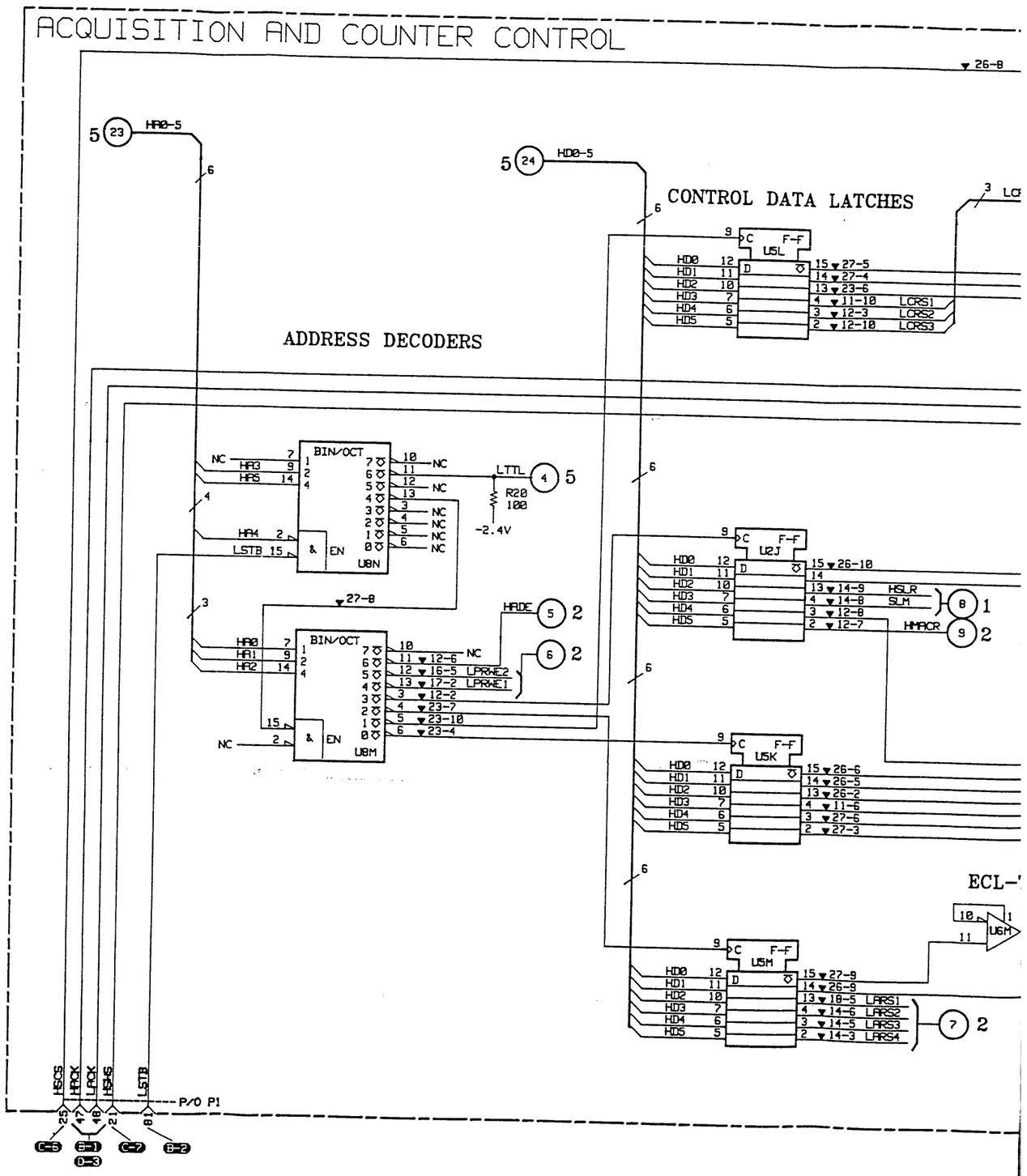




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

C66 P/O P1 R1,2,19-21 RP11-14,16-18,23, 26,27 U2J,5K-M,6K-M, 7I-M,8I-M	



/ICE NECTIONS

IO.	IC GROUP
	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
	U3A-M U4B,D,F,H
	U6E,G,H,I
	U6L,M U8C-G
	U7C
	U7D-G
	U7H U8H
	U7J

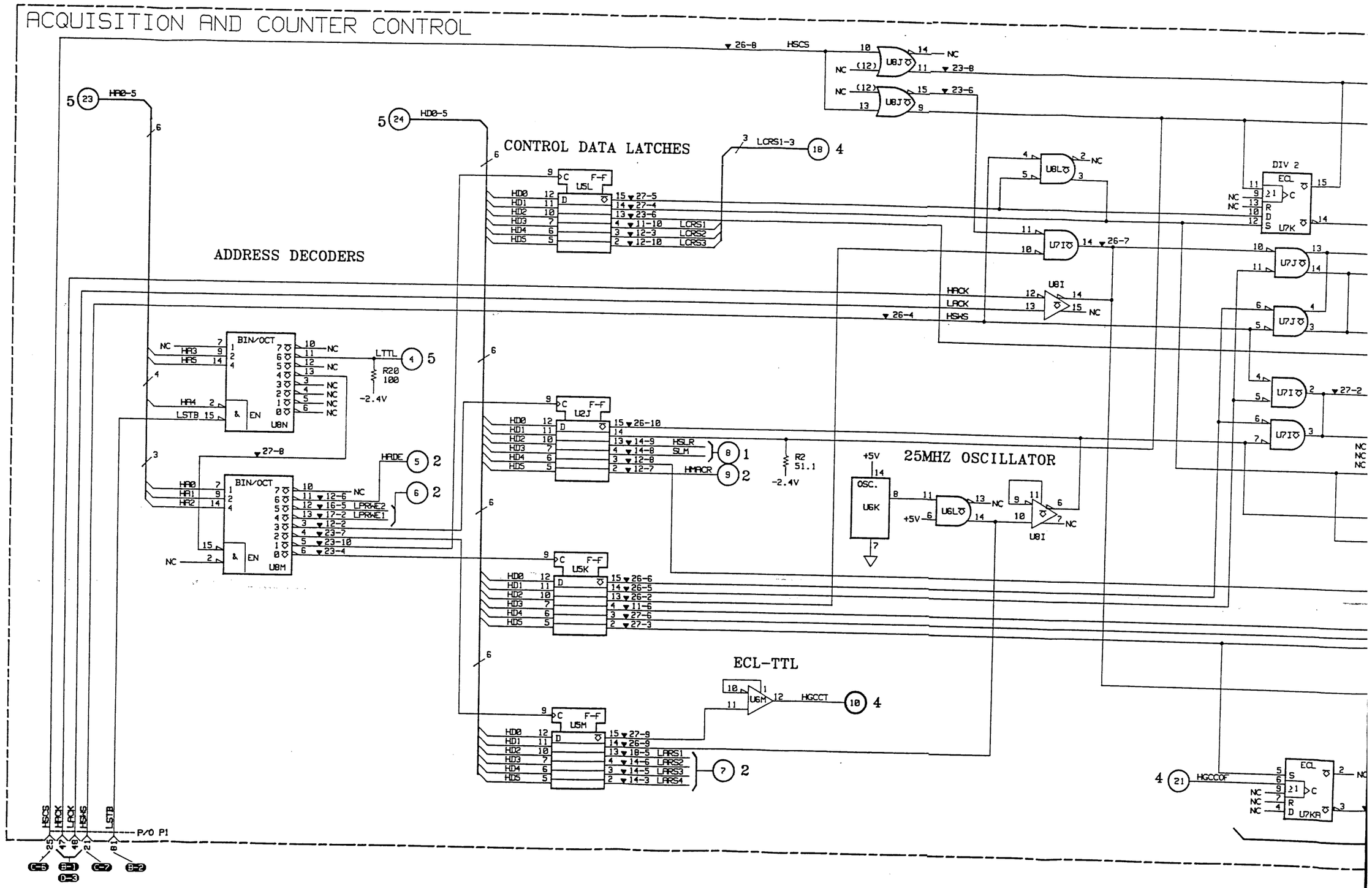
ESCRIPTIONS:

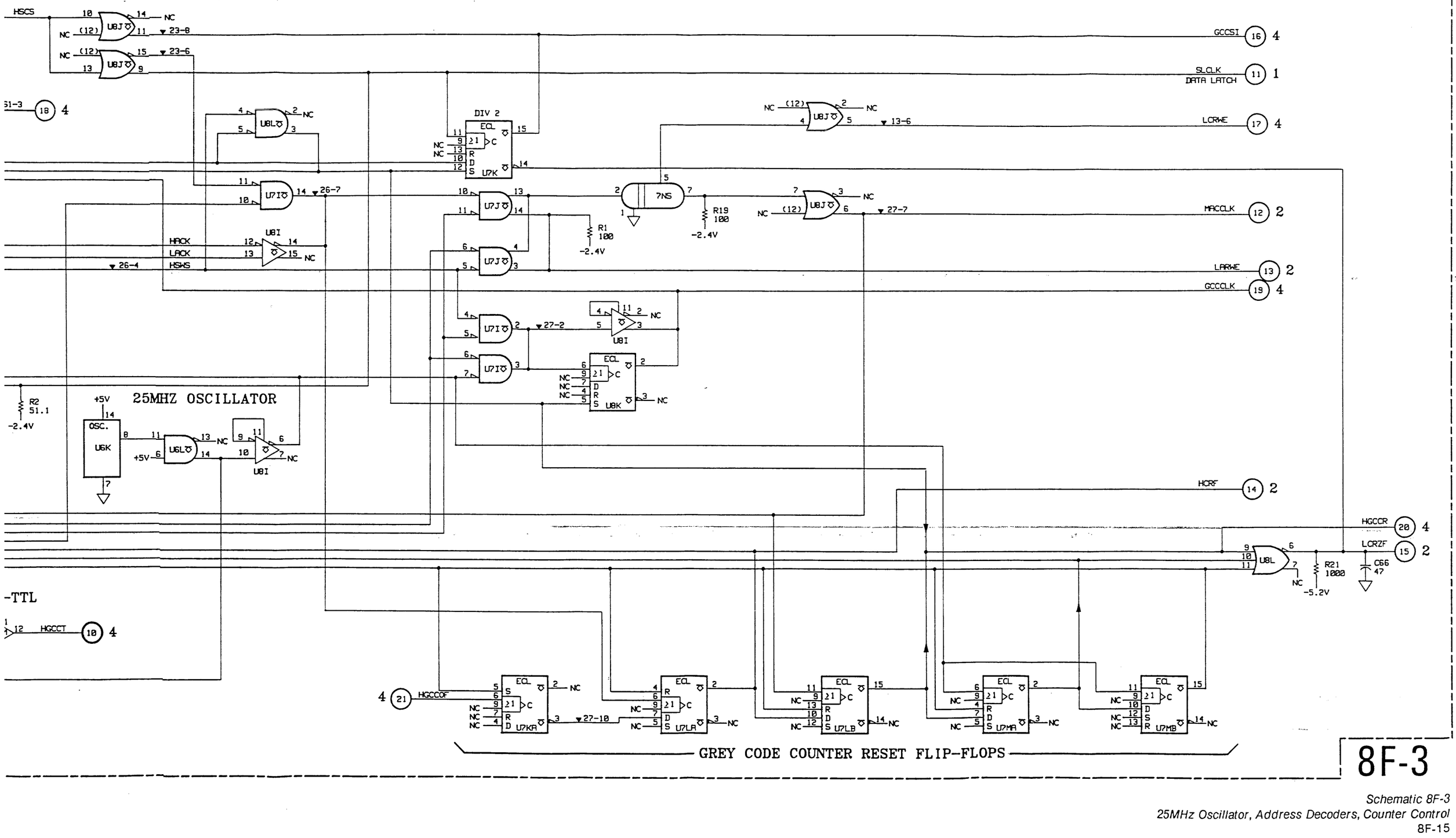
P VALUE TABLE FOR INFORMATION

RESISTOR PACK
PACK NUMBER (RP)
BEING PULLED DOWN
EING PULLED UP

OR E	POWER PIN	VOLTAGE
	1	-5.2V
	1	-2.4V
	1	-2.4V
	1	-5.2V
9	1	+5V

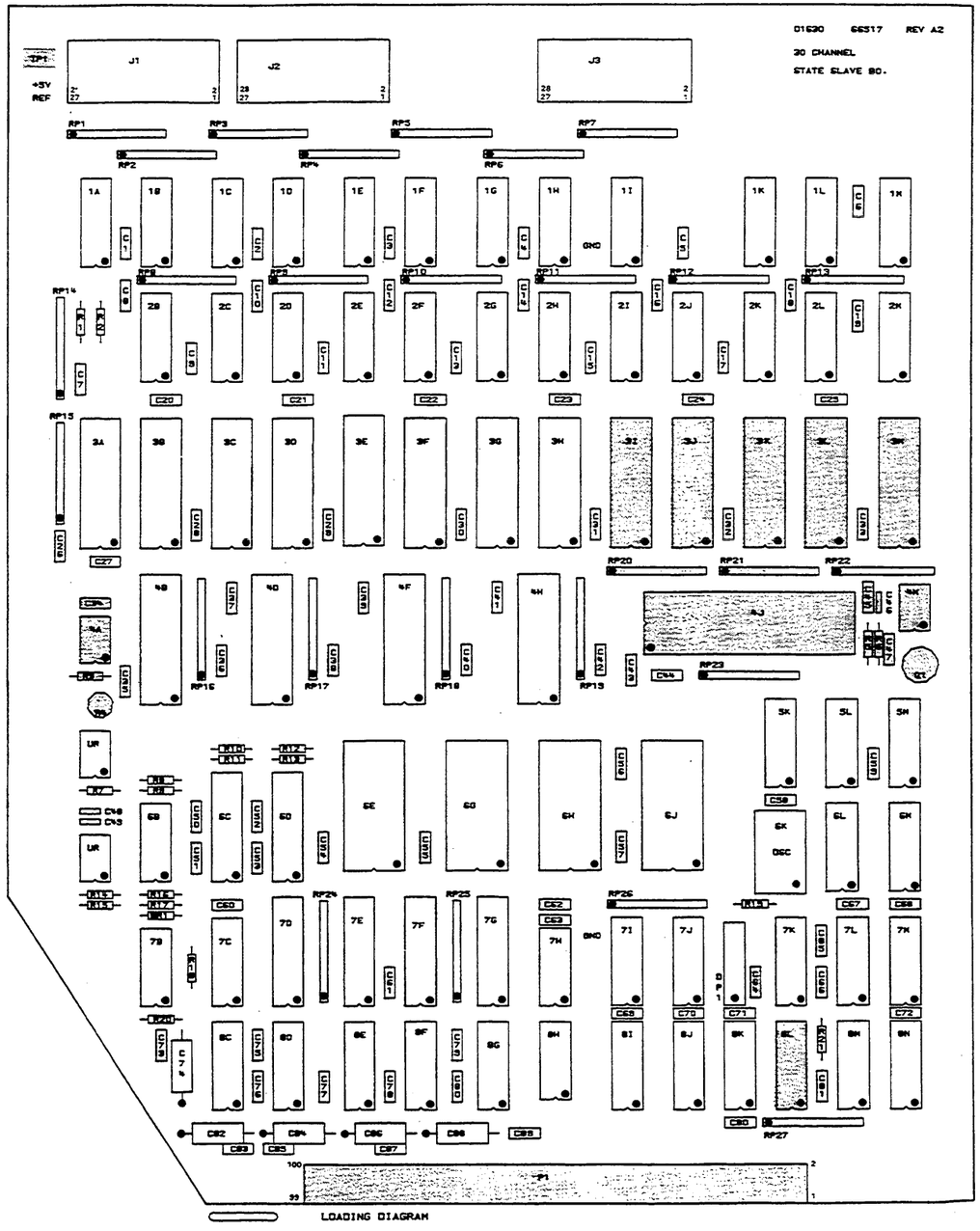
SCHEMATIC





8F-3

Schematic 8F-3
25MHz Oscillator, Address Decoders, Counter Control

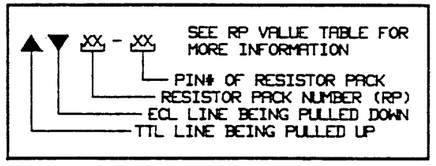


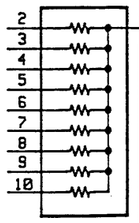
Component Locator for Schematic 8F-4

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:





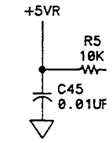
RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

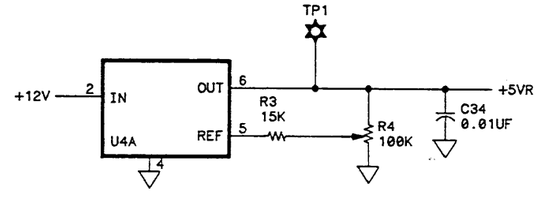
C1-47,54-65,67-90 P/O P1 Q1 R3-6 RP20-22 U3I-3M,4A,4J,4M U8L	

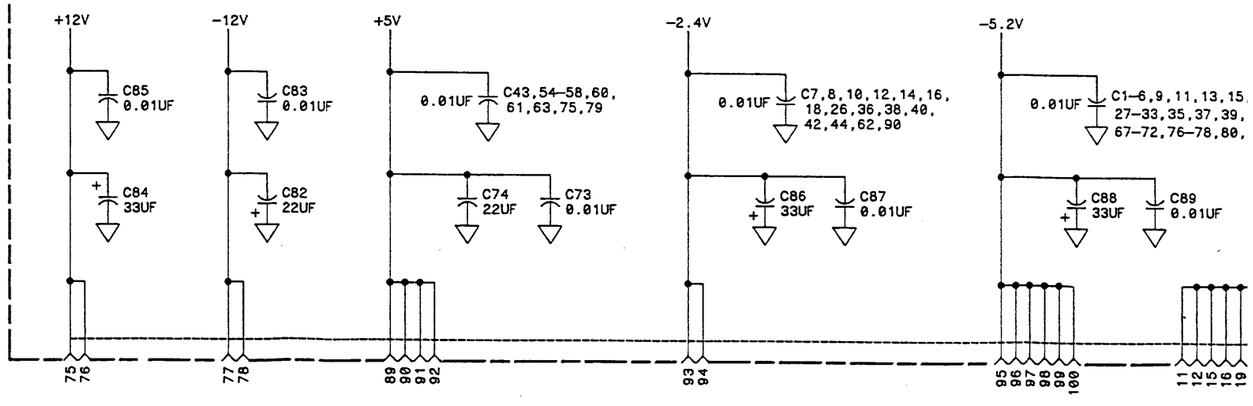
GREY CODE COUNTER AND MEMORY

-3.25 VOLT POWER SUPPLY



+5V REFERENCE SUPPLY





DEVICE CONNECTIONS

PIN NO.	IC GROUP
1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
1 24 12	U3A-M U4B,D,F,H
24 12	U5E,G,H,I
9 8 16	U6L,M U8C-G
8 16	U7C
20 10	U7D-G
14 7	U7H U8H
16 15 1 8	U7J

:K DESCRIPTIONS:

SEE RP VALUE TABLE FOR MORE INFORMATION

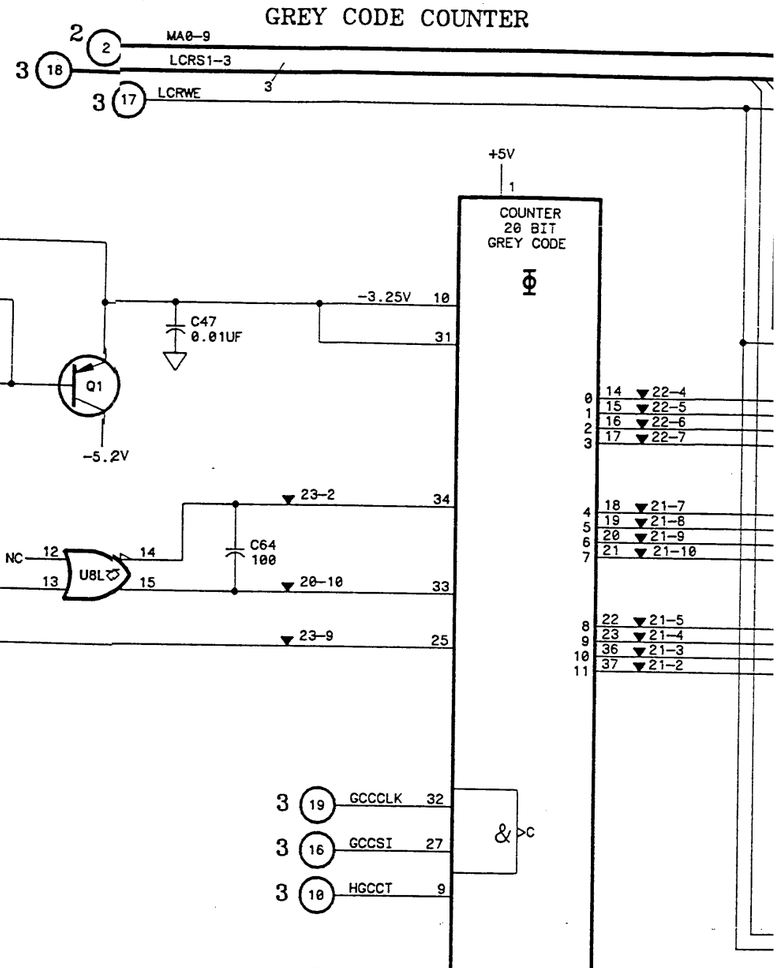
PIN# OF RESISTOR PACK
:SISTOR PACK NUMBER (RP)
LINE BEING PULLED DOWN
-INE BEING PULLED UP

RESISTOR VALUE	POWER PIN	VOLTAGE
330X9	1	-5.2V
100X9	1	-2.4V
50X9	1	-2.4V
1KX9	1	-5.2V
2.2KX9	1	+5V

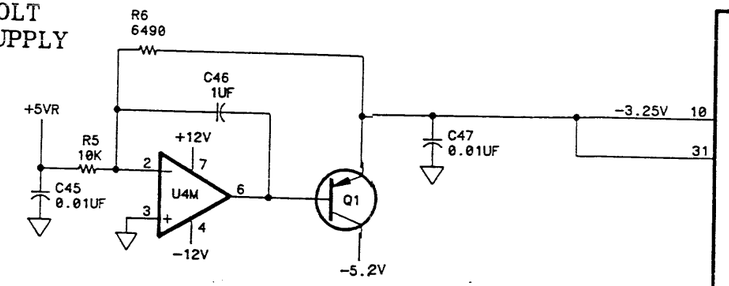
THIS SCHEMATIC

GREY CODE COUNTER AND MEMORY

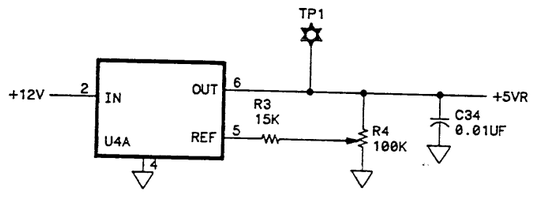
GREY CODE COUNTER

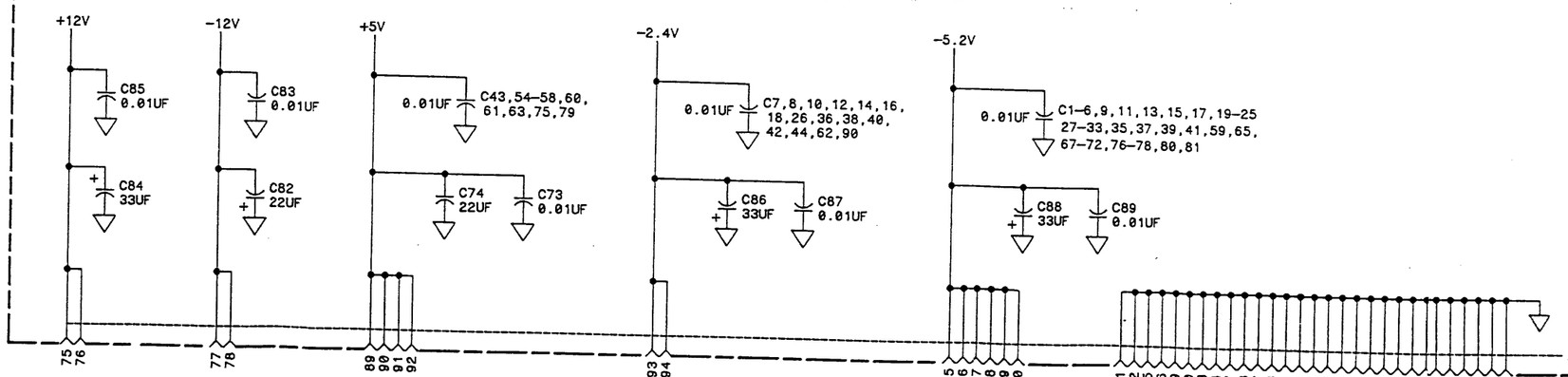


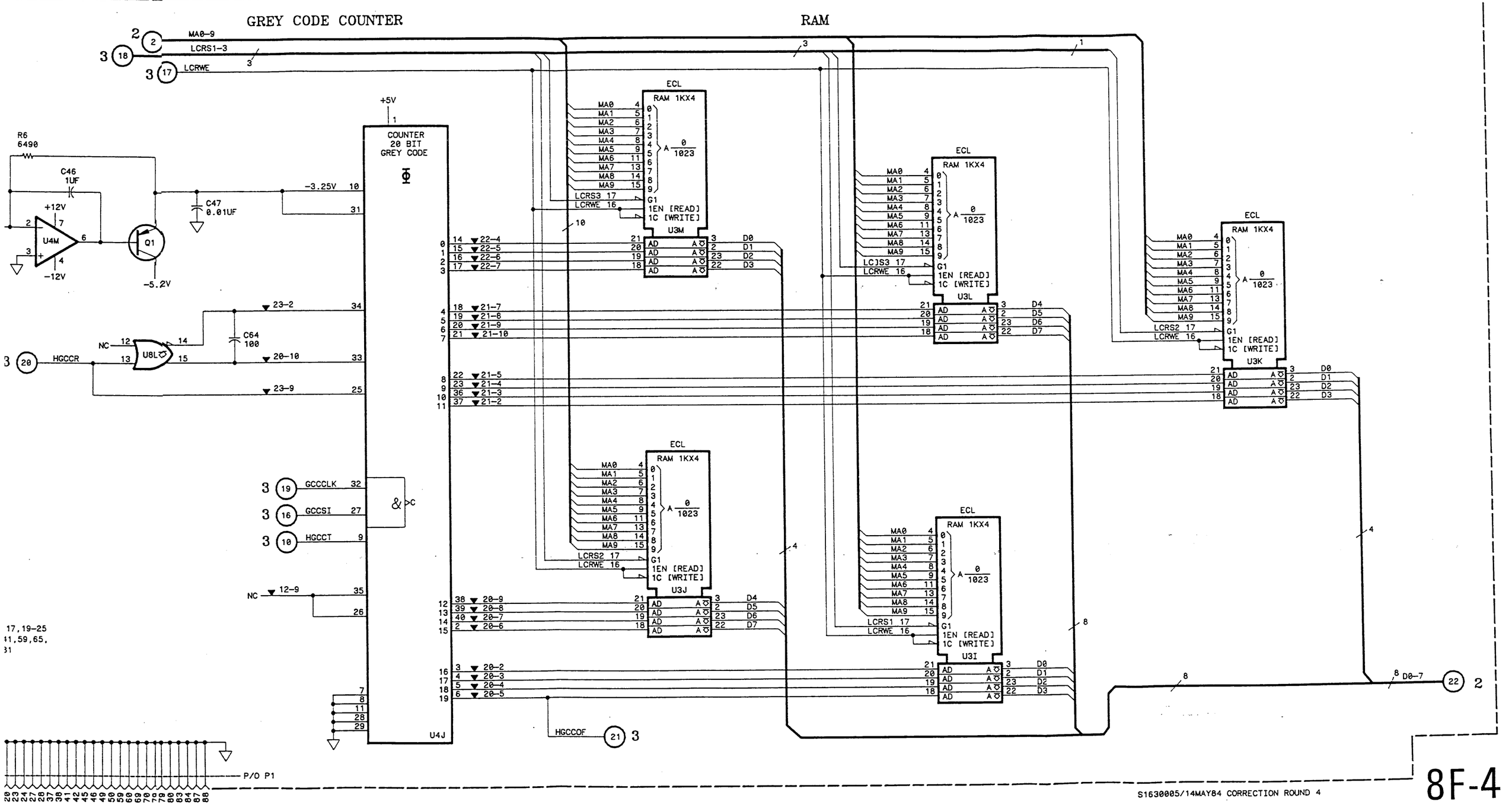
-3.25 VOLT POWER SUPPLY

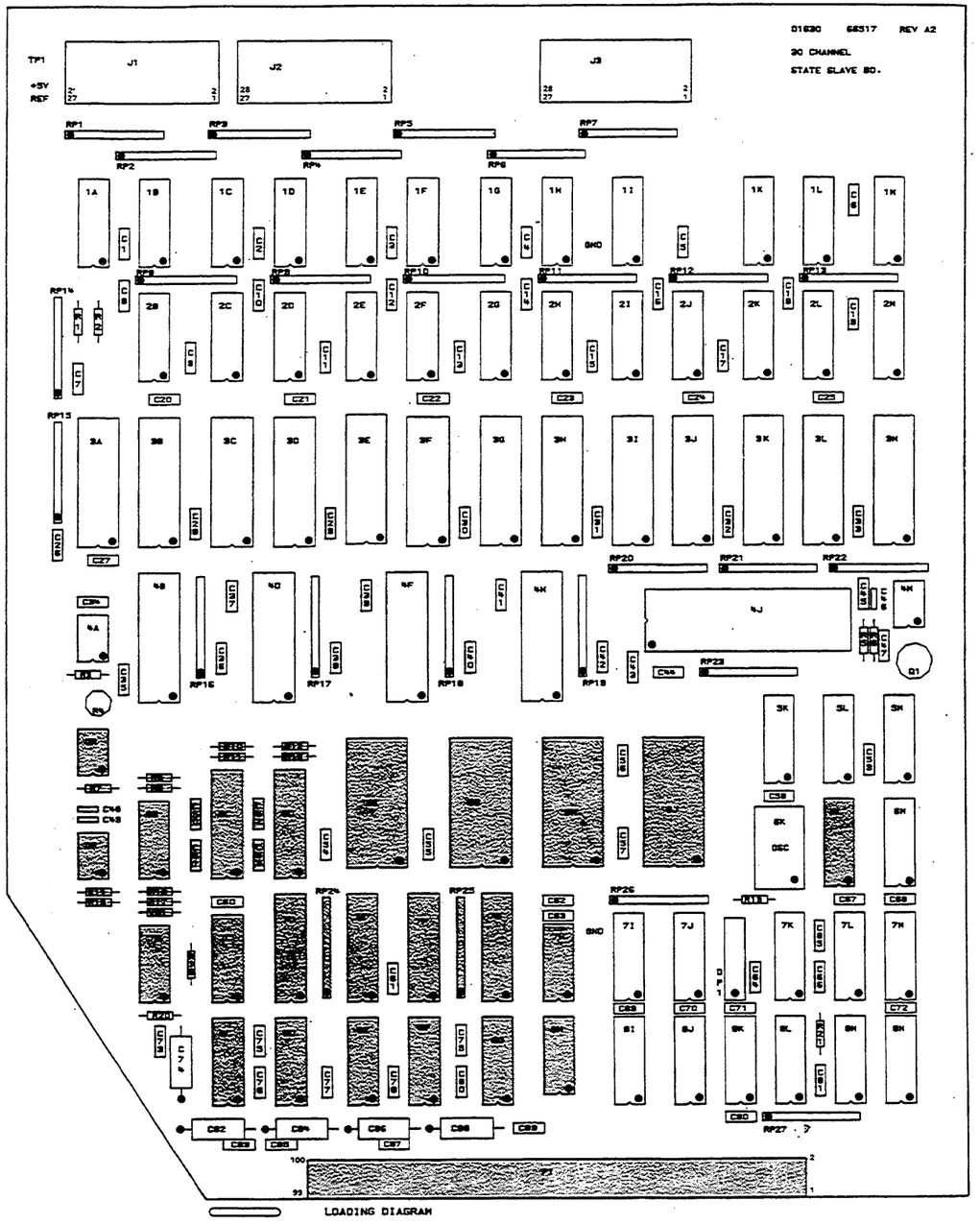


+5V REFERENCE SUPPLY






GREY CODE COUNTER
RAM
MA0-9
LCRS1-3
LCRWE
+5V
COUNTER
20 BIT
GREY CODE
U4J
R6
6490
C46
1UF
C47
0.01UF
C64
100
U4M
U8L
Q1
+12V
-12V
-5.2V
-3.25V
NC
HGCCR
GCCCLK
GCCSI
HGCCT
HGCCOF
P/O P1
ECL
RAM 1KX4
U3M
U3L
U3K
U3J
U3I
LCRS3
LCRS2
LCRS1
LCRWE
1EN [READ]
1C [WRITE]
AD
D0
D1
D2
D3
D4
D5
D6
D7
D0-7
S1630005/14MAY84 CORRECTION ROUND 4

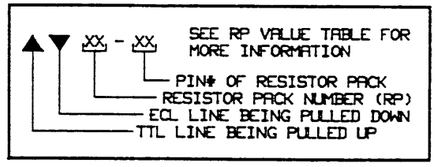


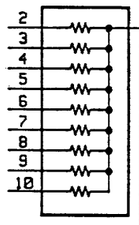
Component Locator for Schematic 8F-5

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
GND GND -5.2V	1 24 12	U3A-M U4B,D,F,H
+5V GND	24 12	U6E,G,H,I
+5V -5.2V GND	9 8 16	U6L,M U8C-G
+5V GND	8 16	U7C
+5V GND	20 10	U7D-G
+5V GND	14 7	U7H U8H
-5.2V -5.2V -5.2V -5.2V GND	16 15 1 8	U7J

RESISTOR PACK DESCRIPTIONS:

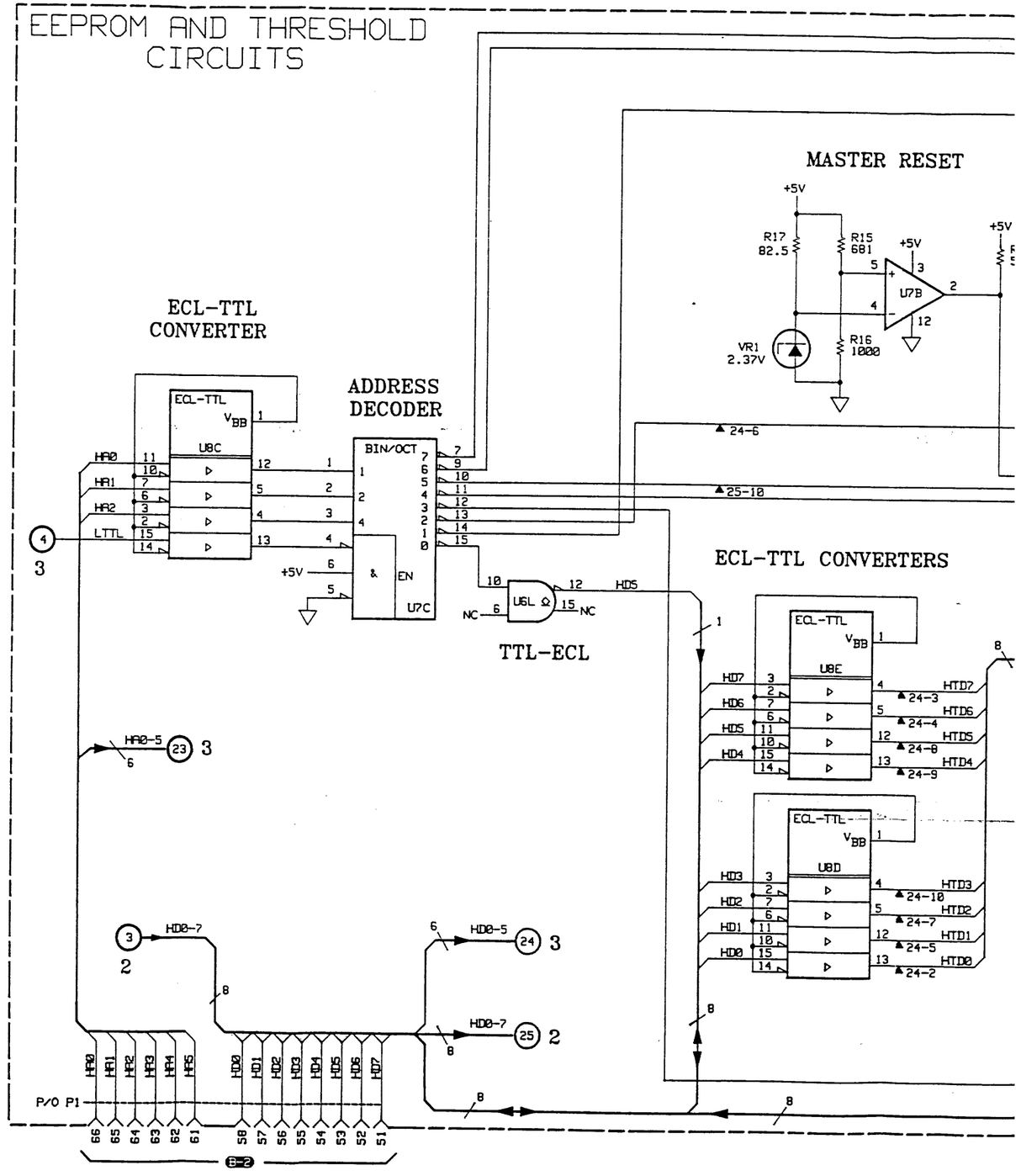




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

PARTS ON THIS SCHEMATIC

C48-53 P/O P1 R7-17 RP24,25 U6B-I,6L,7B-H,8C-H, UR5A,6A VR1	



IC DEVICE
WER CONNECTIONS

	PIN NO.	IC GROUP
	1 16 8	U1A-I,K-M, U2B-M,U5K-M, U7I,K-M,U8I-N
	1 24 12	U3A-M U4B,D,F,H
	24 12	U6E,G,H,I
	9 8 16	U6L,M U8C-G
	8 16	U7C
	20 10	U7D-G
	14 7	U7H U8H
	16 15 1 8	U7J

PACK DESCRIPTIONS:

- XX — SEE RP VALUE TABLE FOR MORE INFORMATION
- PIN# OF RESISTOR PACK
- RESISTOR PACK NUMBER (RP)
- ECL LINE BEING PULLED DOWN
- TTL LINE BEING PULLED UP

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1-7 8-14	330X9	1	-5.2V
16-19 23,26, 27	100X9	1	-2.4V
15	50X9	1	-2.4V
20-22	1KX9	1	-5.2V
24,25	2.2KX9	1	+5V

ON THIS SCHEMATIC

'B-H,8C-H,	

EEPROM AND THRESHOLD CIRCUITS

MASTER RESET

ADDRESS COUNTER

ECL-TTL CONVERTER

ADDRESS DECODER

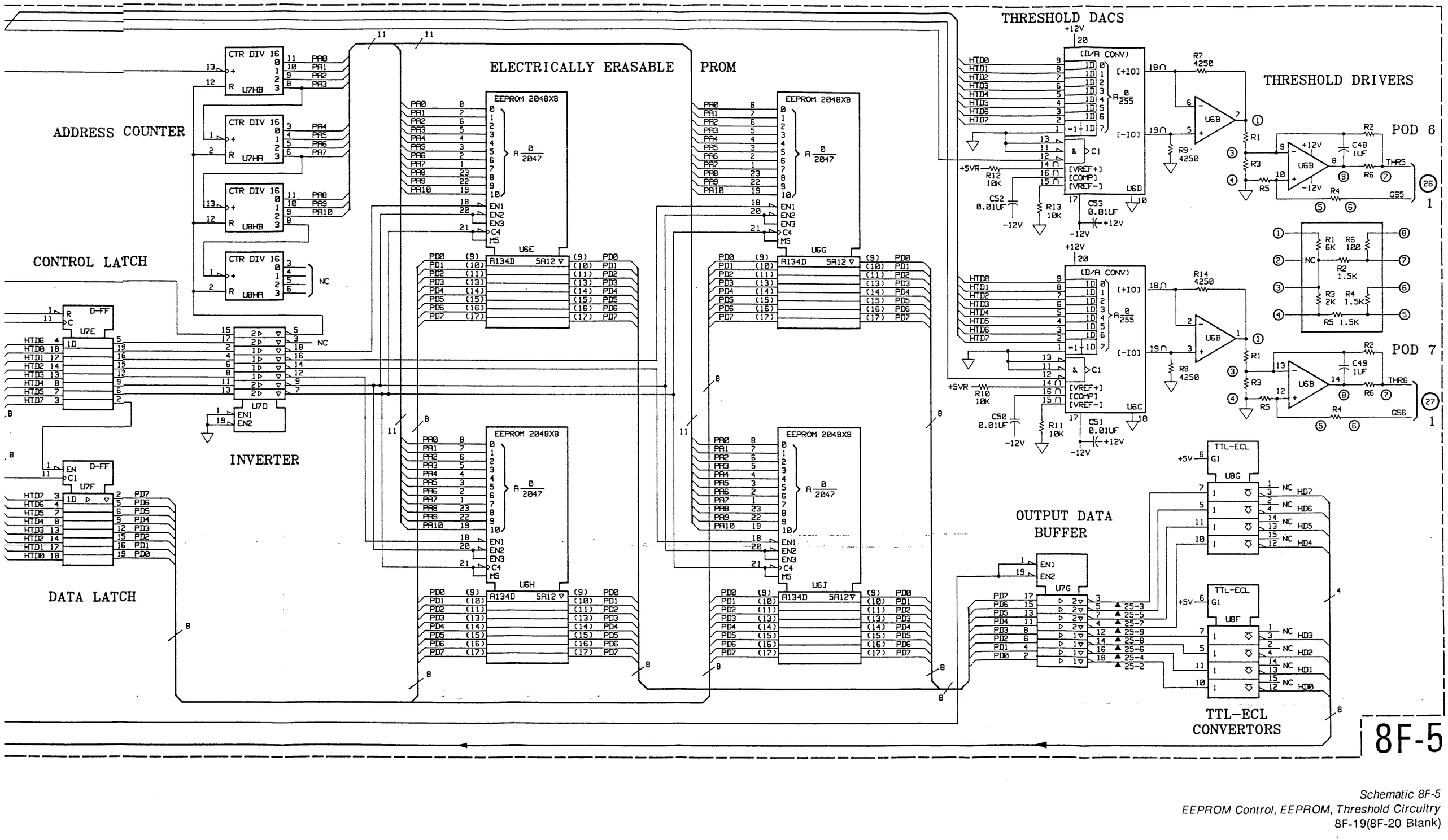
CONTROL LATCH

ECL-TTL CONVERTERS

TTL-ECL

INVERTER

DATA LATCH



Schematic 8F-5
EEPROM Control, EEPROM, Threshold Circuitry
8F-19(8F-20 Blank)

Service Group 8G Table of Contents

Paragraph		Page
8G-1.	Introduction	8G-1
8G-2.	Analog System Block Diagram	8G-1
8G-3.	General.	8G-1
8G-4.	Analog Input.	8G-1
8G-5.	Analog to Digital.	8G-1
8G-6.	Acquisition Memory	8G-1
8G-7.	Digital Control	8G-1
8G-8.	Analog Control	8G-2
8G-9.	Operating Routine.	8G-2
8G-10.	Loading	8G-2
8G-11.	Acquisition Sequence	8G-4
8G-12.	Theory of Operation	8G-5
8G-13.	Analog Input	8G-5
8G-14.	General	8G-5
8G-15.	Impedance Converters	8G-5
8G-16.	Gain Hybrid	8G-5
8G-17.	Gain Control	8G-6
8G-18.	Output Circuitry	8G-6
8G-19.	Channel Amplifiers	8G-8
8G-20.	Internal Trigger Circuitry	8G-9
8G-21.	External Trigger Circuitry	8G-9
8G-22.	Trigger Multiplexer	8G-9
8G-23.	Auto-Calibration Routine	8G-9
8G-24.	Gain, Vernier, and Offset Calibration	8G-10
8G-25.	Trigger Level Calibration	8G-10
8G-26.	Analog to Digital	8G-11
8G-27.	General	8G-11
8G-28.	Analog to Digital Converters	8G-11
8G-29.	Trigger Initiation	8G-11
8G-30.	Sample Clocking	8G-12
8G-31.	Clock Signals	8G-12
8G-32.	Trigger Synchronizer	8G-12
8G-33.	Trigger Identification	8G-12
8G-34.	Synchronous Stop	8G-12
8G-35.	Measurement Complete	8G-12
8G-36.	BNC Output	8G-12
8G-37.	Acquisition Memory	8G-13
8G-38.	General	8G-13
8G-39.	Write Sequence	8G-13
8G-40.	Read Sequence	8G-13
8G-41.	Digital Control	8G-14
8G-42.	General	8G-14

Service Group 8G Table of Contents (Cont'd)

Paragraph		Page
8G-43.	Control Latch	8G-14
8G-44.	Block Select	8G-14
8G-45.	Counters	8G-15
8G-46.	Delay Counter	8G-15
8G-47.	Memory Address Counter	8G-15
8G-48.	Poststore Counter	8G-15
8G-49.	Arming Logic	8G-15
8G-50.	Prestore Valid/Memory Full	8G-16
8G-51.	Output Data Selectors	8G-16
8G-52.	Analog Control	8G-16
8G-53.	General	8G-16
8G-54.	Analog Gain Select	8G-16
8G-55.	Channel Vernier DACs	8G-17
8G-56.	Internal Trigger Level DAC	8G-18
8G-57.	Offset DACs	8G-18
8G-58.	Mnemonics	8G-18

List of Illustrations

Figure		Page
8G-1.	Analog System Block Diagram	8G-3
8G-2.	Acquisition Sequence Diagram	8G-4
8G-3.	Hybrid Output Circuit	8G-7
8G-4.	Channel Amplifier	8G-8
8G-5.	Acquisition Memory Write Timing Diagram	8G-13
8G-6.	Acquisition Memory Read Timing Diagram	8G-14
8G-7.	Channel Vernier Control Circuit	8G-17

List of Tables

Table		Page
8G-1.	Gain Control vs. Full-scale Deflections	8G-6
8G-2.	Gain Vernier Current Relationships	8G-17
8G-3.	Mnemonics	8G-18

List of Schematics

Schematic		Page
8G-1.	Analog Input, Gain Hybrid, Trigger Select	8G-23
8G-2.	ADC Clocking, ADC, Measurement Complete	8G-25
8G-3.	Acquisition Memory	8G-27
8G-4.	Digital Control, Counter Chains	8G-29
8G-5.	Analog Control, DACs	8G-31

SERVICE GROUP 8G
ANALOG

8G-1. INTRODUCTION

The analog board supplies two channels of digitized analog waveform. The analog board can be set up as slave, where it stores data after arming by the state or timing boards, or it can be master, where it supplies the arming signal for the rest of the system. Analog input and timing parameters are set by the system CPU which uses data keyed into the instrument through the analog menus.

8G-2. ANALOG SYSTEM BLOCK DIAGRAM

8G-3. General.

The Analog System has been divided into five sections, each of which corresponds to a separate service sheet. The block diagram is also divided so that the five sections are apparent. Use the block diagram, figure 8G-1, along with the following descriptions.

8G-4. ANALOG INPUT. The Analog Input accepts three analog signals, two waveform channels and an external trigger. The analog inputs are impedance converted and have their amplitude and offset adjusted to fit the input requirements of the Analog to Digital Converters, 0 to -1.25V. Trigger signals from the channels can also be selected. The selected internal trigger is level shifted for the desired trigger level and opposite phases of ECL signal are provided to the trigger multiplexer. The external trigger is impedance converted and processed into two ECL level signals of opposite phase. One of the two phases of the selected internal trigger or one of the two phases of the external trigger are selected by the trigger multiplexer. The positive edge of the signal from the trigger multiplexer corresponds to the desired trigger.

8G-5. ANALOG TO DIGITAL. The Analog to Digital section takes samples of the channel signals and digitizes them for the Acquisition Memory. The sample clock is provided on the system bus. The maximum sample rate is 200 megasamples per second.

The clocking circuitry provides clock and clock enables for the ADCs. The Synchronous Stop circuit halts clocking in a known state at the end of the acquisition period. Measurement Complete controls a system line to indicate analog status to the rest of the analyzer. The Trigger Logic qualifies the selected analog trigger. The Trigger ID tells the CPU between which samples trigger occurred. The synchronizer synchronizes the qualified trigger to the sample clock.

8G-6. ACQUISITION MEMORY. The Acquisition Memory stores the analog waveform data. Data is stored in frames of four samples each in a 24 X 256 RAM array. Data from both channel ADCs is stored simultaneously. Block selects enable parts of memory for reading by the CPU. Data from RAM is enabled onto the CPU data bus through the data selector multiplexers.

8G-7. DIGITAL CONTROL. The Digital Control provides control signals decoded from the system bus and strobe lines. It also includes the counter chains which control data storage.

The Delay Counter counts the delay time between trigger and the tracepoint, the Start, Center or End of trace as defined in the menus. It also counts any prestore requirement necessary to ensure full memory. It counts at the frame rate. The Tracepoint Latch enables the Poststore Counter and provides the arming signal if analog is the system master. The Poststore Counter counts at $1/16^{th}$ the frame rate. It counts the events necessary to fill memory from the time of tracepoint. The Memory Address Counter also counts at the frame rate. All counters can be clocked and loaded by the CPU for setup for a run and for self testing.

8G-8. ANALOG CONTROL. The Analog Control provides control primarily for the Analog Input circuitry. It controls the analog gain and offsets, trigger selection, trigger level, and provides a calibration signal for the internal calibration routine. The calibration routine is done any time a change is made in the Analog Format Specifications in the analog menus.

8G-9. Operating Routine

8G-10. LOADING. Before a run the analog system is calibrated and loaded depending on information keyed into the analog menus. The calibration routine is covered in the theory of operation of the Analog Input in this section. The following sequence is used to initialize the analog system.

1. Turn sample clock off (HACK/LACK).
2. Enable write to TTL devices
3. Reset
4. Set Control Latch 1 (schematic 8G-5) to desired settings.
5. Set Control Latch 3 (schematic 8G-5) to desired settings.
6. Load all DACs (schematic 8G-5). (Data was obtained and stored during the calibration routine.)
7. Load Delay Counter, upper and lower sections (schematic 8G-4).
8. Load Poststore Counter (schematic 8G-4).
9. Load Memory Address Counter (schematic 8G-4).
10. Set Control Latch 2 (schematic 8G-4).
11. Configure Sample Clock Rate.

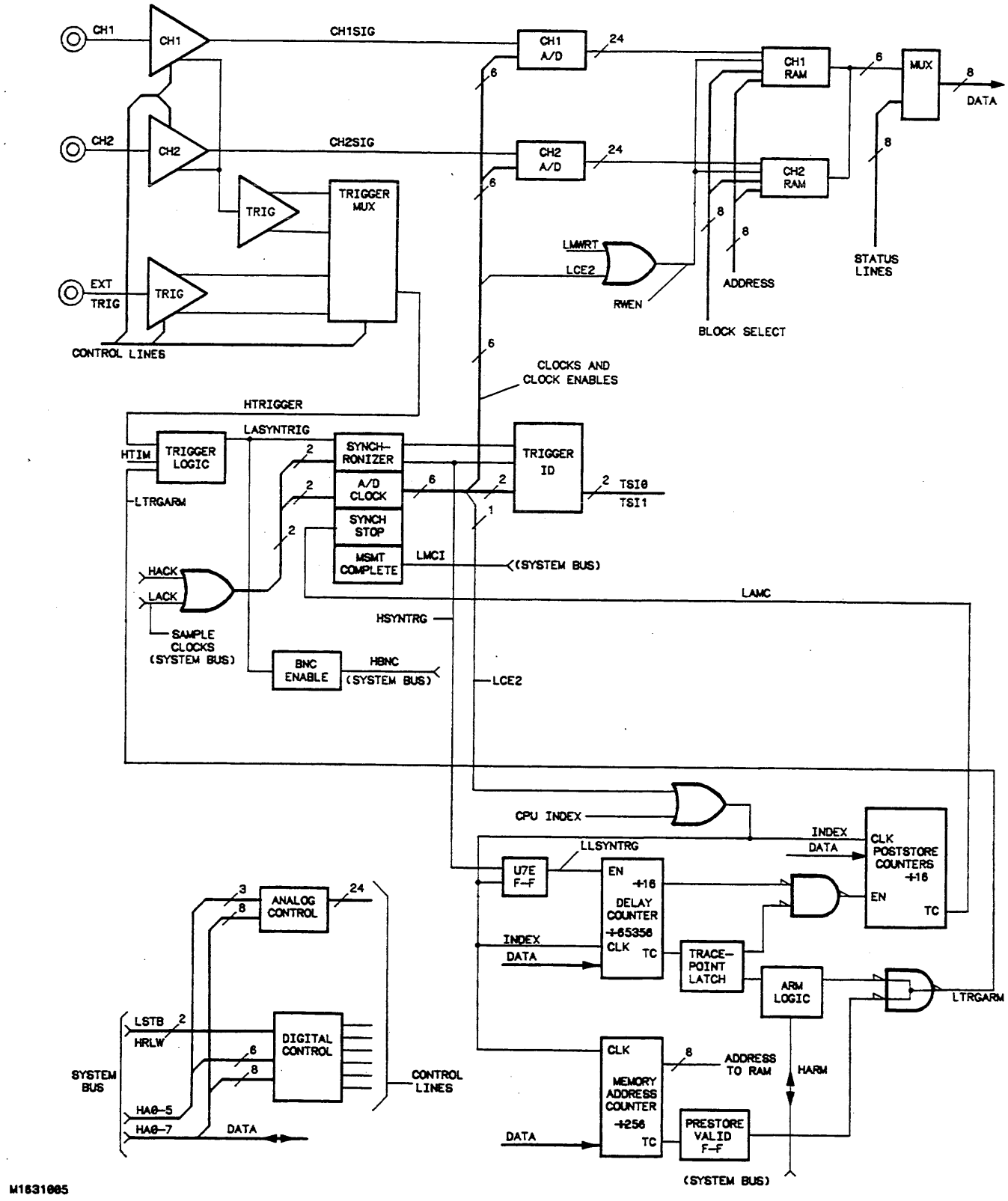


Figure 8G-1. Analog System Block Diagram.

8G-11. ACQUISITION SEQUENCE. The following sequence of steps occurs once the run is initiated. Refer to figure 8G-2 for supplementary information.

1. Sample Clock (HACK/LACK) is started.

   ADC is running.

   Memory Address Counter is running and any prestore requirement is being counted out. Waveform data is being stored.

2. Analyzer system arms. If Analog is master, analyzer system arms when prestore requirement is met. If another acquisition system is master, analog arms when master arms the system and the prestore requirement is met.

3. Analog system triggers.

   Trigger sample is identified and Delay Counter starts.

   If the trigger immediate mode is selected, trigger occurs when prestore and arming requirements are met. If an analog trigger is required, its occurrence triggers the analog system.

4. Delay Counter reaches terminal count, Tracepoint is reached.

   Tracepoint is latched and Poststore Counter starts counting.

   If Analog is master the rest of the analyzer system is armed.

5. Poststore Counter reaches terminal count. The entire analog data acquisition is complete.

   The terminal count of the Poststore Counter initiates the synchronous stop of the ADC Clocking.

   Once ADC clocking stops all acquisition counting stops. The MAC points to the newest frame in memory.

   The Measurement Complete circuit allows the LMCI line low (it may still be held high by one of the other acquisition systems).

6. The system CPU can begin post-processing.

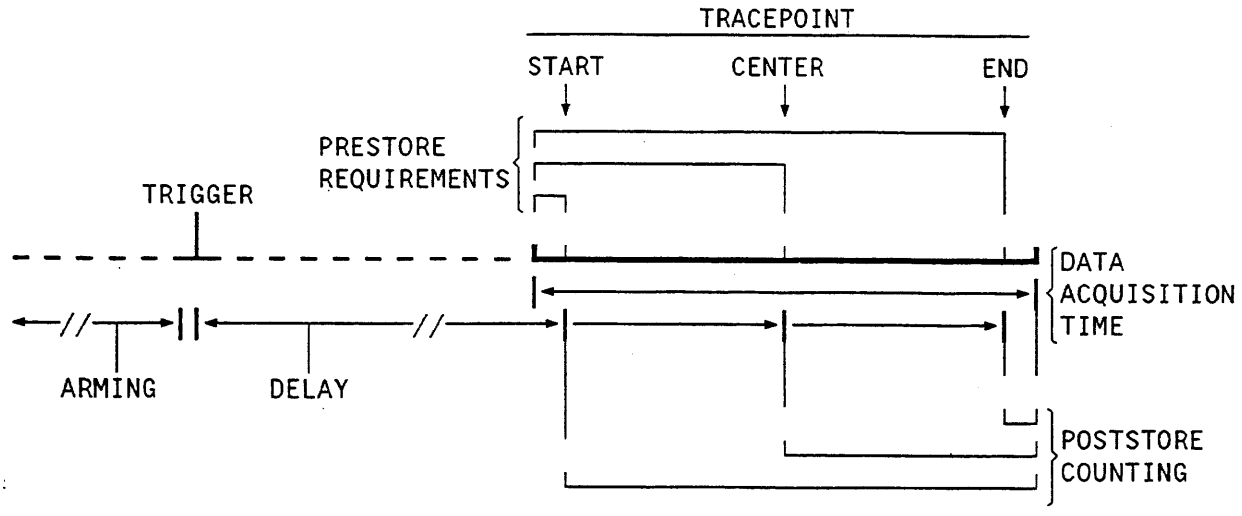


Figure 8G-2. Acquisition Sequence Diagram.

8G-12. THEORY OF OPERATION

8G-13. Analog Input (see schematic 8G-1)

8G-14. GENERAL. The Analog Input consists of impedance converters, gain control, and differential to single ended converters for the two data channels and an impedance converter, level shifting, shaping, and trigger selection for the trigger input. All control of this circuitry comes from the Analog Control, schematic 8G-5, and the outputs are to the Analog to Digital Converter schematic, 8G-2.

The waveform acquisition window is set up by defining the upper and lower voltage limits, not by setting "volts/division" like an oscilloscope. For this reason the CPU must compute, then adjust, the gain and offset of the analog signal path in order to put a signal with the menu defined limits into a window defined by the input limits of the Analog to Digital Converters.

The analog channels are calibrated by the system CPU. A D/A converter (schematic 8G-5) supplies a known signal (on EXTOFFS) which is selected by the relays at the input to the Channels 1 and 2 impedance converters.

8G-15. IMPEDANCE CONVERTERS. The three impedance converters, for the two analog channels and the trigger, are virtually identical. At the front of the channel inputs are relays which select the calibration signal.

The impedance converter as a whole is a unity gain amplifier with an input impedance of 1MΩ and an output impedance of approximately 50Ω. The dynamic range of the circuit is ±1.25V.

The channel offset inputs are used to center the signal input window, as defined in the analog menus, to the center of the dynamic range of the Gain Control Hybrid. All drifts and offsets within the waveform acquisition system are compensated for with the offset calibration. (See AUTO-CALIBRATION ROUTINE.) The relationship between the offset signal and the output of the impedance converter is: $+V_1$ at OFFSET = $-V_1(.4)$ at converter output

The resistors marked with asterisks on the schematic are part of a custom, laser trimmed network. Values shown are nominal, however the ratios between some sections are accurate. Further information is provided in the schematic notes.

The analog signal is split into two paths. The low frequency path is divided by two and fed into an opamp. The output of the opamp is summed with the high frequency signal (through the 1000pF capacitor) into the gate of the FET.

The output of the opamp is also divided by two (RP-R2 and RP-R3, both ≃40K) and with the .022μF capacitor forms an integrator function with the opamp. The inverting input also gets an input consisting of impedance converter feedback summed with an offset and drift correction signal set up by the CPU during the calibration sequence. Feedback from the output of the impedance converter works into a 2 to 1 divider of RP-R6 (≃39K) in series with the parallel combination of RP-R5 (≃74K) and RP-R7 (≃100K). The offset signal works into a 4 to 1 divider of RP-R7 (≃100K) in series with the parallel combination of RP-R5 (≃74K) and RP- R6 (≃39K). The summing junction of these signals is not accessible for measurement. The summed signal is fed through RP-R4 ≃300K).

The 51.1Ω resistor at the output of the converter, along with the source impedance of the converter, front-matches the 70Ω characteristic of the PC trace to the gain hybrid.

8G-16. GAIN HYBRID. The Gain Hybrid controls channel gain and internal trigger selection. The input impedance of the gain hybrid is approximately 2KΩ. The input dynamic range is ±1.25 volts. The gain is controlled by both discrete steps and vernier. The gain range is approximately from 1/2 to 32 and is continuously variable between the steps. The gain in the trigger path tracks the gain of the respective channel.

8G-17. Gain Control. Gain control is identical for both signal channels. Only one will be described. The gain control is used to fit the signal amplitude window defined in the analog menus to the input amplitude window of the Analog to Digital Converters. All control originates on the Analog Control schematic, 8G-5. See the Analog Control theory for further information.

The gain range of the entire channel amplifier system, to the input of the A/D converter, is from 32 (vernier at maximum) to 1/2 (vernier at nominal 1/2). This corresponds (as set up in the analog menus) to full scale data acquisition of 40mV to 2.5V, using a direct input or 1:1 probe. The following table shows the nominal full-scale windows for given gain selections.

Table 8G-1. Gain Control vs. Full-scale Deflections.

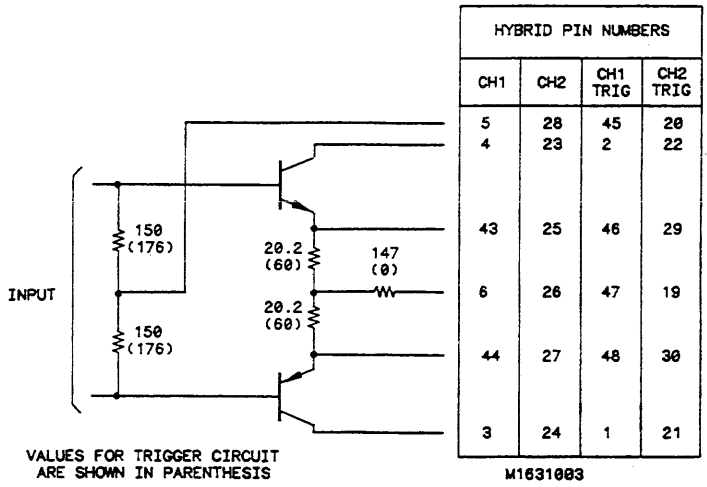
FULL SCALE INPUT	DISCRETE GAINS					VERNIER GAIN	OVERALL GAIN	FULL SCALE OUTPUT
	X8	X1A	X4	X2	X1B			
40mV	X		X			MAX (X1)	32	1.25V
80mV	X			X			16	
160mV	X				X		8	
320mV		X	X				4	
640mV		X		X			2	
1.28V		X			X	MAX (X1)	1	
2.5V		X			X	X1/2	1/2	1.25V

Five lines, CH1G1/2/4 AND CH1X1/8 control the discrete gain steps. Two lines, CH1VERN+/-, control the vernier gain. All control lines are current sources. The discrete lines are switched and the vernier lines are the output of a digital to analog converter. The vernier provides overlap between the gain ranges in order to accommodate variations in parts and the automatic calibration routine. A given gain factor could be reached with more than one combination of control steps.

The input of the hybrid includes an 8 to 1 divider that is selected by CH1X1A. CH1X8 selects the unattenuated signal. CH1X4/2/1B control the direct gain of the hybrid. CH1X1B selects the lowest gain factor and CH1X4 the highest.

The gain vernier lines, CH1VERN+ and CH1VERN-, control the summation of out-of-phase versions of the analog signal. The sum of the current in the lines is constant, about 4mA. When the current in the two lines is equal the summation makes the gain 0. When the current in CH1VERN+ is greater the signal has an amplitude dependent on the ratio between the currents. If the current in CH1VERN- was greater, the signal would be inverted. However, this is not done in the 1631A/D. Also, the calibration routine will not set the vernier to less than the nominal 1/2 except to allow for for minor non-overlap in the discrete gains due to parts variations. For further information, see the circuit description under Channel Vernier DACs in the Analog Control section of this theory.

8G-18. Output Circuitry. The output circuit of the channels and each trigger path are nearly identical differential amplifiers. A schematic is shown in the figure below. The collector outputs drive the external common base amplifiers. The emitters are connected to a frequency compensation series RC network.



HYBRID PIN NUMBERS			
CH1	CH2	CH1 TRIG	CH2 TRIG
5	28	45	20
4	23	2	22
43	25	46	29
6	26	47	19
44	27	48	30
3	24	1	21

Figure 8G-3. Hybrid Output Circuit.

8G-19. CHANNEL AMPLIFIERS. A simplified diagram of the Channel Amplifiers is shown below. Please use it for the following discussion.

The Channel Amplifier converts the differential current output of the Gain Control Hybrid to a single-ended voltage level output. The common base transistors Q8 and Q9 shift the 7V output voltage to a lower level. Voltage reference U5F and resistors R42 and R43 are the output load. (The voltage divider effect of R42 and R43 and the parallel combination of their values makes the equivalent circuit shown in the diagram.) Q4 and Q5 form a current mirror. Q4 is connected as a diode and provides temperature compensation for Q5 and compensates for the base emitter voltage drop of Q5.

The circuit works in the following manner. The sum of the currents in Q8 (I_1) and Q9 (I_2) is a constant, about 12mA. The current in Q4 (I_2) always equals the current in Q5 (I_3). The current in the load (I_4) equals I_1 - I_3.

With an input of 0V to the hybrid $I_1 = I_2$, about 6mA. Since $I_3 = I_2$, I_4 will be 0 and the output voltage is the same as the supply, -.62V. If the input of the hybrid goes to the positive limit, +1.25V, I_1 increases and I_2 decreases, about 1.5mA. I_4 equals twice the change in I_1, about 3mA, making the output voltage 0V. If the input goes to the negative limit, -1.25V, I_1 decreases and the output goes to -1.25V.

The equal resistors, R38 and R39, set the equal currents in Q4 and Q5. In addition, R39 is shunted by two RC time constants which provide peaking. The peaking compensates for rolloffs in other parts of the circuitry. R41/C51 is a low frequency peak and R40/C50 a high frequency peak. When there is a change in signal current (I_1 and I_2) that falls within the frequency range of one of the peaking circuits, the equivalent impedance in the emitter circuit of Q5 lowers, resulting in a greater change in I_3 than I_2 and I_1. The result is a greater change in the load current I_4 than the steady-state value of $2I_1$.

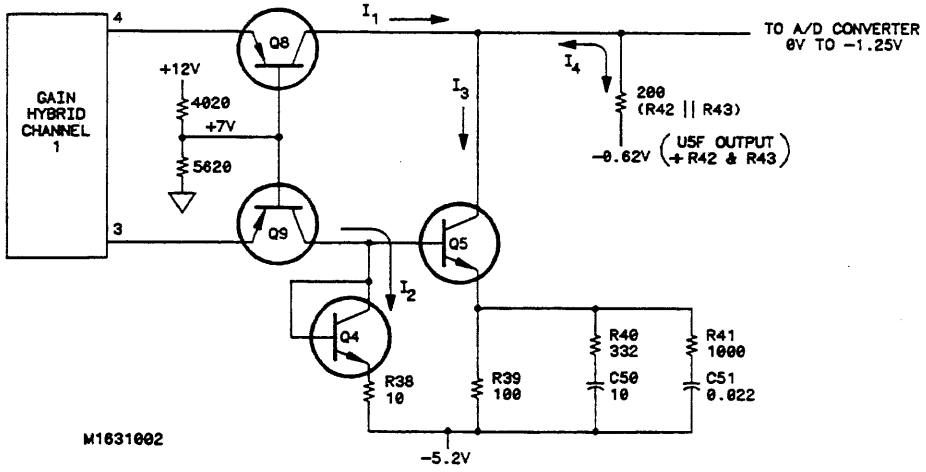


Figure 8G-4. Channel Amplifier.

8G-20. INTERNAL TRIGGER CIRCUITRY. The internal triggers from channels 1 and 2 are split off, selected, and amplified within the gain hybrid and summed at the output of the hybrid. Only one or the other can be selected. Q10 and Q11 amplify and match the trigger signal to the differential line receiver U15E (pins 9 and 10). Hysterisis for noise immunity is added with R55.

A D/A converter with current source output (U5J schematic 8G-5) is used to adjust the DC output of the sync sources so that the trigger level is correct when all of the circuit drifts and offsets are considered. The D/A current source is applied through R51 and R54. During the internal calibration sequence the CPU reads the status of the trigger signal at U7F pin 2. The current through R51 and R54 is adjusted to provide the trigger at the proper threshold.

8G-21. EXTERNAL TRIGGER CIRCUITRY. The trigger impedance converter is virtually identical to those in the data channels. The converter feeds into an amplifier that operates as a discriminator. The base of Q14 is at ground potential and the emitters of Q14 and Q15 are tied together, therefore the threshold at Q15 base is 0V. The system CPU, in setting the external trigger level requested, provides the offset (EXTOFFS) that puts the base of Q15 at 0V when the input signal is at the trigger level. An offset of 0V provides a trigger level at 0 volts.

The collector outputs of Q14 and Q15 are at ECL threshold at the trigger level. They drive differential line receiver U15E (pins 4 and 5) which has hysterisis provided by R66 so that noise in the trigger signal will not cause unwanted triggering. U15E drives two inputs to the trigger multiplexer.

8G-22. TRIGGER MULTIPLEXER. The Trigger Multiplexer selects the trigger source, internal or external, and polarity. The following circuit (Trigger Logic, schematic 8G-2) uses the positive edge of the signal from the multiplexer. The trigger is also read as a status line by the CPU.

8G-23. AUTO-CALIBRATION ROUTINE. The automatic calibration routine uses information entered into the analog menus to provide auto-calibration parameters. Calibration is done within the following considerations.

1. Complete auto-calibration is done when the instrument is turned on. The menu default values are used as parameters.

2. Calibration is done for gain and offset of each channel individually. Whenever an upper or lower limit is changed for a channel, the calibration routine is done for that channel.

3. The internal trigger is selected from a point in the circuitry after the gain and offset adjustment so the trigger signal path is affected by channel gain and offset changes. Calibration of internal trigger level adjusts for the difference between the center of the calibrated signal input window and the trigger level set in the menus. Therefore internal trigger level calibration is done whenever channel calibration is done.

4. Even if there are no changes in the Channel 1 or 2 parameters, internal trigger level is calibrated as soon as a RUN is initiated. The CPU does not check for changes in trigger parameters. It automatically recalibrates internal trigger before the run.

5. The CPU will make 45 attempts to calibrate a channel. If unsuccessful, the nominal values will be used to set up the channel and a warning message will be displayed.

Two basic elements are used in the calibration routine.

1. The External Trigger Offset DAC is used as a signal source for gain and offset calibration of the waveform channels. A signal of -2.048 to +2.048 volts can be set at the input of a channel. It is also used as a signal source for calibration of the internal trigger level.

2. The input relay selects the calibration signal for input to the channel.

8G-24. Gain, Vernier, and Offset Calibration. The purpose of this part of the auto-calibration is to make the signal window defined in the analog menus fit the entire dynamic range of the Analog to Digital Converters. This provides digitization of the signal with maximum resolution. The offset puts the input signal window at the center of the dynamic range of the Gain Control Hybrid. The gain makes the defined window amplitude fit the input amplitude window of the ADCs. The input amplitude window to the ADCs is 0 to -1.25V. The procedure starts with the CPU guessing the nominal gain and offset values from the menu entries.

To guess the gain:

$$\textbf{GAIN} = \frac{1.25}{\textbf{W.S.}}$$

(Window setting)

The fixed gain (F.G.) is:

F.G. = Closest Integer (1,2,4,8,16,32) > GAIN

The variable gain (V.G.) is:

$$\textbf{V.G.} = \frac{1.25}{\textbf{W.S.} \times \textbf{F.G.}}$$

For example, with an input window of -.1V to +.8V the gains would be:

$$\textbf{GAIN} = \frac{1.25}{.9} = 1.388$$

F.G. = 2

$$\textbf{V.G.} = \frac{1.25}{.9 \times 2} = .694$$

The fixed gain (F.G.) is one of the discrete gains set in the gain hybrid. The variable gain (V.G.) is also set in the gain hybrid by the Gain Vernier DAC.

The calibration routine effectively centers the channel input window around 0 volts at the input to the Gain Control Hybrid. Therefore the guessed offset is that required to provide 0V into the Gain Hybrid with an input equal to the center of the window. In the example above the center of the window is +.35V, therefore the guessed offset offsets that value.

The defined input window, centered around zero, is divided into equal voltage intervals. The number of intervals depends on the amplitude of the window and the resolution of the External Trigger Level DAC. The DAC is used to feed the window voltage, one interval at a time, into the signal path and digitize them. The Waveform Acquisition Memory is incremented after each digitization so an approximate straight line has been digitized. The corresponding values are read by the CPU and and an RMS Error (line fitting) algorithm is run to calculate the the gain and offset errors. This routine repeats until the RMS errors are less than one increment of the gain and offset DACs. If the calibration routine for a channel fails to converge in 45 trials for any window, auto-calibration will be turned off and the default (guessed) values will be used.

After each channel is calibrated, the values for fixed gain, variable gain, and offset are saved and used for pre-run loading of the analog board.

8G-25. Trigger Level Calibration. While the ADCs are used to monitor the output of the channels during calibration, the CPU monitors the state of the trigger by watching the level, high or low, of the output of the Trigger Source and Slope Selector, U7F. This output, HTRIGGER, is read as a status line by the CPU. Only the Internal trigger level needs to be calibrated. The external trigger level is set directly by the External Trigger Level DAC.

To calibrate the internal trigger level the following steps are used.

1. The trigger level specified in the menu is made an input from the External Trigger Offset DAC, to the channel specified to be the trigger channel.

2. Starting with the lowest possible code, the Internal Trigger Level DAC is incremented down, step by step, until the trigger output (HTRIGGER) toggles.

3. The DAC value that makes the trigger level change is recorded.

4. Next, starting with the highest possible code, the Internal Trigger Level DAC is incremented down until the trigger output toggles.

5. The second DAC value is recorded and averaged with the first and that value is saved and used as the input to the Internal Trigger Level DAC.

8G-26. Analog to Digital (see schematic 8G-2)

8G-27. GENERAL. The Analog to Digital circuitry samples and digitizes the two channel input signals and outputs the data to the acquisition RAM. Sampling is initiated by the inputs to U13I and U11J, and is clocked by the acquisition clock H/LACK.

8G-28. ANALOG TO DIGITAL CONVERTERS. The ADCs are "flash converters" which digitize samples of the input signals. The input signal range is from 0V to -1.25V. The minimum sample period is 5ns, a 200MHz sample rate from both edges of the 100MHz (maximum) clock. HCLK and LCLK provide the sample rate. The clock enable signals, LCE0-3, provide four phases at half the sample rate to help move data inside the converters.

The converters consist of an array of comparators, of which one input of each is connected to the input signal and the other is connected to a tap on an accurate voltage divider stick. A reference voltage is applied to the divider stick. At the time of the sample, the output of the comparators is latched. The amplitude of the signal determines which comparator outputs were high or low and logic circuitry then converts the comparator outputs into a six-bit binary code. Four samples are taken and stored in the converter before the data is updated at the converter output. The data at the output is stable for four sample periods before it is updated again.

The output data, CH1(2)D00-35, is bused to the Acquisition RAM, schematic 8G-3. The digits in the output mnemonics, XX, refer to the sample number and bit significance in that order.

A reference supply, U8G, sets up the bias on the voltage divider stick in the converter. It uses an output of the Channel 1 converter as a reference. The output of the reference supply is 1.2V more negative than the reference.

U9D monitors certain lines of the converters and compares them with references, then sets the bias at other lines. Voltage levels are shown on the schematic.

8G-29. TRIGGER INITIATION. The trigger is initiated by the inputs to the Trigger Logic circuit. The output of this circuit is LASYNTRG (Low Asynchronous Trigger). When this signal goes low the trigger point is marked.

The analog reset, HRESET, sets U13I at pin 12. Pin 15 is therefore high preventing data storage. When LTRGARM becomes true (schematic 8G-4), the next positive edge of the analog trigger (schematic 8G-1) clocks LTRGARM into U13I and LASYNTRG marks the analog trigger point.

If HTIM (High Trigger Immediate) is high (DON'T CARE TRIGGER is selected) U13I is held reset so pin 15 is held high by pin 14 of U11J. As soon as LTRGARM is true the trigger point will be marked without benefit of analog trigger.

8G-30. SAMPLE CLOCKING

8G-31. Clock Signals. The clock rate is set by the CPU depending on the Sample Period selected through the analog menus. If the sample rate defined in the menus is from 5ns to 200ns, the sample clock originates on the Timing Master board. If the sample rate is from 500ns to 500ms it originates on the CPU board. During calibration routines the sample clock can be toggled one clock at a time from the Timing Master board.

The Clock Shaper cleans up the HACK and LACK signals to form the HCLK and LCLK signals. The SKEW adjustment changes the threshold of U15E input to make the duty cycle for the H/LCLK signals exactly 50%. Samples are taken on both edges of HACK and LACK so the timing of these two signals is critical for precise clocking of the ADCs.

The Clock Enable Generator provides four phases at half the clock rate. These four signals, LCE0-3, are used to move data through the ADCs. Two of the signals, LCE0 and LCE3, are monitored to tell the CPU on which sample of the four-sample frame that asynchronous trigger occurred.

8G-32. Trigger Synchronizer. The Trigger Synchronizer synchronizes the qualified but asynchronous trigger from the analog circuits, to the acquisition clock. One output, HSYNTRG, is used to enable the delay counters (schematic 8G-4). Both of the outputs are used to clock the Trigger Sample Identifier flip-flops.

8G-33. Trigger Identification. The analog system is always storing data before the trigger-point because no less than 1/16th of the acquired data is stored before trigger. Data is also being stored during delay times. Data is stored in 4-sample increments, so the Trigger Sample Identifier is used to identify between which samples trigger occurred.

The complementary outputs of U15F provide low-to-high transitions which clock the status of LCE0 and LCE3 into U13H. The outputs of U13H, TSI0 and TSI1, are read by the CPU to identify the trigger point.

8G-34. Synchronous Stop. At the end of a run it is important to stop the clocking circuitry in a known state and signal the rest of the system that the measurement is complete. The sample clocks continue to run after the trace so the Synchronous Stop Flip-Flop is used to halt the Clock Enable Generator.

When the Poststore Counter (schematic 8G-4) reaches terminal count the acquired data is considered complete. LABORT is high during a run so the Poststore terminal count output, LAMC Analog Measurement Complete), is gated to pin 10 of U15G. The next positive edge of LCE1 toggles the flip-flop. When U15G pin 14 goes high, it's clock input pin 11 will be high and effectively latch the flip-flop in that state, LCE1 will be locked high. The same high at U15H pin 10 latchs that flip-flop with both outputs high on the next edge of the sample clock. The other half of U15H also halts when LCE3 stops.

8G-35. MEASUREMENT COMPLETE. As LAMC is clocked into U15G pin 10, Pin 15 goes low, which is clocked into the Measurement Complete Flip-Flop. The low at U15G pin 2 is gated (LABORT is high during a run) onto the LMCI line to the rest of the system. If a trace is aborted during a run LABORT puts LMCI low.

The LABORT line (U11H pin 5) is also used by the CPU to keep the analog system off of the LMCI line when analog is not in use.

8G-36. BNC OUTPUT. If the analog trigger has been selected for output to the rear panel BNC, the CPU puts LBNCEN low. LASYNTRG is gated and inverted and becomes the signal on the HBNC bus.

8G-37. Acquisition Memory (see schematic 8G-3)

8G-38. GENERAL. The Waveform Acquisition Memory consists of two sections, one for each channel. There are 1024 six-bit samples in the acquired data of each channel. One memory IC stores the same significant bit of every sample in that channel. The Memory Address Counter (schematic 8G-4) sequences the memory via MA0-7. The block selects, LBS0-7, enable read/write. R/WEN (Read/Write Enable) controls read or write function.

It should be noted that the address bus is not connected to the memory devices with the same bit significance as that shown in the manufacturers data book. Since the device is truly random access, the connection to other circuitry is unimportant.

8G-39. WRITE SEQUENCE. The write sequence is shown in the timing diagram below.

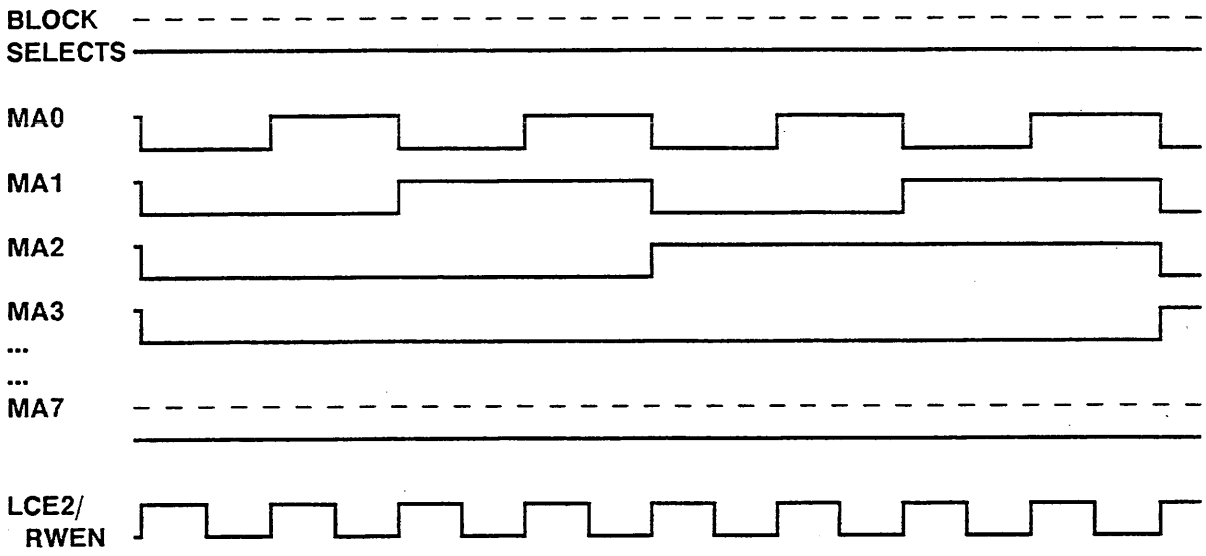


Figure 8G-5. Acquisition Memory Write Timing Diagram.

8G-40. READ SEQUENCE. The read sequence is shown in the timing diagram, figure 8G-6. At the end of the acquisition period the Memory Address Counter points to the newest data in memory. If memory has been filled (no abort) the next memory position holds the oldest data. The CPU clocks the MAC to the first new data before reading. The CPU always keeps track of the clocking of the MAC because it cannot read the address output. The newest data would not likely be in address 0000 0000 but for purposes of the example, the timing diagram assumes so.

The RWEN line is high because LCE2 is low and LMWRT is high. This enables the read function of the RAM.

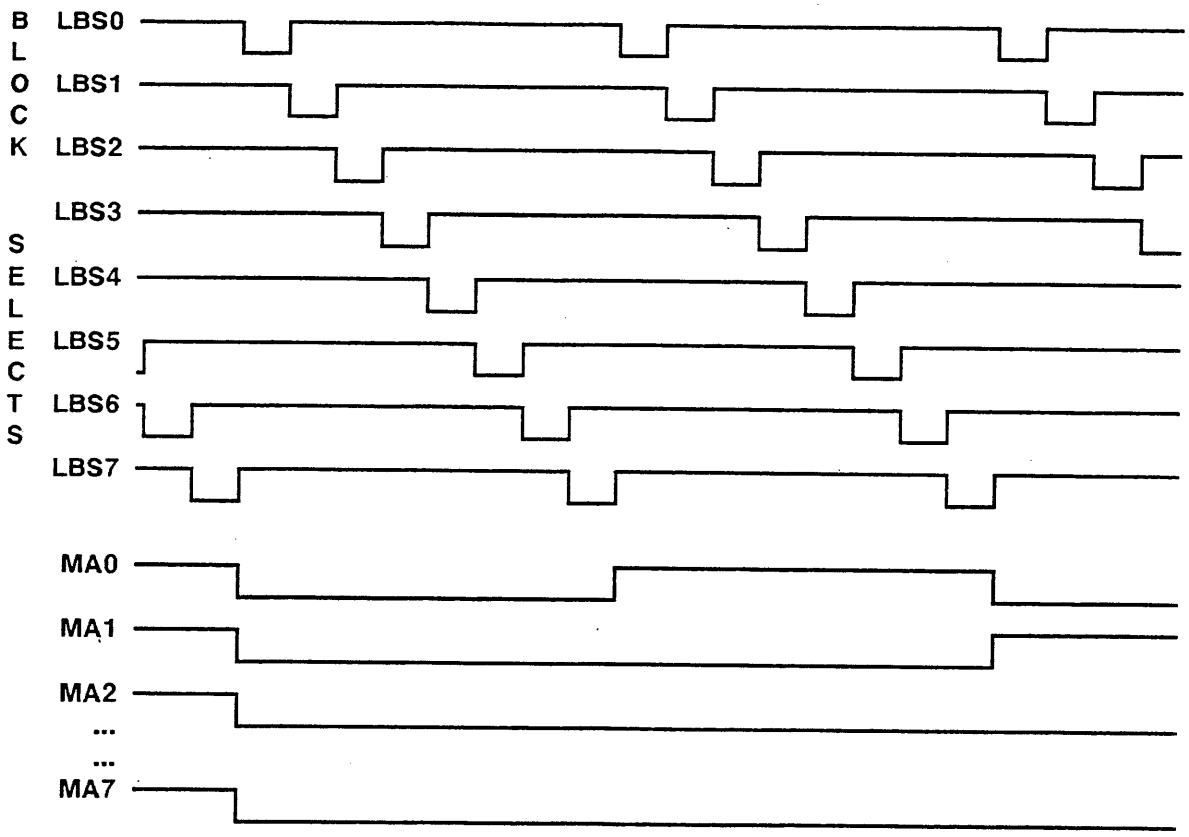


Figure 8G-6. Acquisition Memory Read Timing Diagram.

8G-41. Digital Control (see schematic 8G-4)

8G-42. GENERAL. The Analog Board is controlled by the system CPU from the system bus. Assigned to this board are 16 read and 16 write addresses. When HA4 and HA5 (U11K pins 12 and 13) are high the Analog Board is being accessed by the system CPU. LSTB (Low Strobe U13J pin 10) is then gated to U13J pins 5 and 6. HRLW (High Read Low Write, U13J pin 13) is buffered and the two phases of it are gated through U13J (pins 4 and 7) to provide the read/write aspects of control. U13J pin 3, is therefore low during CPU write and pin 2, LCPUR, is low during CPU read.

Eight of the 16 write addresses are used for ECL control (this schematic) and eight are used for TTL control (schematic 8G-5). A low at U11J pin 6 and pin 7 (HA3 high) provides a low at pin 3 which enables writing to TTL, LTWRT (Low TTL Write).

8G-43. CONTROL LATCH. Quint latch U7J latches data from the CPU data bus to set five control lines. The functions of these lines is covered along with the circuits they control.

8G-44. BLOCK SELECT. The Block Select helps control writing to and reading of the Waveform Acquisition Memory. During the entire acquisition time, while the waveforms are being written to RAM, BS0-7 are held low by the output of U11J (pins 9 and 15) which disables U7H and the inputs to U11K (pins 4 and 6). This allows the Memory Address Counter full access to RAM.

When the Acquisition RAM is being read, the block select is enabled through U7H and U11K. When decoder U9H is enabled, the output lines are high except for the line corresponding to the decoded input. Therefore BS0-7 are held high, except the line for the block being read from.

8G-45. COUNTERS. Three sets of counters control the storage of data into RAM. The Delay Counter, Memory Address Counter, and Poststore Counter are composed of one or more 4-bit binary counters which can be preloaded from the data bus by the CPU. After a binary counter pair (or U3C by itself) is enabled by an output of U9H the CPU uses HA2 (enabled by LCPUW at U11J pin 4), through U11J, U7K, and U9C, to strobe data into the counters. U9C pin 11 is held low any time data is not being acquired, so the INDEX line at U9C pin 14 follows pin 10.

8G-46. Delay Counter. The Delay Counter counts the delay between the occurrence of asynchronous trigger and the Start, Center, or End of the acquired data (depending on the setup of the instrument). The counter chain is loaded so that it reaches terminal count at the end of the delay period. The counter is enabled by LLSYNTRG and incremented by INDEX which, during a run, is CE2B gated by U9C (U9C pin 10 is low). CE2B has a rate one fourth that of the sample rate so the Delay Counter counts frames of four samples each.

When U3E reaches terminal count and pin 4 goes low U7E pin 6 also goes low allowing the next INDEX clock to toggle U7E. U7E, the Tracepoint Latch Flip-Flop, was set before the run. If the Analog Board has been set up as master, the resulting high at U11H pin 14 (HARM) tells the system that the tracepoint has been found. The complementary low at U7E pin 2 tells (through U3F) that tracepoint was found and also enables incrementation of the Poststore Counter through U9C (pin 6).

8G-47. Memory Address Counter. The Memory Address Counter (MAC) sequences the acquisition memory to load and read the stored data. It is clocked by the INDEX line.

To be sure that the entire memory is full of new data after a run, the CPU loads the counter with a prestore requirement before the run. In a case such as Center or End trace on trigger the acquisition cycle could end before the MAC had counted a full 256 states (256 X 4 = 1024 samples, a full fresh memory). To prevent this the CPU considers the instrument setup (Start, Center, or End Trace on Trigger), Sample Rate, and Delay, then calculates and loads the prestore requirement. When the MAC reaches the first terminal count the terminal count output, U5C pin 4, clocks the Prestore Valid Flip-Flop, which is one of the prerequisites for trigger arming.

During an acquisition run the counter is clocked by LCE2 which runs at 1/4th the sample rate. Each increment of the counter is used to load one frame (four samples). During a read the CPU increments the counter with one of the address lines (HA2) and the memory is read one sample at a time.

8G-48. Poststore Counter. The Poststore Counter counts the period between tracepoint and the end of the acquired data. It provides the difference between Start, Center, and End of trace. It counts overflows of the first hexade (÷16) of the Delay Counter (16 frames-64 samples), which are gated through U9C by the Tracepoint Latch Flip-Flop. The count range therefore, is approximately 256 frames (1024 samples), the length of acquired data.

When Start trace on tracepoint is set up, the counter is loaded with 0000 which gives 15/16ths of the acquired data after tracepoint. For Center, it is loaded with 0111 and for End, it is loaded with 1110 which gives 15/16ths of the acquired data before the tracepoint.

The terminal count of the counter goes to U3F for the CPU to recognize and to the Analog to Digital circuits (schematic 8G-2) where it initiates the synchronous stop of the A/D Converter clocking.

8G-49. ARMING LOGIC. The Arming Logic selects the source of the HARM signal. HARM is a line that can be used by either the State, Timing Master, or Analog acquisition systems to arm the other systems, depending on which has been designated as master. If Analog has been designated as master HANMAST (U7J pin 4) is put high. The other acquisition systems read the HARM line rather than control it. HANMAST gates the tracepoint signal from the Tracepoint Latch Flip-Flop onto the HARM line.

If HANMAST is low, one of the other acquisition systems is master so the HARM signal is gated through U11I (pin 10) and used to arm the analog system.

8G-50. PRESTORE VALID/MEMORY FULL. The Prestore Valid Flip-flop is set before a run, therefore pin 15 is high, which "disarms" the trigger (schematic 8G-2). After reaching the first terminal count of the Memory Address Counter, the prestore requirement has been met. The next count (FF to 00, terminal count low to high) clocks U9I pin 15 low and satisfy one of the requirements for trigger arming.

The Memory Full Flip-Flop is reset before the run. Upon reaching the second terminal count of the Memory Address Counter the next count (FF to 00) clocks U9I pin 3 low. This tells the CPU that memory is indeed full. In the event of an aborted trace the CPU can increment the MAC while watching LMFULL. Along with other information, this allows the CPU to figure out the status of the data acquired.

8G-51. OUTPUT DATA SELECTORS. The Output Data Selectors are enabled during a CPU read. They are two-input multiplexers. One set of inputs is the six bits of data from the Waveform Acquisition Memory (schematic 8G-3). These lines cannot be read during a run since the memory cannot be written to and read from at the same time.

The other inputs are status lines from several areas of the analog system. They can be monitored while the system is acquiring data.

8G-52. Analog Control (see schematic 8G-5)

8G-53. GENERAL. The Analog Control, schematic 8G-5, provides all of the control for the Analog Input section of the analog system (schematic 8G-1). Eight of the sixteen write addresses assigned to the analog system are used for control in this section.

Most of the devices in the Analog Control are TTL. The system bus is ECL, so ECL-TTL converters provide TTL address and data for most of this circuitry. To prevent excess noise on the board, the TTL data and address lines are kept quiet except when needed. This is controlled by the HTTL line. The HTTL line is ECL level. When low, R8 and R9 divide the ECL low (pulled down to -5.2V) down to -2.2V. This keeps the threshold input at the ECL to TTL line receivers below the ECL threshold. When HTTL is ECL high, the threshold input goes to -1.3V, ECL threshold, and the signals at the input of the line receivers is enabled to the output.

The ECL address lines HA0-2 and LWRT, Low Write, are shifted to TTL by U9J. The address lines are decoded by U9K. The outputs of U9K control loading of data into the TTL circuitry. Four of the outputs of U9K are pulled up by 5KΩ resistors. This provides extra high level drive for the TTL D/As which may be marginally driven by U9K which is low power Schottky.

8G-54. ANALOG GAIN SELECT. The Analog Gain Select Circuitry consists of a group of converters to convert ECL and TTL levels to the currents necessary to drive the gain select inputs of the Gain Control Hybrid (schematic 8G-1). The actual significance of individual control lines is covered in the theory for the Analog Input schematic (8G-1).

ECL latch U7I is actually loaded with data as part of the ECL group but is shown here grouped with the rest of the analog control. One latched output, HTIM (High Trigger Immediate), controls functions of the asynchronous trigger generation on schematic 8G-2. HEXT and H+SLP control selection of internal or external triggering and trigger slope respectively. The other two outputs are used to drive the inputs of four comparators with current source outputs. Each ECL line drives

two comparators so that the complementary ECL levels provide complementary drive for the two gain control lines. For example, an ECL low at U7I pin 3 drives U17A pin 1 to -12V and pin 14 open circuit. This enables the CH1X8 function. Conversely ECL high activates the CH1X1A function.

TTL latch U5I is enabled by an output of the address decoder U9K. Three of the TTL outputs, HCAL, LCH1TRSEL and LCH2TRSEL control analog functions directly. The other four outputs, two for each channel, are used to set gain functions of the Gain Control Hybrid. The three transistors in a channel control group work as a three way steering switch. The object is to provide approximately 2mA of current into the gain line to be activated. The discrete transistor sets the switching threshold. A TTL high at the base of both of the transistors in the array keeps them off and the discrete transistor on, activating the (CH1/2)X4 function. If one of the array transistors is on (base at TTL low) that gain function active and the discrete transistor turns off, deactivating the function.

8G-55. CHANNEL VERNIER DACS. The Channel Vernier DACs are 8-bit DACs with current outputs. The DACs are loaded from the data bus when enabled by the respective output of the Address Decoder, U9K. Figure 8G-7 shows the DAC as connected to the Gain Hybrid.

The current outputs are referenced to the current into DAC pin 14 (VREF+) with the relationship:

$$[I+]+[I-] = 4I_{REF}$$

I_{REF} is .5mA. CR1 and CR2 are located next to the Gain Hybrid and compensate for temperature changes in the hybrid. The current relationships for different gain values are shown in table 8G-2.

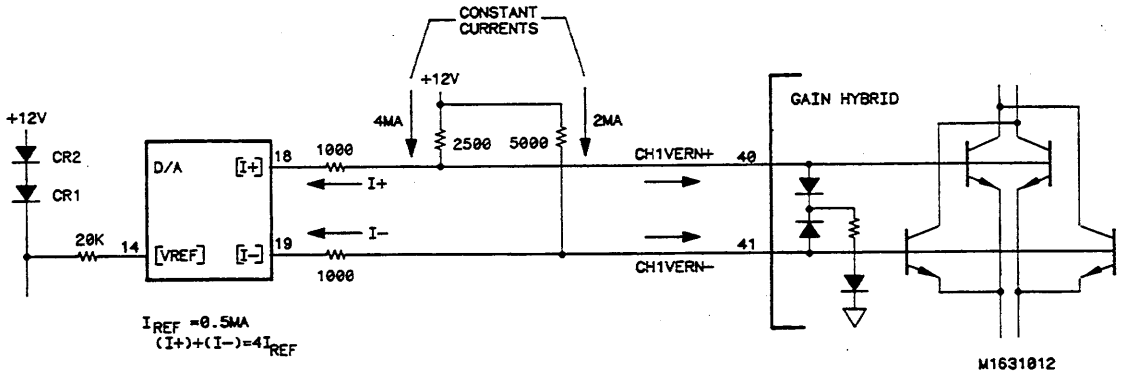


Figure 8G-7. Channel Vernier Control Circuit.

Table 8G-2. Gain Vernier Current Relationships.

GAIN	I+	I-	$I_{CH1VERN+}$	$I_{CH1VERN-}$
X1	0mA	2mA	4mA	0mA
X.5	1mA	1mA	3mA	1mA
X0	2mA	0mA	2mA	2mA

It should be noted that although the DAC and the Gain Hybrid can be set for a gain of 0, it is never set up for that. The discrete gains have a nominal 2:1 progression so a nominal vernier gain of 1/2 is the lowest needed. Any vernier setting below 1/2 is set because there is not an exact 2:1 relationship between two of the discrete gains.

8G-56. INTERNAL TRIGGER LEVEL DAC. The Internal Trigger Level DAC is the same as the Channel Vernier DACs except that it's output is used as a current source for the Internal Trigger Amplifier.

8G-57. OFFSET DACS. The three Offset DACs are 12-bit devices with voltage level outputs of ±5V. Two of the DACs offset the analog channel signals and the other the external trigger level. The latter is also used to provide a calibration signal for the analog signal channels. It is provided with a reference adjustment to make it more accurate.

The DACs are loaded from an 8-bit data bus so they have to be loaded in sections. The decoder U9K provides the enables for loading. There are four latches in the DACS, 2D, 3D, 4D, and 5D. The enables to the 2D, 3D, and 5D latches are connected together on a given DAC but separate for the three DACs. The enable for the 4D latch is common to all DACs. The DACs are loaded with a series of steps involving the enables to the latches. The step sequence follows.

1. Data on HTD0-3 is enabled into all DACs, latch 4D.

2. New data on HTD0-7 is enabled into first DAC, latches 2D and 3D. At the same time, data is latched from 2D, 3D, and 4D into 5D. The first DAC is now loaded and the output changes.

3. New data on HTD0-3 is again loaded into 4D of all DACs.

4. New data on HTD0-7 is loaded into the second DAC, latches 2D and 3D and again all latches are loaded into 5D. The new data, while it is loaded into 4D of the first DAC, it is not loaded into 5D so it has no effect.

5. The process repeats once more for the third DAC.

8G-58. MNEMONICS

The following signals, listed in alphabetical order, are used on the Analog Board. Active high signals have "H" as the first letter; active low signals have "L".

Table 8G-3. Mnemonics

Mnemonic	Description
CALSIG	CALIBRATION SIGNAL. Signal used as an input to the analog channels during the internal calibration routine. A divided version of the EXTOFFS signal from a D/A.
CH1D00-35	CHANNEL 1 DATA. Data output of the Channel 1 Analog to Digital Converter. Twenty-four data bits, four samples of the analog signal, six bits each.
CH1OFFS	CHANNEL 1 OFFSET. Compensates for input signal DC component and drifts in the analog circuitry. Signal level is ±5V.
CH1SIG	CHANNEL 1 SIGNAL. Channel 1 analog signal prepared for A/D Converter. Signal level is from 0V to -1.25V maximum.
CH1VERN+ CH1VERN-	CHANNEL 1 VERNIER. An analog current which provides gain vernier control in the gain control hybrid.

Table 8G-3. Mnemonics (Cont'd)

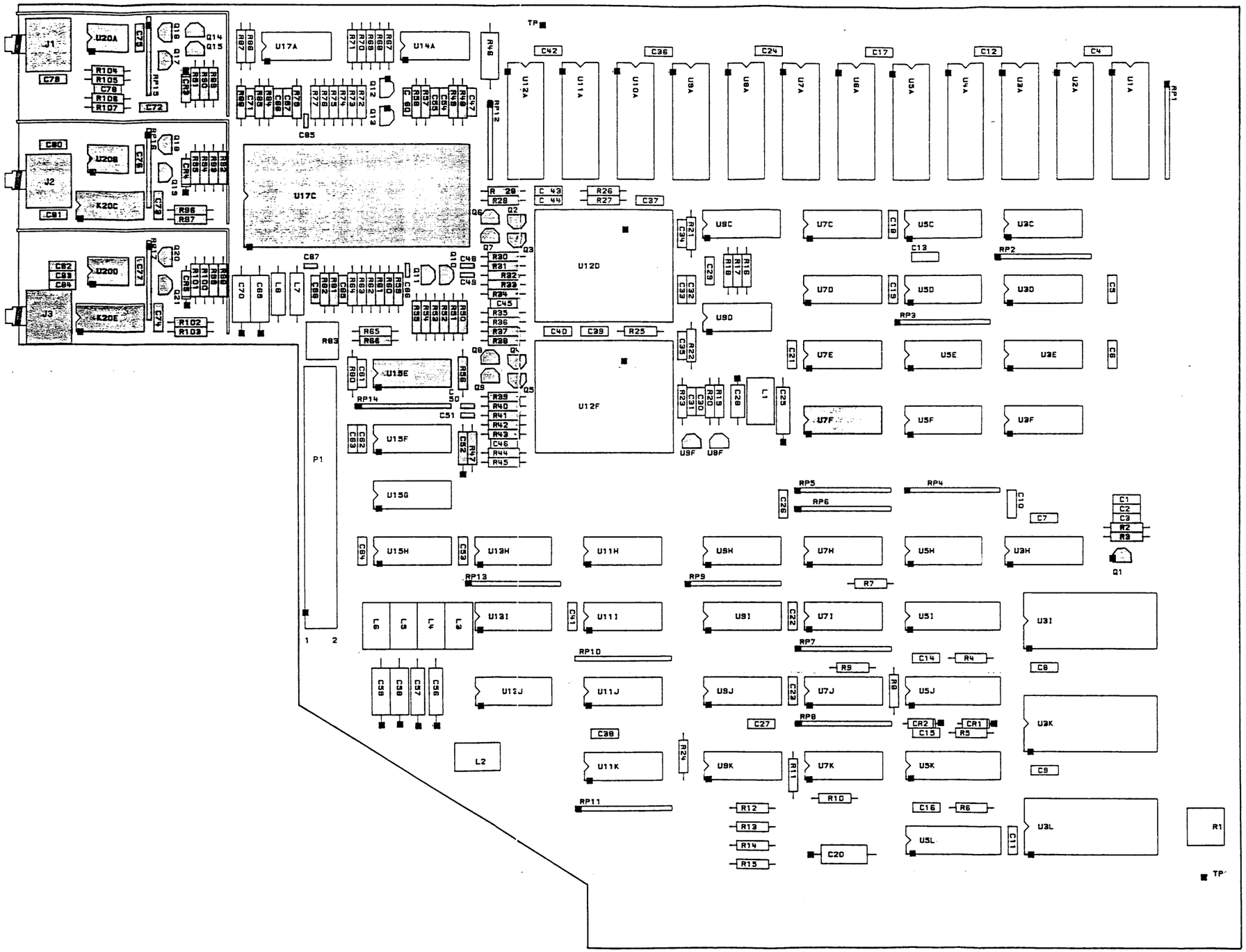
Mnemonic	Description
CH1X1A CH1X8	CHANNEL 1 GAIN CONTROLS. These are current sources which control gain in the Gain Control Hybrid.
CH1X1B CH1X2 CH1X4	CHANNEL 1 GAIN CONTROLS. These are current sources which control gain in the Gain Control Hybrid.
CH2D00-35	CHANNEL 2 DATA. Comparable to CH1D00-35.
CH2OFFS	CHANNEL 2 OFFSET. Comparable to CH1OFFS.
CH2SIG	CHANNEL 2 SIGNAL. Comparable to CH1SIG.
CH2VERN+ CH2VERN-	CHANNEL 2 VERNIER. Comparable to CH1VERN+ and CH1VERN-.
CH2X1A CH2X8	CHANNEL 2 GAIN CONTROLS. Comparable to CH1X1A and CH1X8
CH2X1B CH2X2 CH2X4	CHANNEL 2 GAIN CONTROLS. Comparable to CH1X1B, CH1X2, and CH1X4.
CPUINDEX	Signal set up by CPU, buffered to the INDEX line and used to clock circuitry under control of the CPU during loading etc.
EXTOFFS	EXTERNAL OFFSET. Analog signal used to compensate for the DC component of the external trigger signal, for drifts in the external trigger circuitry, and set the external trigger level. This signal is also used as a signal source when setting the gains of the channels 1 and 2 signal path during the calibration routine.
HA0-5	CPU ADDRESS BUS.
HACK LACK	ADDRESS CLOCK. System clock derived on the Timing Master board. Complementary signals used as a sample clock on the Analog board.
HANMAST	ANALOG MASTER. Set true by CPU to make the analog system the master system. Used to gate tracepoint signal onto the system arming bus, HARM.
HARM	ARM. Line used by master acquisition system to arm slave systems.
HBNC	Mainframe bus line used to drive rear panel BNC output.
HCAL	CALIBRATE. ECL signal which energizes the relays that connect the EXTOFFS signal to the input of the channels for internal calibration.
HCLK LCLK	Sample CLOCK. Cleaned up version of the H/LACK signal. Used to clock the Analog to Digital Converters.

Table 8G-3. Mnemonics (Cont'd)

Mnemonic	Description
HD0-7	CPU DATA BUS.
HEXT	EXTERNAL. ECL level signal. High selects external and low internal trigger.
HPSVLD	PRESTORE VALID. Indicates prestore requirements met. Monitored by CPU.
HRESET	RESET. Reset signal for analog system.
HRLW	HIGH READ LOW WRITE. ECL level read/write control signal from the CPU.
HSYNTRG	SYNCHRONOUS TRIGGER. Corresponds to LASYNTRG but is synchronized to the acquisition clocking, HACK and LACK.
HTD0-7	TTL DATA. CPU data bus converted to TTL and enabled by HTTL.
HTIM	TRIGGER IMMEDIATE. TTL signal set by CPU to allow triggering immediately after trigger circuit is armed.
HTRIGGER	An ECL representation of the analog trigger after processing and selection.
HTTL	Enables TTL functions for CPU write.
HWDSEL	WAVEFORM DATA SELECT. Selects acquired waveform data for output onto the CPU data bus.
INDEX	Clock signal used to increment counter chains. Derived from LCE2 during data acquisition and HA2 when CPU preloads counters.
INTRLVL+ INTRLVL-	INTERNAL TRIGGER LEVEL. Analog current sources used to set the DC level of the internal trigger circuitry.
LABORT	ABORT. Set by system CPU to end data acquisition.
LAMC	ANALOG MEASUREMENT COMPLETE. True at terminal count of Poststore Counter. Signals the end of the analog acquisition period and is used to initiate synchronous stop of ADC clocking.
LASYNTRG	ASYNCHRONOUS TRIGGER. Qualified analog trigger.
LBNCEN	BNC ENABLE. Set by CPU to put analog trigger, LASYNTRG, onto HBNC.
LBS0-7	BLOCK SELECTS. Select blocks of memory (one analog sample per block) for read and write functions. All are kept low during write function. Set low individually to read data samples out of memory.
LCE0-3	CLOCK ENABLES. Signals consisting of four phases at half of the sample rate used by the ADC to clock data.
LCH1TRSEL	CHANNEL 1 TRIGGER SELECT. ECL signal selects Channel 1 as trigger.

Table 8G-3. Mnemonics (Cont'd)

Mnemonic	Description
LCH2TRSEL	CHANNEL 2 TRIGGER SELECT. Comparable to CH1TRSEL
LCPUR	CPU READ. Low true as CPU is reading analog system data and status lines.
LCPUW	CPU WRITE. Low true when CPU is writing to analog system.
LCTRL1EN	CONTROL 1 ENABLE. Write enable to control latch for ECL level devices in the Analog Control section.
LLSYNTRG	LATCHED SYNCHRONOUS TRIGGER. Corresponds to the synchronous trigger, HSYNTRG, however it has been resynchronized and latched to enable the Delay Counters. Also read by the CPU to indicate achievement of the qualified analog trigger.
LMCI	MEASUREMENT COMPLETE INTERRUPT. Mainframe bus used by any of the acquisition systems to tell CPU they are finished with acquisition. Becomes true when all acquisition systems are finished.
LMFULL	MEMORY FULL. Monitored by CPU to tell when Acquisition Memory has been completely filled.
LMWRT	MEMORY WRITE. Read and write enable for the Acquisition Memory.
L+SLP	POSITIVE SLOPE. ECL level signal. Low selects analog trigger on positive slope, high selects trigger on negative slope.
LSTB	STROBE. ECL level control signal from the CPU. Used with HRLW to indicate a data transfer between the CPU and one of the acquisition systems.
LTPL	TRACEPOINT LATCHED. Monitored by CPU to tell when tracepoint, the end of delay, has occurred.
LTRGARM	TRIGGER ARM. Arming signal for analog trigger. True after arming and prestore requirements are met.
LTWRT	TTL WRITE. Set low true when the CPU is writing to TTL circuitry, primarily the D/A converters in the analog control section.
MA0-7	MEMORY ADDRESS. Output of the Memory Address Counter.
RWEN	READ/WRITE ENABLE. Sets the Read/Write function of the Acquisition RAM. Low true sets the write function.
TSI0 TSI1	TRIGGER SAMPLE IDENTIFIER. The state of two CLOCK ENABLE LINES, LCE3 and LCE0, just after occurence of the asynchronous trigger, LASYNTRG. Used by CPU to mark between which samples trigger occurred.
WD0-5	WAVEFORM DATA. Stored analog waveform data. Output from Acquisition RAM to Output Data Selectors, then CPU data bus.



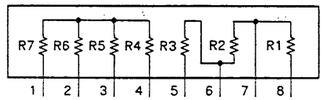
Component Locator for Schematic 8G-1

NOTE 1:

Resistor packs RP15-RP17 are a custom laser-trimmed network. The nominal values of these resistors is shown on the schematic. However, the resistor values may vary considerably (±25%) from nominal. The ratios between the resistors are what is important.

RP-R1 = 1MΩ ±25%
RP-R2 = 40KΩ ±25%
RP-R3 = RP-R2 ±2%
RP-R4 = 300KΩ ±25%
RP-R5 = 0.747×RP-R7 ±2%
RP-R6 = 0.393×RP-R7 ±2%
RP-R7 = 100KΩ ±25%

RESISTOR PACKS RP15–17

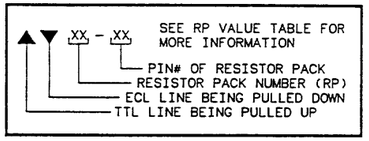


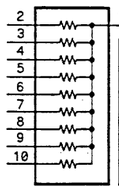
As can be seen RP-R1, R2, and R3 can be measured directly. The other resistors do not have the common node as an output so they can only be measured in combination with the other resistors in the group.

IC DEVICE POWER CONNECTIONS

SUPPLY	PIN NO.	IC GROUP
GND GND −5.2V	1 16 8	U7F,15E

RESISTOR PACK DESCRIPTIONS:

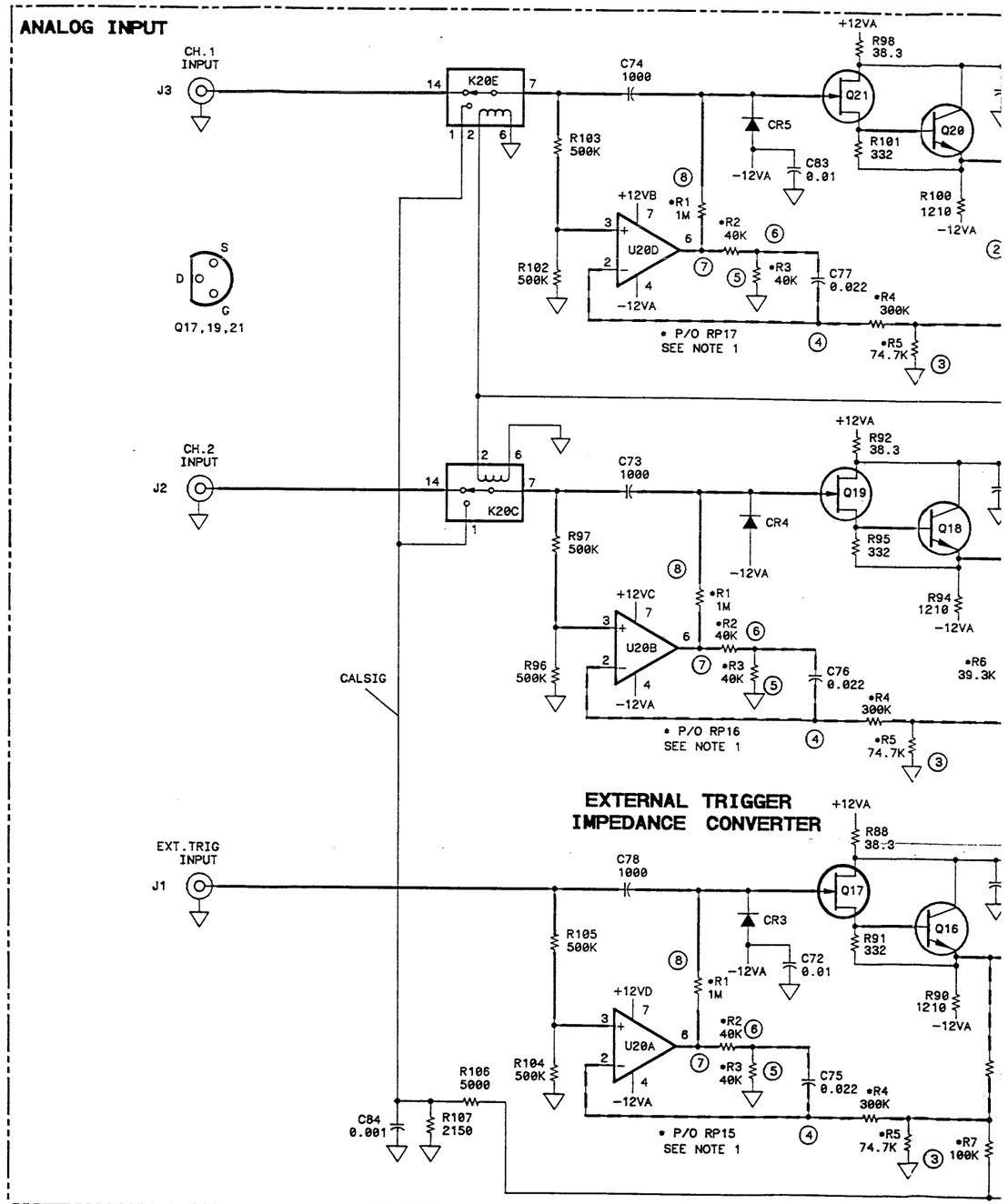




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	−5.2V
2–5 13,14	100X9	1	−2.4V
6–11	100X9	1	−2.4V

PARTS ON THIS SCHEMATIC

C48–52,54,55,60, 65–68,71–84 CR3–5 J1–3 K20C,E RP15–17 Q1–11,14–21	R2,3,28–34,37–43, 47–61,66,71,79, 81,82,84,85,88–107 P/O RP14 P/O U15E U7F,9F,17G,20A,20B, U20D



C DEVICE CONNECTIONS

	PIN NO.	IC GROUP
	1 16 8	U7F,15E

CK DESCRIPTIONS:

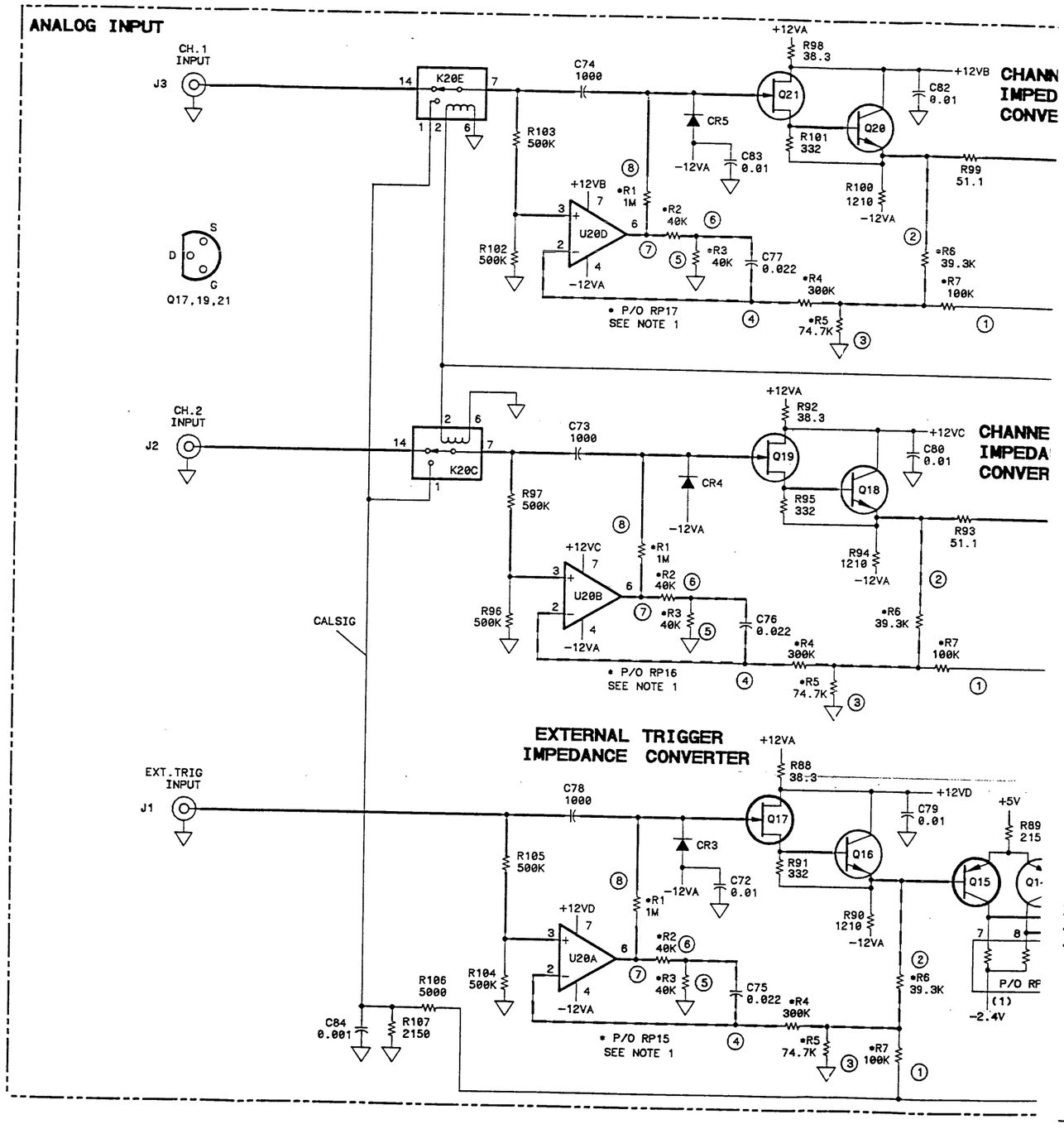
SEE RP VALUE TABLE FOR MORE INFORMATION

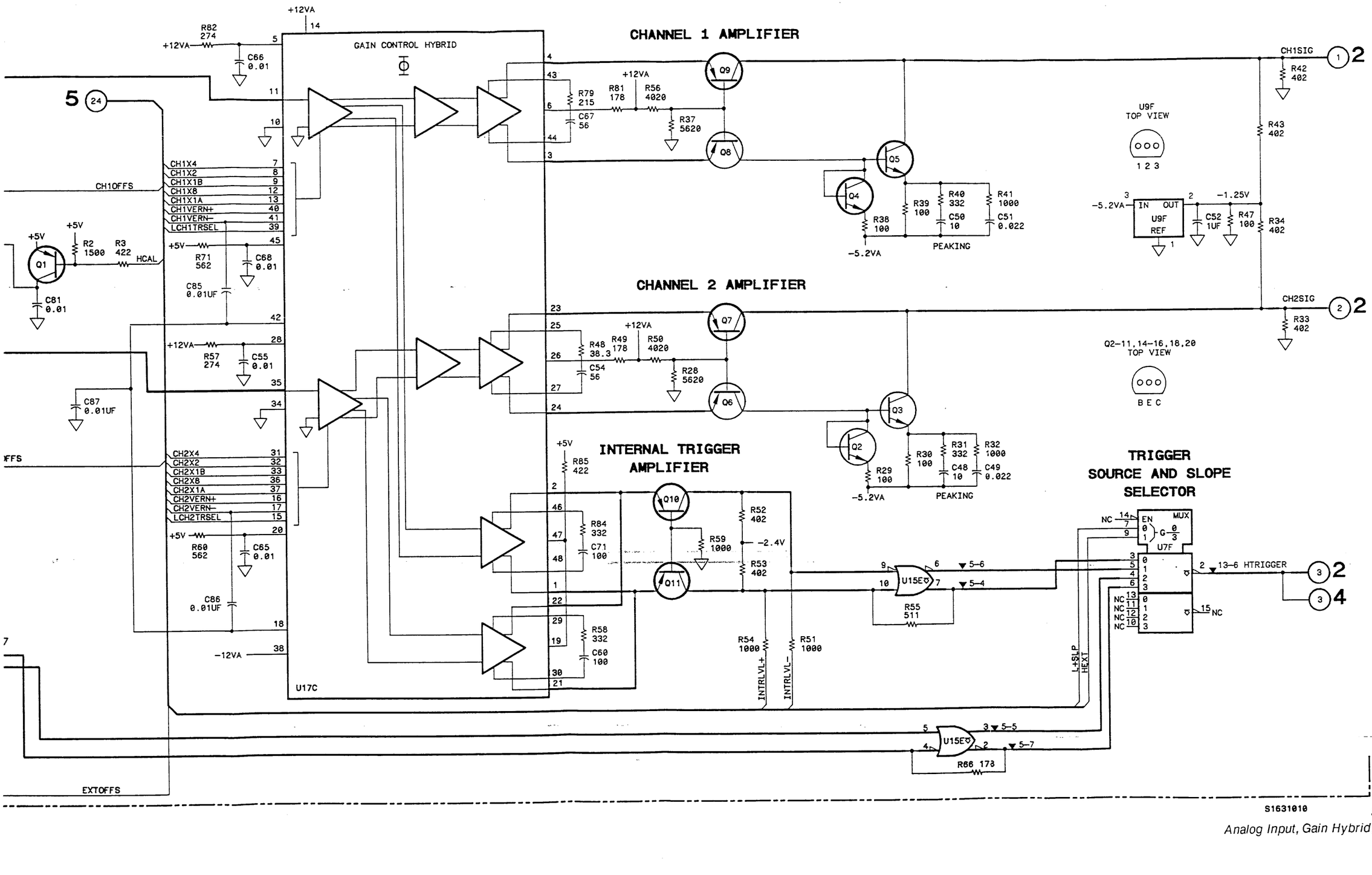
— PIN# OF RESISTOR PACK
· RESISTOR PACK NUMBER (RP)
ECL LINE BEING PULLED DOWN
L LINE BEING PULLED UP

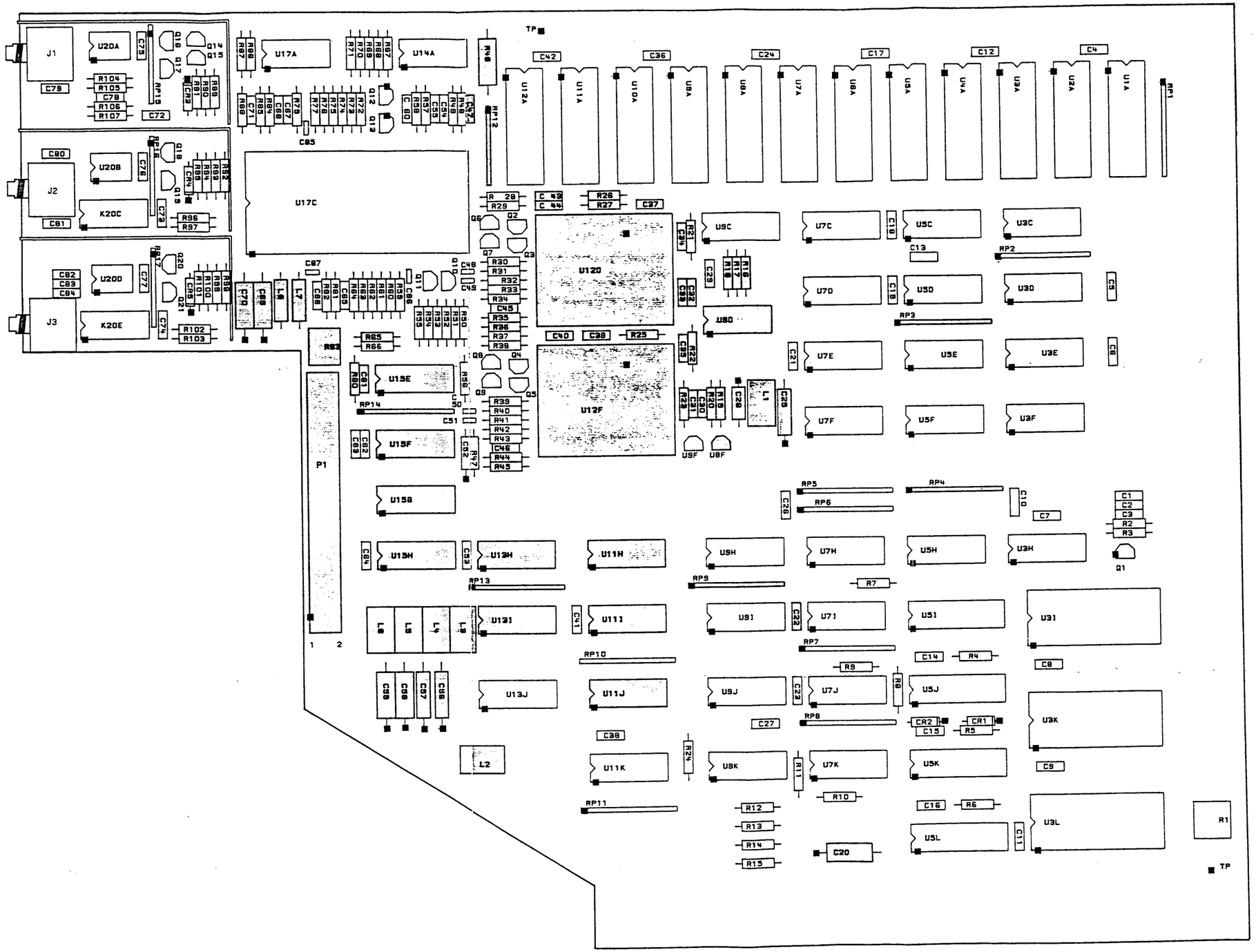
	RESISTOR VALUE	POWER PIN	VOLTAGE
	330X9	1	−5.2V
	100X9	1	−2.4V
4	100X9	1	−2.4V

THIS SCHEMATIC

0,	R2,3,28–34,37–43, 47–61,66,71,79, 81,82,84,85,88–107 P/O RP14 P/O U15E U7F,9F,17G,20A,20B, U20D




CHANNEL 1 AMPLIFIER
CHANNEL 2 AMPLIFIER
INTERNAL TRIGGER AMPLIFIER
TRIGGER SOURCE AND SLOPE SELECTOR
GAIN CONTROL HYBRID
+12VA
-12VA
-5.2VA
+5V
-2.4V
CH1SIG
CH2SIG
CH1OFFS
CH2OFFS
EXTOFFS
HCAL
PEAKING
U17C
U9F
U7F
U15E
U9F TOP VIEW
Q2-11,14-16,18,20 TOP VIEW
B E C
1 2 3
CH1X4
CH1X2
CH1X1B
CH1X8
CH1X1A
CH1VERN+
CH1VERN-
LCH1TRSEL
CH2X4
CH2X2
CH2X1B
CH2X8
CH2X1A
CH2VERN+
CH2VERN-
LCH2TRSEL
INTRLVL+
INTRLVL-
L+SLP
HEXT
13-6 HTRIGGER
R82 274
C66 0.01
R79 215
R81 178
R56 4020
R37 5620
C67 56
R42 402
R43 402
R34 402
R38 100
R39 100
R40 332
R41 1000
C50 10
C51 0.022
C52 1UF
R47 100
R2 1500
R3 422
C81 0.01
R71 562
C68 0.01
C85 0.01UF
R57 274
C55 0.01
C87 0.01UF
R48 38.3
R49 178
R50 4020
R28 5620
C54 56
R33 402
R29 100
R30 100
R31 332
R32 1000
C48 10
C49 0.022
R85 422
R84 332
C71 100
R59 1000
R52 402
R53 402
R54 1000
R51 1000
R58 332
C60 100
R60 562
C65 0.01
C86 0.01UF
R55 511
R66 173
R89 215



Component Locator for Schematic 8G-2

NOTE 1

Resistor R17 is 3480Ω on early boards. It was changed to 4420Ω to optimize bias for the ADC. The latter is the preferred part and should be used for all resistor replacements. It should also be checked, and if necessary changed to 4420Ω, if the ADC is replaced. See section 7.

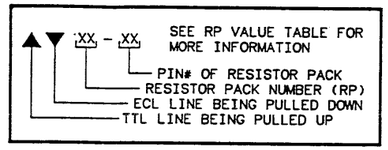
IC DEVICE POWER CONNECTIONS

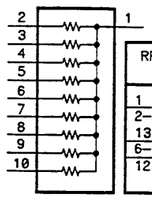
SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U11H-J,13H,13I, U15E-H

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:





RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	-5.2V
2-5 13,14	100X9	1	-2.4V
6-11	100X9	1	-2.4V
12	51X7	1	*

*ABOUT -1.9V DROPPED THROUGH R46

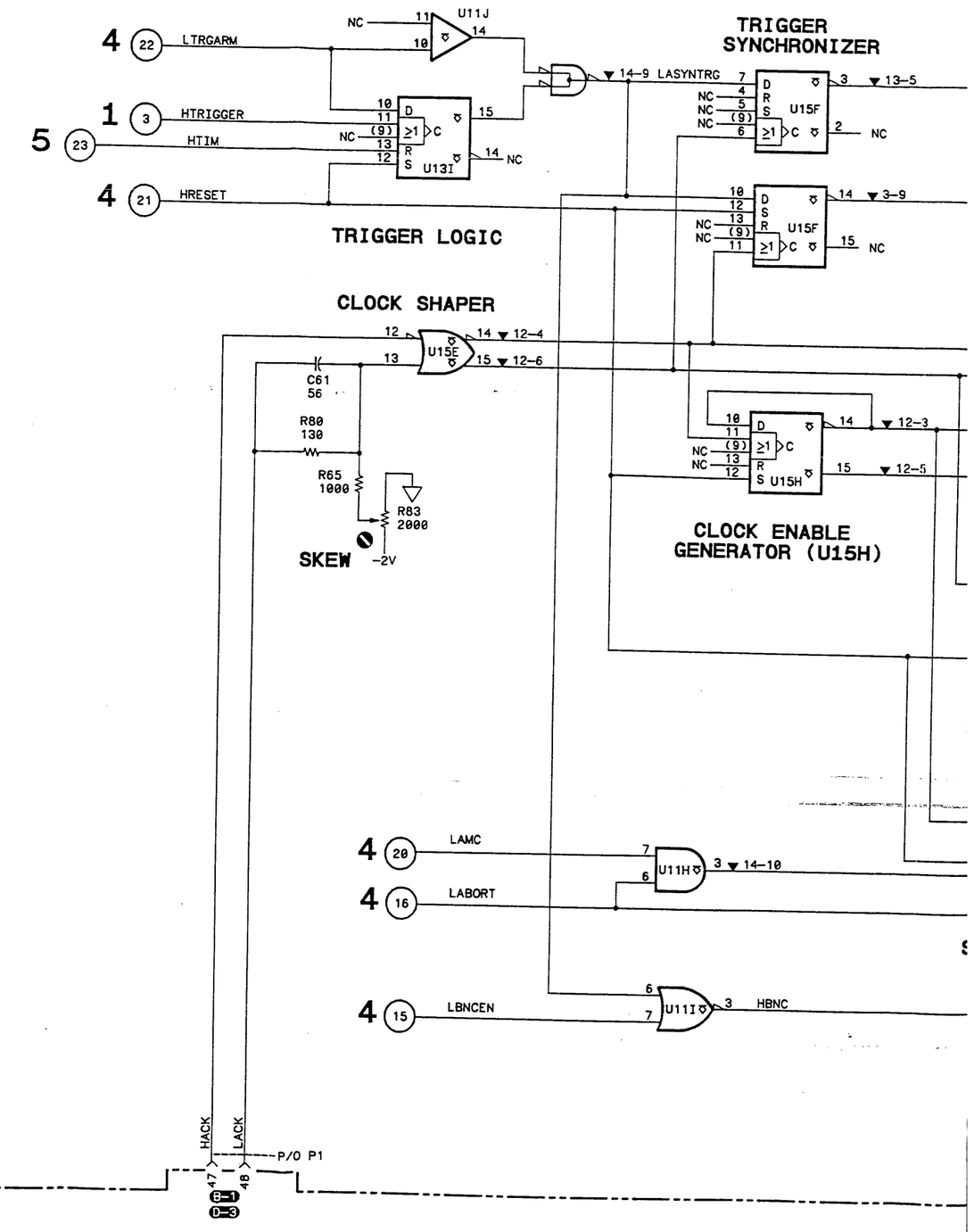
PARTS ON THIS SCHEMATIC

C28,30-35,37,39,40, 43-46,61 P/O P1 R16-23,25-27,35,36, 44,45,65,80,83	P/O RP3,4,9,12,13,14 U8F,9D,12D,12F, U13H,15F-H P/O U11H-J,13I,15E

POWER SUPPLY DISTRIB. PARTS ON THIS SCHEMATIC

C1-7,10,12,17-27, 29,36,41,42,47,51, 56-59,62-64,69,70 L1-8 R46 U15E	

ANALOG TO DIGITAL



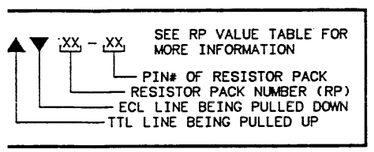
IC DEVICE POWER CONNECTIONS

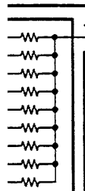
SUPPLY	PIN NO.	IC GROUP
GND	1	U11H-J,13H,13I,
GND	16	U15E-H
-5.2V	8	

NOTES:

GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:





RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	-5.2V
2-5 13,14	100X9	1	-2.4V
6-11	100X9	1	-2.4V
12	51X7	1	*

*ABOUT -1.9V DROPPED THROUGH R46

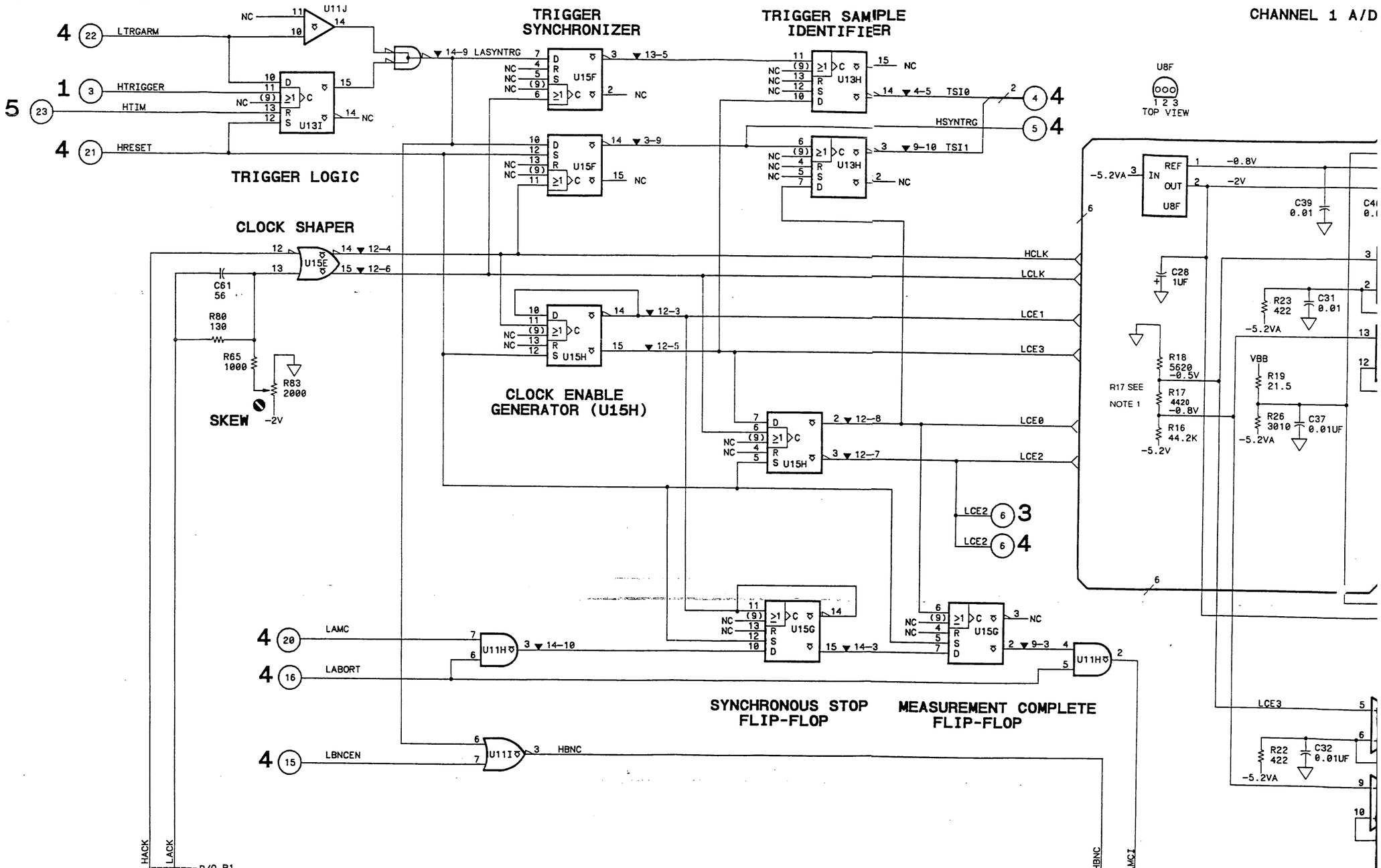
PARTS ON THIS SCHEMATIC

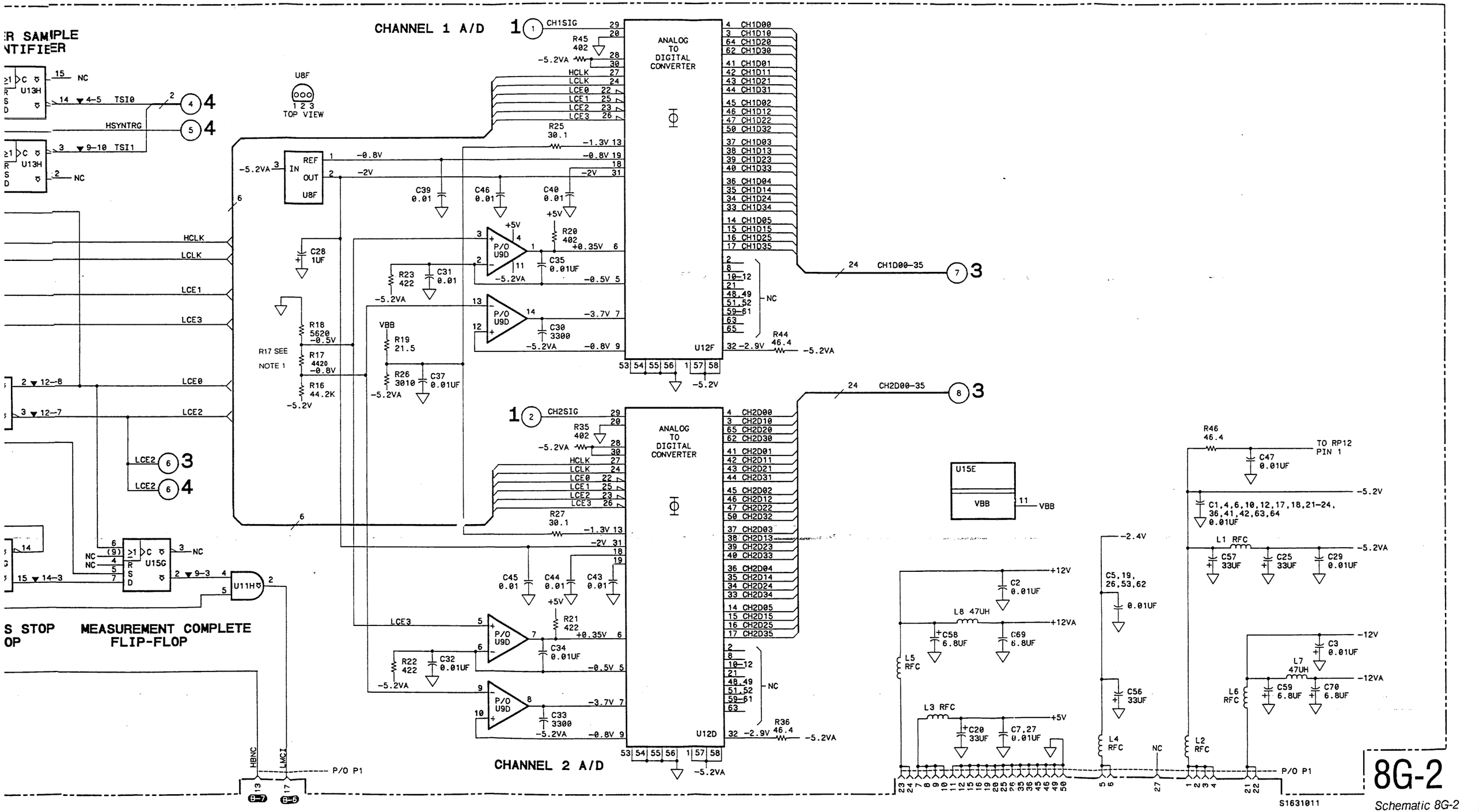
C28,30-35,37,39,40, 43-46,61	P/O RP3,4,9,12,13,14
P/O P1	U8F,9D,12D,12F,
R16-23,25-27,35,36, 44,45,65,80,83	U13H,15F-H
	P/O U11H-J,13I,15E

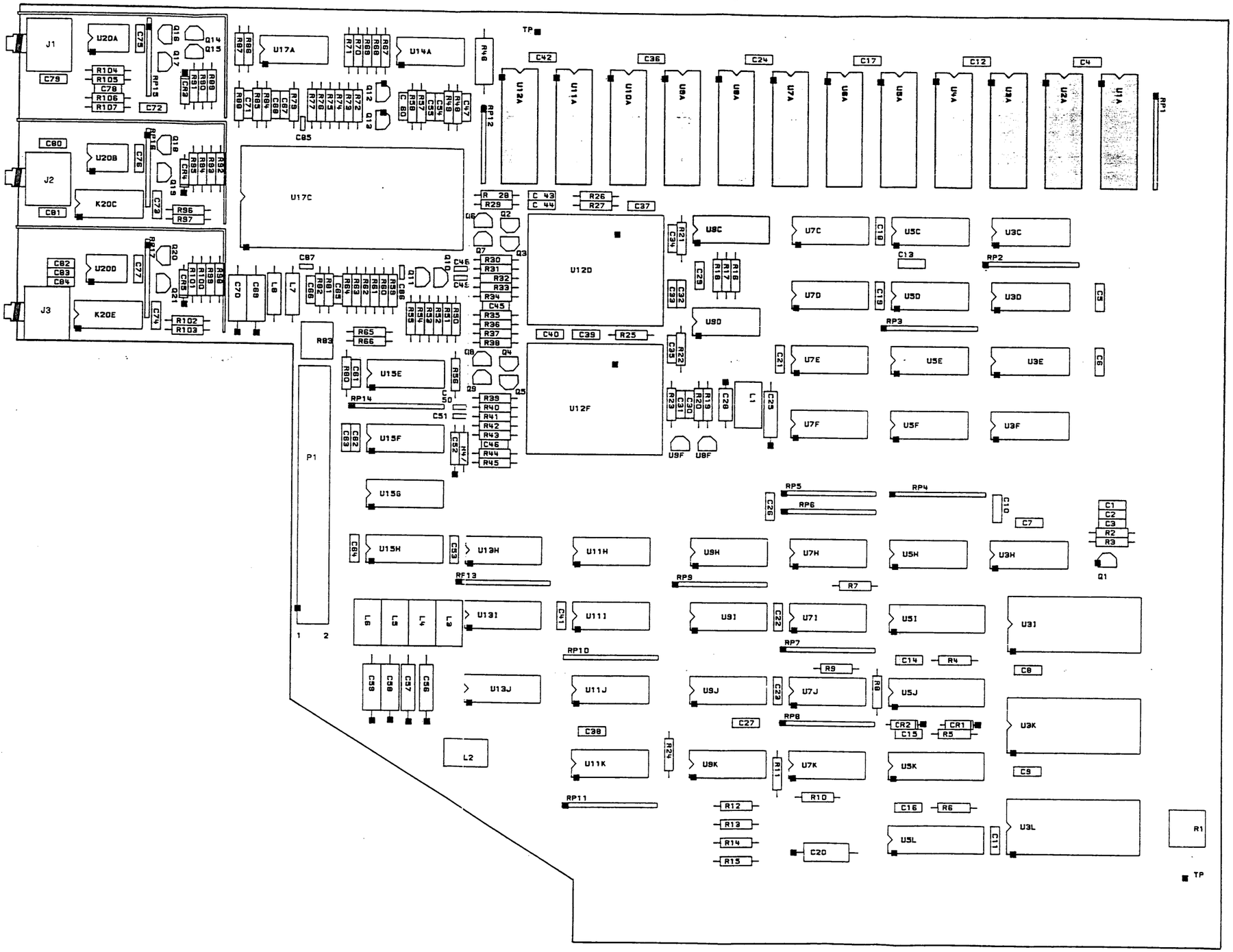
POWER SUPPLY DISTRIB. PARTS ON THIS SCHEMATIC

C1-7,10,12,17-27, 29,36,41,42,47,51, 56-59,62-64,69,70	
L1-8	
R46	
U15E	

ANALOG TO DIGITAL




CHANNEL 1 A/D
CHANNEL 2 A/D
ANALOG TO DIGITAL CONVERTER
U12F
U12D
U8F
TOP VIEW
REF
IN
OUT
P/O U9D
R45 402
R25 30.1
R20 402
R23 422
C31 0.01
C35 0.01UF
R18 5620
R17 4420
R16 44.2K
R19 21.5
R26 3010
C37 0.01UF
C30 3300
R35 402
R27 30.1
R21 422
R22 422
C32 0.01UF
C34 0.01UF
C33 3300
R44 46.4
R36 46.4
C28 1UF
C39 0.01
C46 0.01
C40 0.01
C45 0.01
C44 0.01
C43 0.01
U15E
VBB
U15G
U11H
R46 46.4
C47 0.01UF
C1,4,6,10,12,17,18,21-24, 36,41,42,63,64 0.01UF
L1 RFC
C57 33UF
C25 33UF
C29 0.01UF
C2 0.01UF
L8 47UH
C58 6.8UF
C69 6.8UF
L5 RFC
C5,19, 26,53,62 0.01UF
C56 33UF
L4 RFC
L3 RFC
C20 33UF
C7,27 0.01UF
C3 0.01UF
L7 47UH
C59 6.8UF
C70 6.8UF
L6 RFC
L2 RFC
CH1SIG
CH2SIG
HCLK
LCLK
LCE0
LCE1
LCE2
LCE3
HSYNTRG
TSI0
TSI1
CH1D00-35
CH2D00-35
NC
TO RP12 PIN 1
P/O P1
HBNC
LMCT
R17 SEE NOTE 1
-5.2VA
-5.2V
+5V
+12V
-12V
-2.4V
+12VA
-12VA
+0.35V
-0.5V
-3.7V
-0.8V
-2V
-1.3V
-2.9V
S STOP
OP
MEASUREMENT COMPLETE FLIP-FLOP
S1631011



Component Locator for Schematic 8G-3

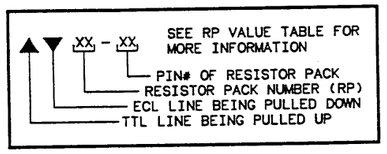
IC DEVICE POWER CONNECTIONS

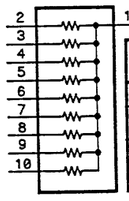
SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 24 12	U1A,2A,3A,4A, 5A,6A,7A,8A,9A, U10A,11A,12A
GND GND -5.2V	1 16 8	U9C

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:



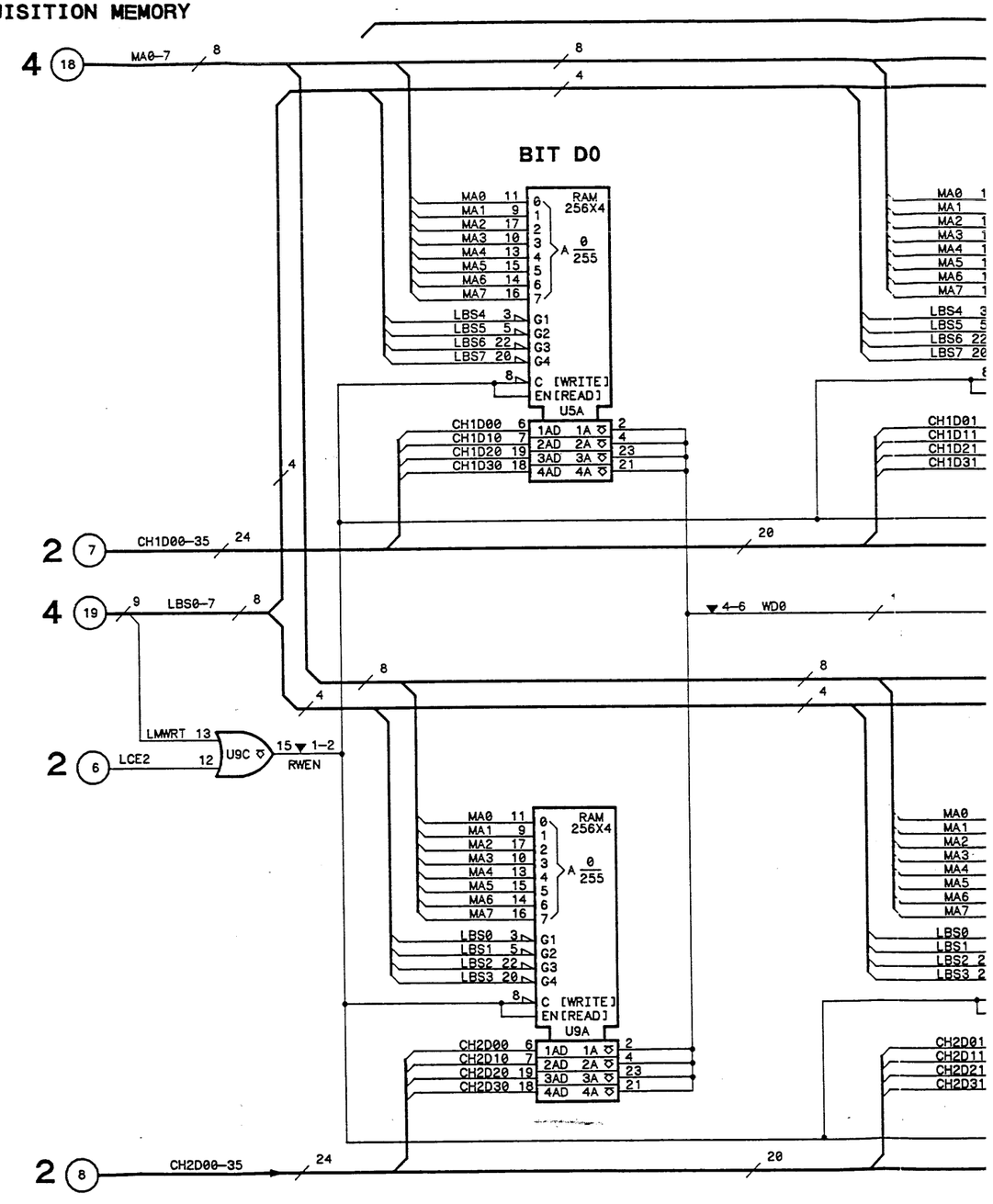


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	-5.2V
2-5 13,14	100X9	1	-2.4V
6-11	100X9	1	-2.4V

PARTS ON THIS SCHEMATIC

P/O RP1,4 U1A,2A,3A,4A,5A,6A U7A,8A,9A,10A,11A, U12A P/O U9C	

ACQUISITION MEMORY



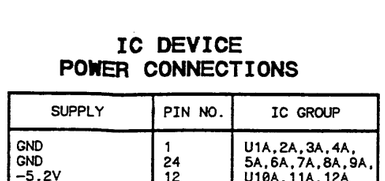
IC DEVICE POWER CONNECTIONS

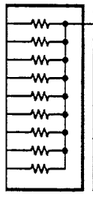
SUPPLY	PIN NO.	IC GROUP
GND GND −5.2V	1 24 12	U1A,2A,3A,4A, 5A,6A,7A,8A,9A, U10A,11A,12A
GND GND −5.2V	1 16 8	U9C

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:

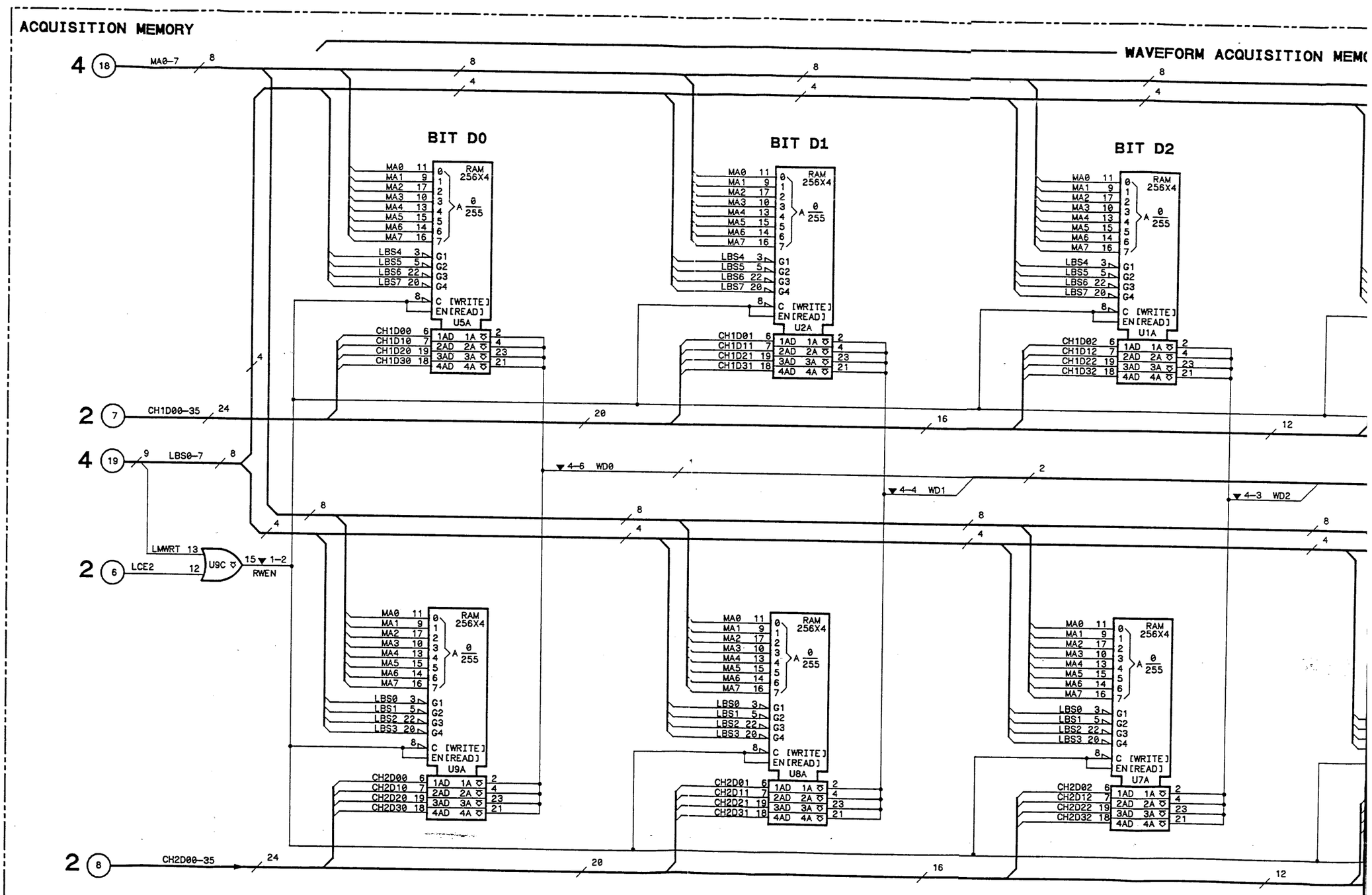




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	−5.2V
2−5 13,14	100X9	1	−2.4V
6−11	100X9	1	−2.4V

PARTS ON THIS SCHEMATIC

P/O RP1,4 U1A,2A,3A,4A,5A,6A U7A,8A,9A,10A,11A, U12A P/O U9C	



WAVEFORM ACQUISITION MEMORY

BIT D2

BIT D3

BIT D4

BIT D5

RAM 256X4

U1A · U3A · U4A · U6A · U7A · U10A · U12A · U11A

MA0 11, MA1 9, MA2 17, MA3 10, MA4 13, MA5 15, MA6 14, MA7 16

LBS4 3, LBS5 5, LBS6 22, LBS7 20

C [WRITE] EN [READ]

CH1D02 6, CH1D12 7, CH1D22 19, CH1D32 18

CH1D03 6, CH1D13 7, CH1D23 19, CH1D33 18

CH1D04 6, CH1D14 7, CH1D24 19, CH1D34 18

CH1D05 6, CH1D15 7, CH1D25 19, CH1D35 18

1AD 1A, 2AD 2A, 3AD 3A, 4AD 4A

CH2D02 6, CH2D12 7, CH2D22 19, CH2D32 18

CH2D03 6, CH2D13 7, CH2D23 19, CH2D33 18

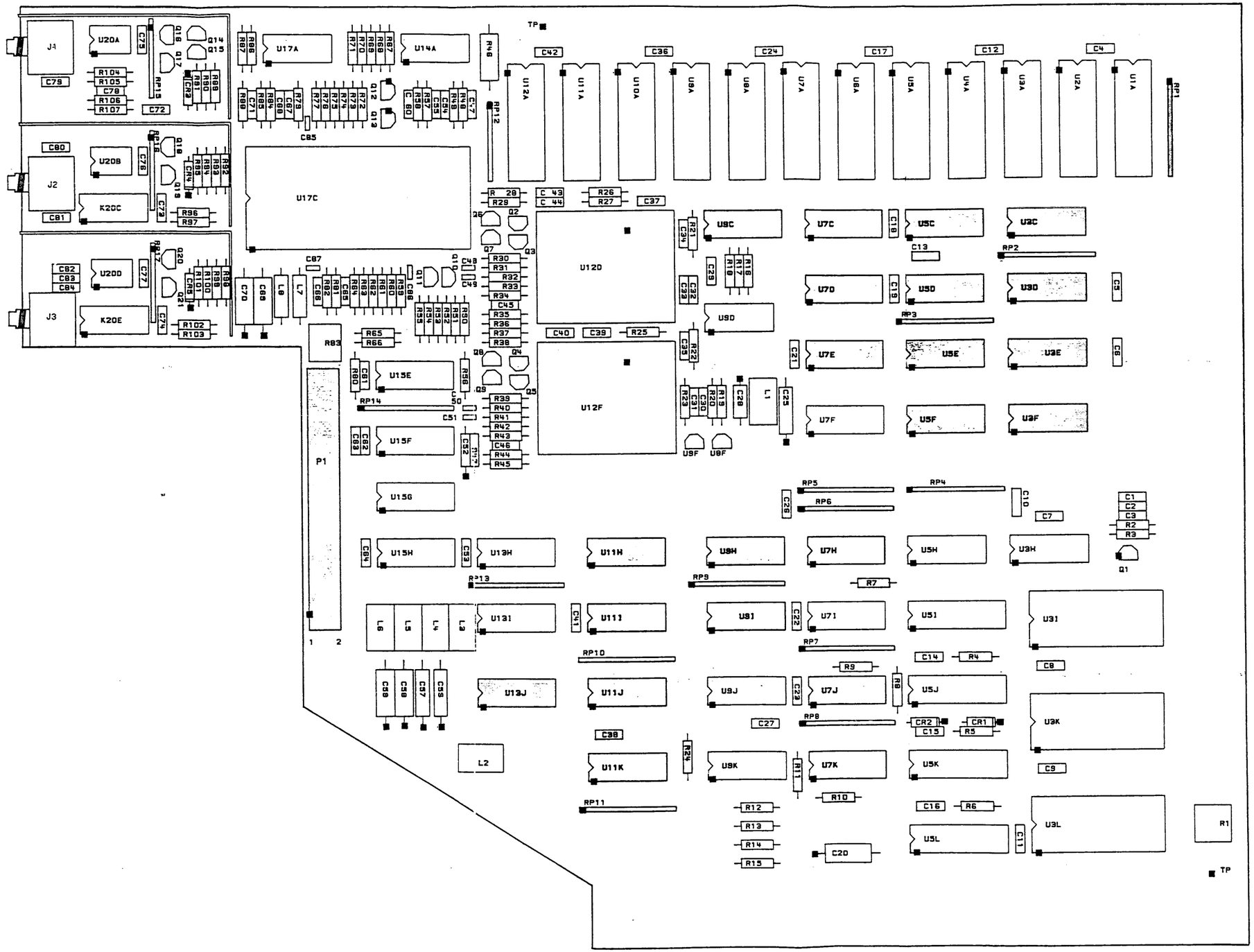
CH2D04 6, CH2D14 7, CH2D24 19, CH2D34 18

CH2D05 6, CH2D15 7, CH2D25 19, CH2D35 18

LBS0 3, LBS1 5, LBS2 22, LBS3 20

4–4 WD1 · 4–3 WD2 · 4–2 WD3 · 4–8 WD4 · 4–10 WD5 · WD0–5

S1631001



Component Locator for Schematic 8G-4

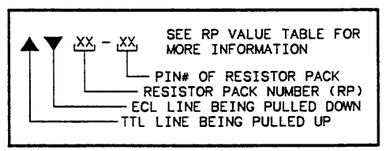
IC DEVICE POWER CONNECTIONS

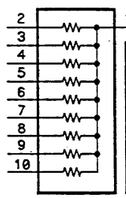
SUPPLY	PIN NO.	IC GROUP
GND GND -5.2V	1 16 8	U3C–E,5C–E, U7C–E,7H,7J,7K, U9C,9H,9I,11H–K, U13J
GND -5.2V	16 8	U3F,5F

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:

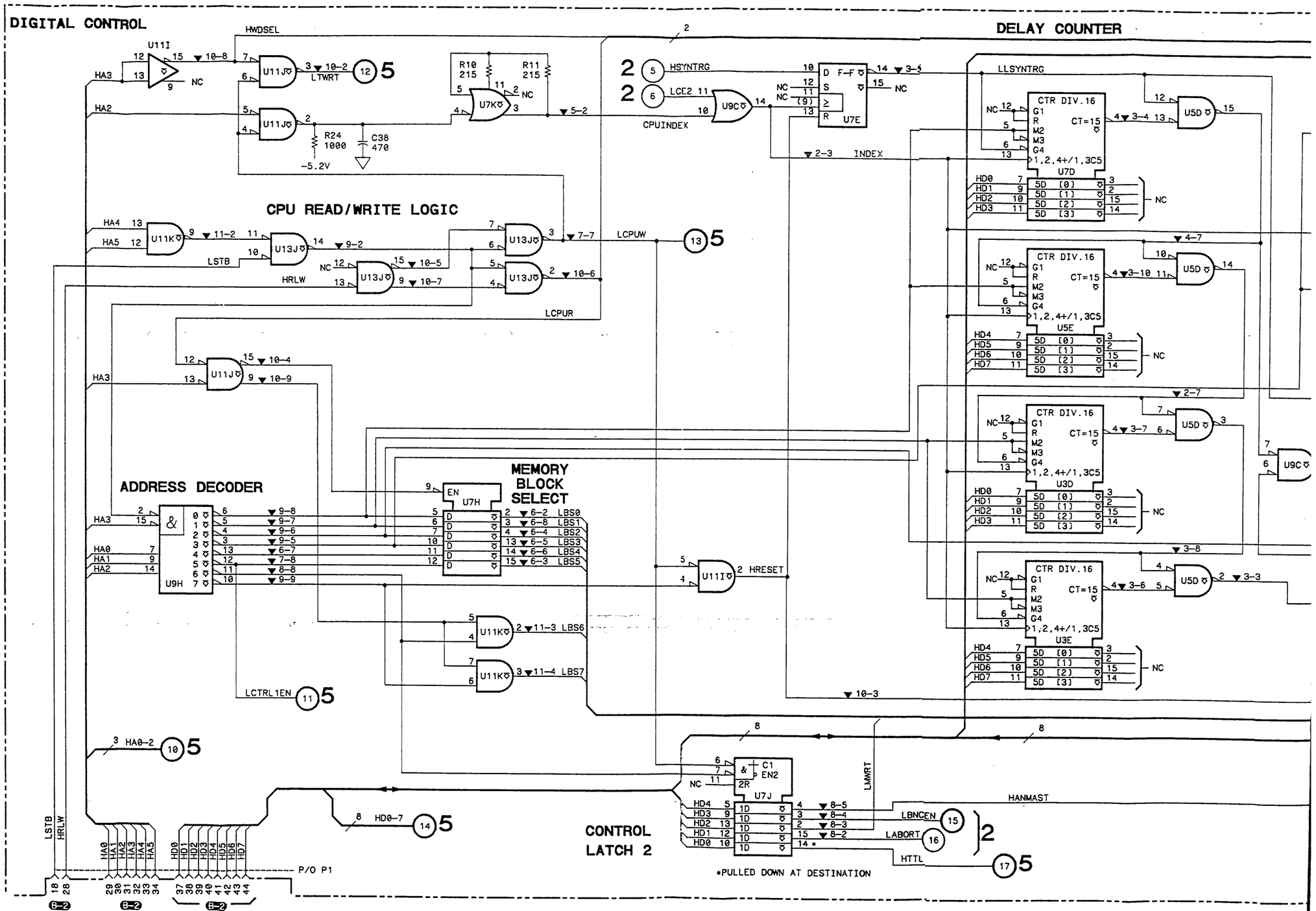




RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	-5.2V
2–5 13,14	100X9	1	-2.4V
6–11	100X9	1	-2.4V

PARTS ON THIS SCHEMATIC

C13,38 P/O P1 R7,10,11,24 P/O RP1–11,13	U3C–F,5C–F,7C–E, U7H,7J,9H,9I,13J P/O U7K,9C,11H–K



DELAY COUNTER

MEMORY ADDRESS COUNTERS

POSTSTORE COUNTER

TRACEPOINT LATCH FLIP-FLOP

WAVEFORM ACQUISITION MEMORY

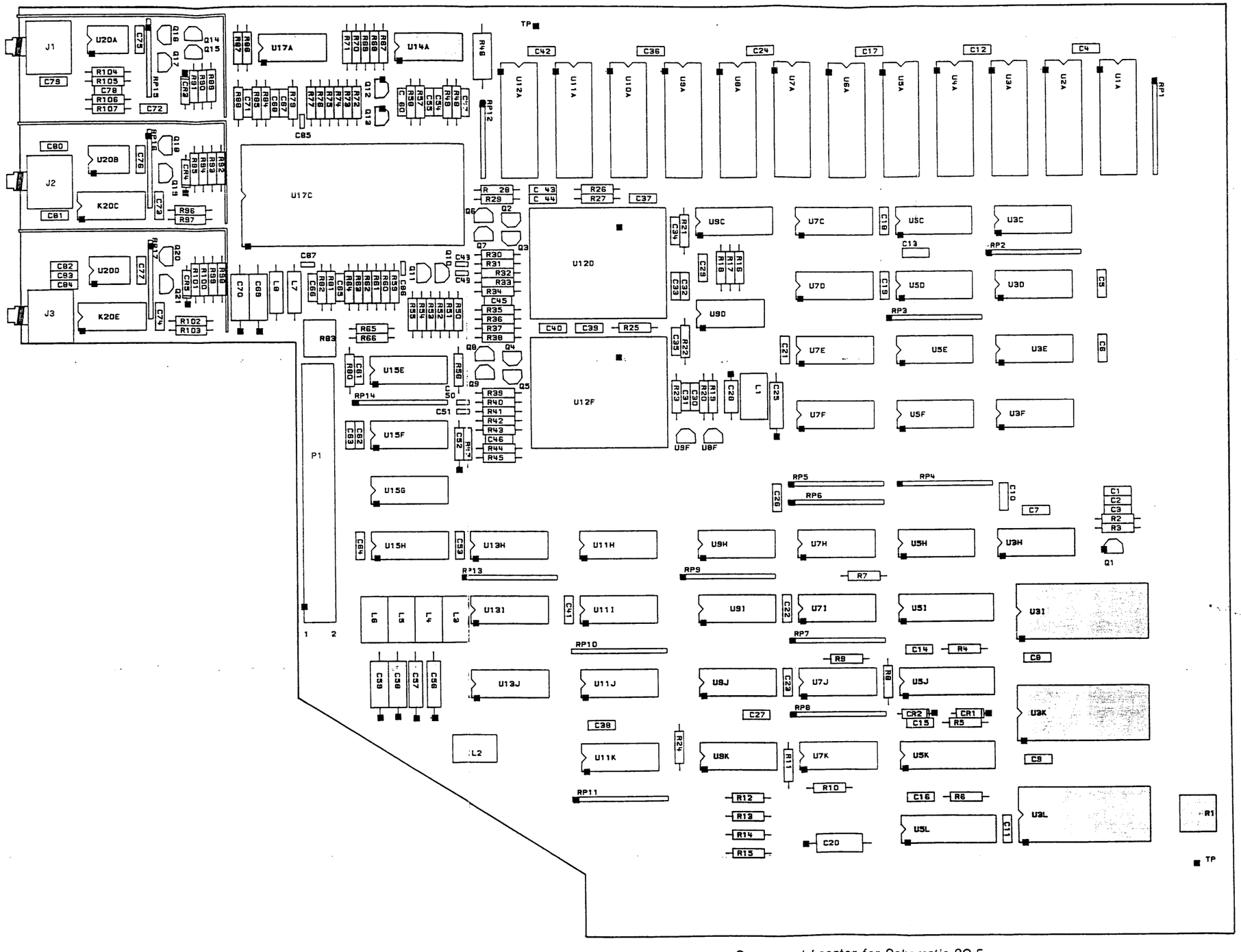
SCHEMATIC 8F-3

OUTPUT DATA SELECTORS

PRESTORE VALID FLIP-FLOP

MEMORY FULL FLIP-FLOP

ARMING LOGIC



Component Locator for Schematic 8G-5

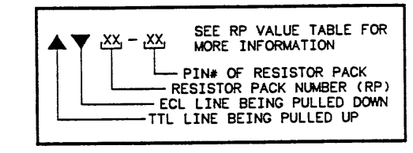
IC DEVICE POWER CONNECTIONS

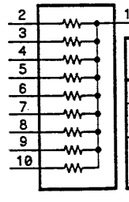
SUPPLY	PIN NO.	IC GROUP
GND GND −5.2V	1 16 8	U7I
GND +5V	10 20	U5I
GND +5V −5.2V	8 9 16	U3H,5H,9J
GND +5V	8 16	U9K

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.

RESISTOR PACK DESCRIPTIONS:



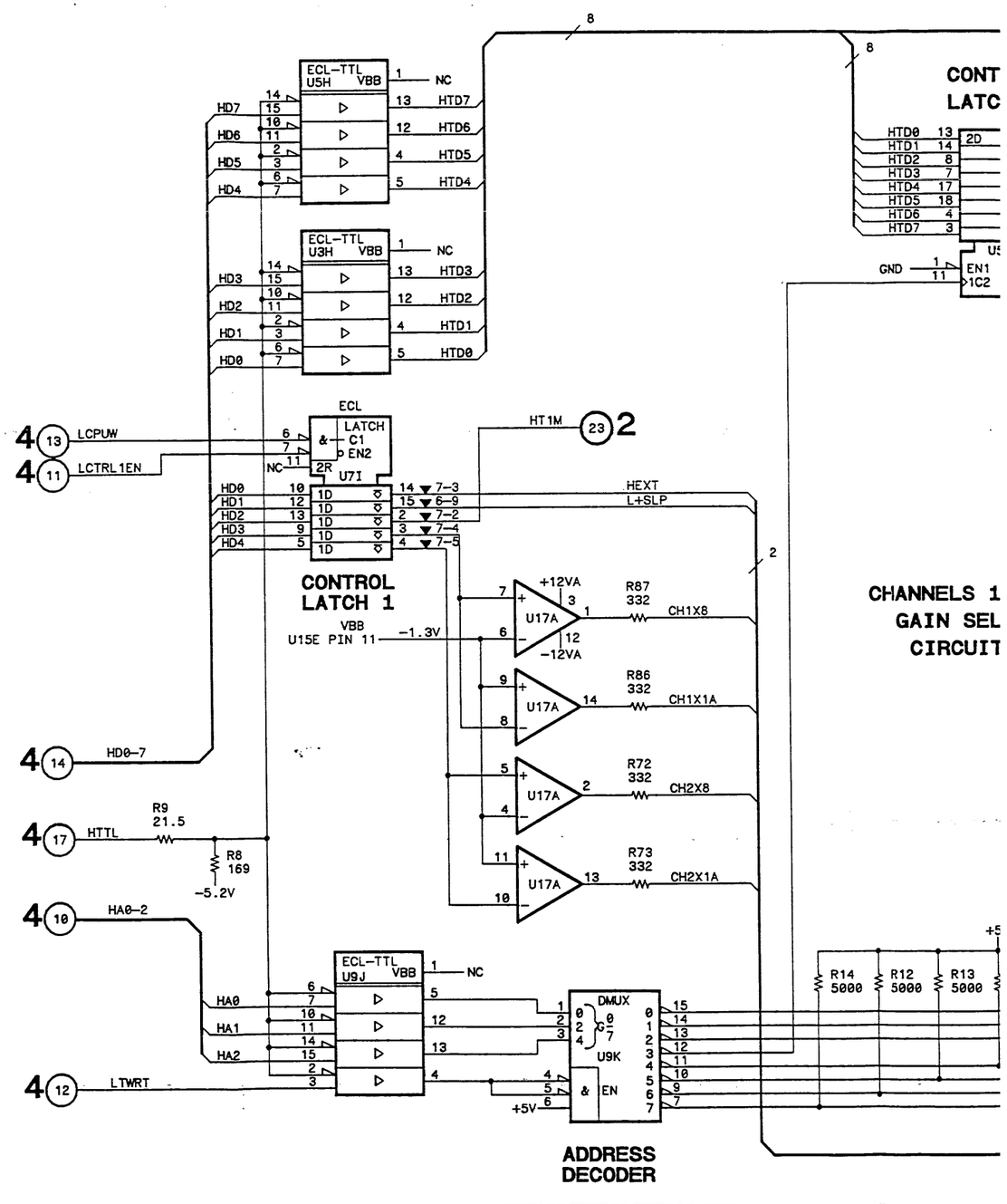


RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
1	330X9	1	−5.2V
2−5 13,14	100X9	1	−2.4V
6−11	100X9	1	−2.4V

PARTS ON THIS SCHEMATIC

C8,9,11,14−16 CR1,2 Q12,13 R1,4−6,8,9,12−15, 61−64,67−70,72−77 86,87	U3H−L,5H−L,7I,9J, 9K,14A,17A

ANALOG CONTROL



C DEVICE
CONNECTIONS

	PIN NO.	IC GROUP
	1 16 8	U7I
	10 20	U5I
	8 9 16	U3H,5H,9J
	8 16	U9K

SYMBOLIZED ACCORDING TO
NCTION.

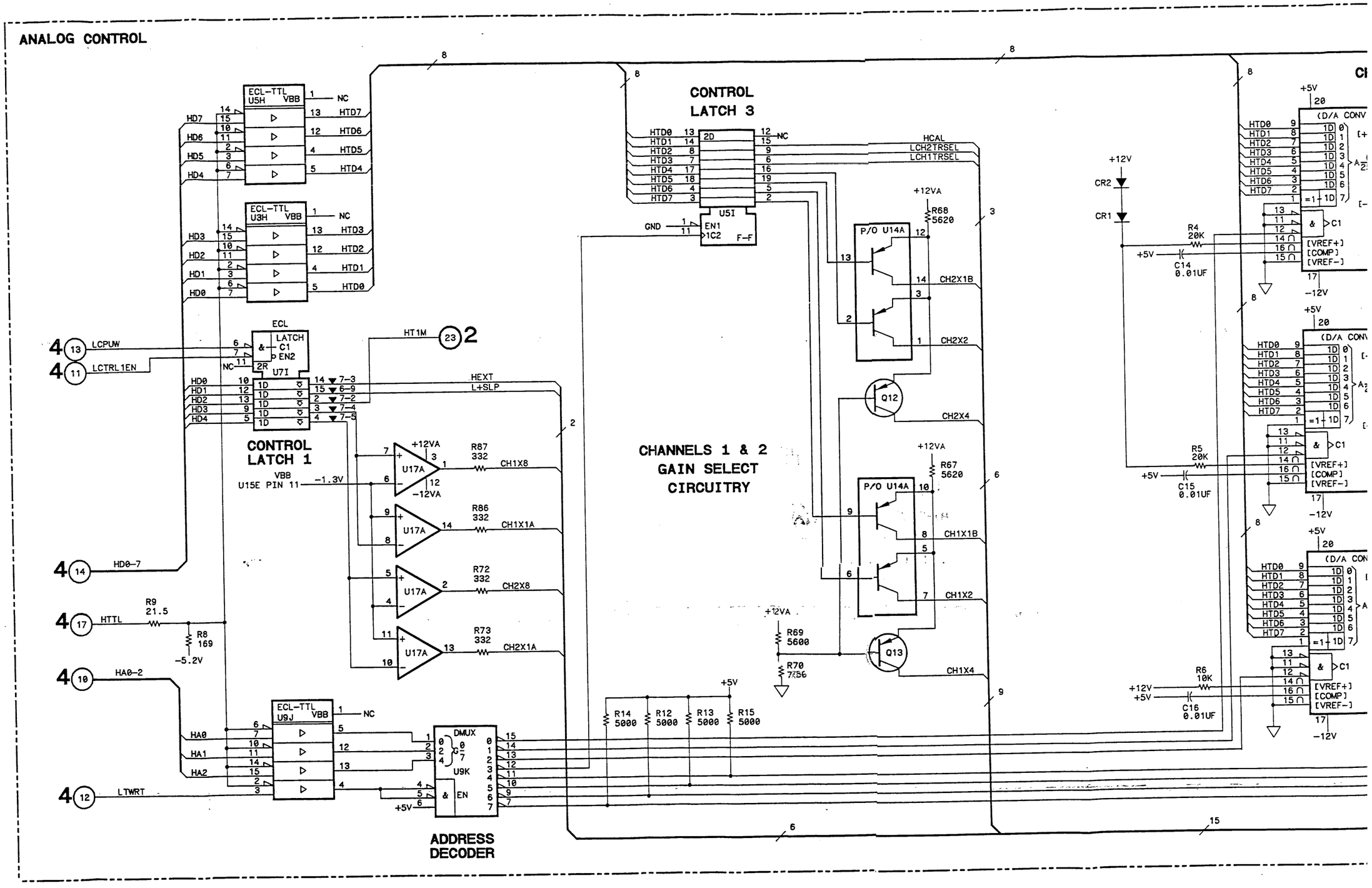
ACK DESCRIPTIONS:

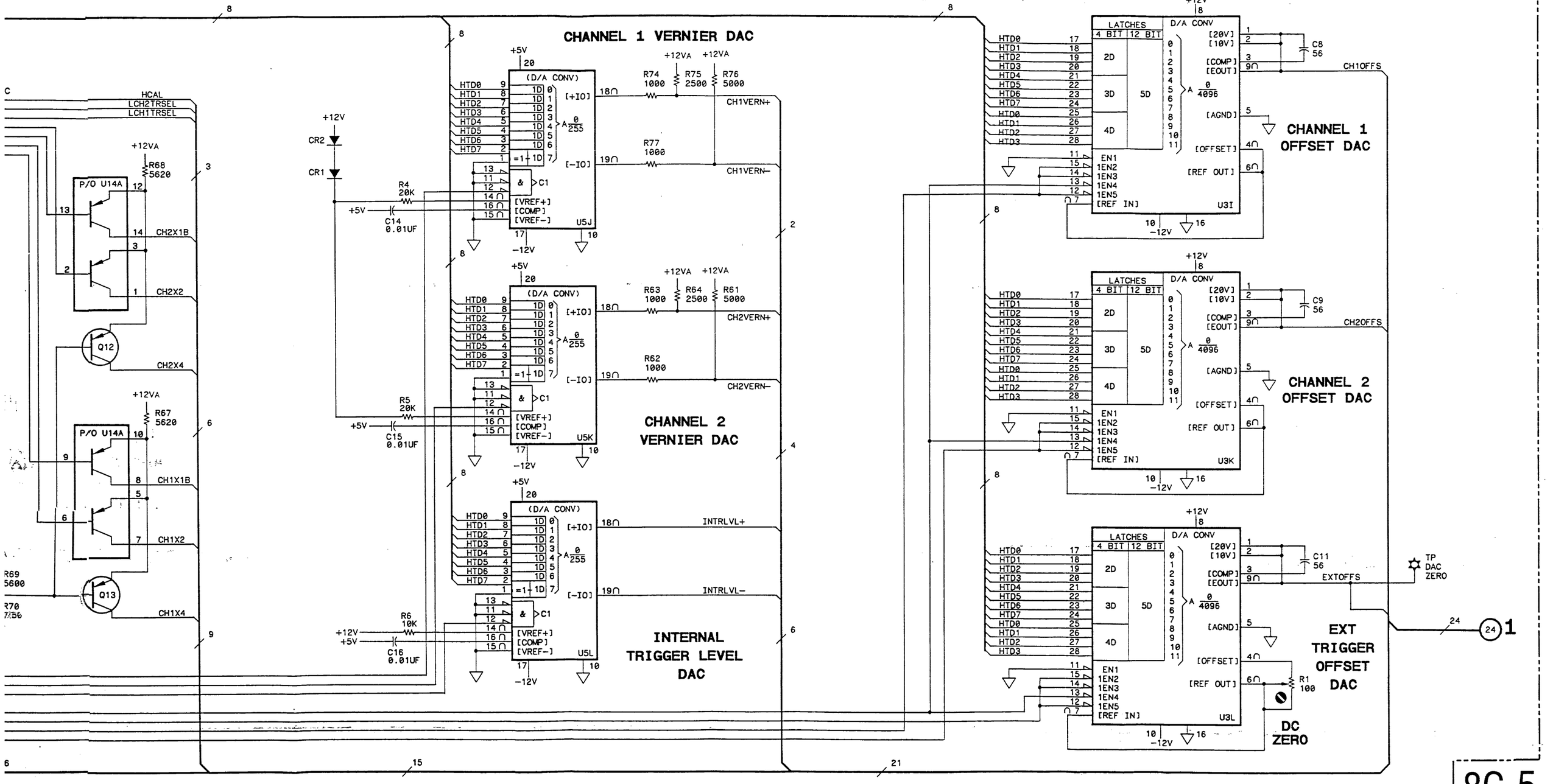
XX SEE RP VALUE TABLE FOR MORE INFORMATION
PIN# OF RESISTOR PACK
RESISTOR PACK NUMBER (RP)
ECL LINE BEING PULLED DOWN
TTL LINE BEING PULLED UP

RP#	RESISTOR VALUE	POWER PIN	VOLTAGE
	330X9	1	-5.2V
-5 3,14	100X9	1	-2.4V
-11	100X9	1	-2.4V

ON THIS SCHEMATIC

-16	U3H-L,5H-L,7I,9J, 9K,14A,17A
,12-15, 0,72-77	





S1631014

Schematic 8G-5
Analog Control, DACs
8G-31/(8G-32 blank)

Appendix A Table of Contents

Paragraph		Page
A-1.	Introduction	A-1
A-2.	Guided Probe Troubleshooting - General Information	A-1
A-3.	1630A/D and 1631A/D Troubleshooting Summary	A-2
A-4.	1630G Troubleshooting Summary	A-4
A-5.	Program Disk Loading Procedure	A-5
A-6.	Operation Verification	A-7
A-7.	Hardware Configuration	A-7
A-8.	Running the Tests	A-7
A-9.	Acquisition Verification; Test #9, Failures	A-8
A-10.	Guided Probe	A-9
A-11.	Hardware Configuration	A-9
A-12.	Running the Tests	A-10
A-13.	Common Adjustments	A-10
A-14.	Hardware Configuration	A-10
A-15.	Running the Tests	A-11
A-16.	1630G, State Slave Board Test and Adjustment	A-11
A-17.	1631A/D, Analog Board Adjustment and Function Tests	A-12
A-18.	1630A/D/G, 1631A/D Performance Checks	A-12

List of Illustrations

Figure		Page
A-1.	1630A/D, 1631A/D Troubleshooting Flow-Chart	A-2
A-2.	1630G Troubleshooting Flow-Chart	A-4

NOTES

APPENDIX A
1630A/D/G, 1631A/D
REPAIR AND VERIFICATION PROCEDURES

A-1. INTRODUCTION

This section consists of the Operation, Guided Probe, and Calibration tests that are downloaded into the logic analyzer via a controller. Operation Verification tests determine which subsystem is faulty (CPU or Acquisition). Guided Probe tests determine which node is bad in the faulty subsystem. The remaining tests are used for Timing and State calibration adjustments in Section V (Adjustments) of this manual. Note that all tests are stored on disk and are written in BASIC.

NOTE

For complete Performance Testing of the logic analyzer perform the Operation Verification Tests in this Appendix, the Parametric Verification Tests in the ET19776 Manual, and the Timing and State calibration adjustments in Section V of this manual.

A-2. GUIDED PROBE TROUBLESHOOTING

The main program allows either Operation Verification or Guided Probing on the subsystem level. System verification is accomplished by executing Operation Verification tests on the CPU and Acquisition subsystems. In the Operation Verification mode, the actual tests are downloaded into the logic analyzer under test over HP-IB from the controller. The controller then instructs the logic analyzer to begin execution of the Operation Verification tests, <ACQvfy> (a single pass or continuous execution can be specified). If a failure is encountered, the program displays the test number that failed. At this point, the failure is isolated to the board level through the results of <ACQvfy>.

Once a failure is isolated to a board, then the Single Board Guided Probe, <GPROBE>, function is selected. The board in question is loaded into the logic analyzer service slot, a right angle connector on the top end of the motherboard. (IMPORTANT: A fan must be used to keep air moving across the PC boards that are under test in the service slot.) Then the functional tests are downloaded into the logic analyzer and run until the hard failure is isolated. The particular test that failed is then run repetitively and the program references signature databases (additional files on the disk) and indicates where to begin probing. Both the topology of the board and nodal information are contained in the signature database files. The controller steps through the database, comparing the actual signatures measured with the information found in the database.

If a bad node is found, the program prompts the user to begin checking all related inputs. If one of those inputs is found to be bad, the program will "re-define" the current bad node and continue checking all related inputs for the most recent bad node. When all inputs are determined to be good, the bad node has been isolated. At this point, as with standard signature analysis, the actual part must be isolated since either a driver or receiver could be at fault. If the node includes wired-ORs, then a current probe and possibly a logic pulser can be used to isolate the failed part.

Provisions are also made in the probing program to determine if the failure includes a group of ICs. This may occur, for example, if a feedback loop has not been broken in the design implementation of signature analysis. In this case, the controller will indicate all inputs to the component group; then the actual bad component in the group must be determined by conventional troubleshooting methods. However, it is important to note that

if a Guided Probe session is begun anywhere except the beginning of a test loop, then the complete nodal history may not be available.

A-3. 1630A/D, 1631A/D TROUBLESHOOTING SUMMARY

The following flow chart and text summarizes troubleshooting of the 1630A/D and 1631A/D. Numbers on the chart correspond to numbers for the text on the adjacent page.

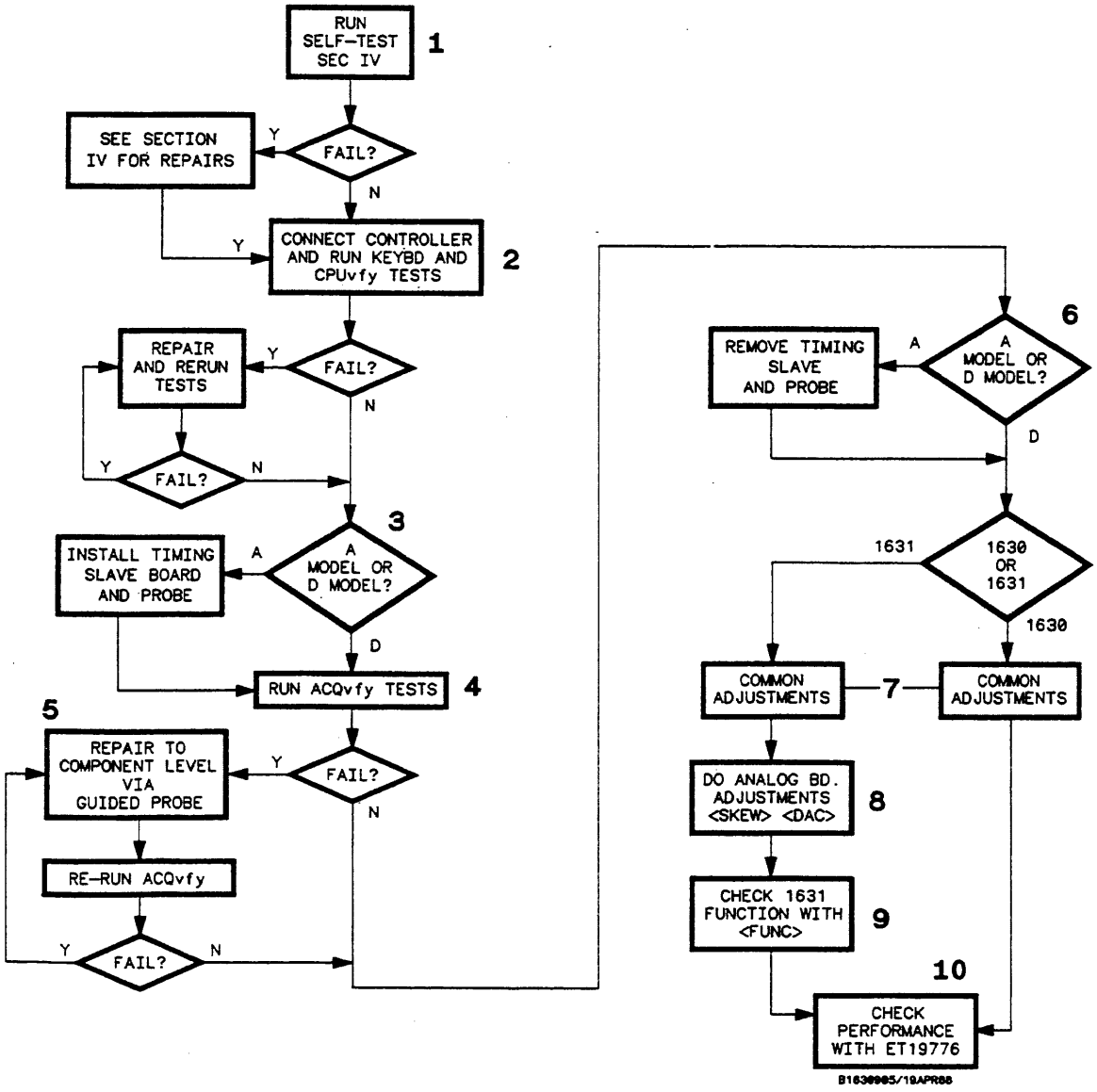


Figure A-1. 1630A/D, 1631A/D Troubleshooting Flow Chart.

Summary Description

1. RUN SELF-TEST — This is described in Section IV, paragraph 4-3.

2. CONNECT CONTROLLER... — This is described in paragraph A-7 and A-8.

3. INSTALL TIMING SLAVE... — Install a Timing Slave board and probe to convert the instrument to a "D" model (paragraph A-8). Assembly removal and installation instructions are in Section VIII.

4. RUN < ACQvfy > TESTS — Paragraphs A-8 and A-9 and the software cover these tests.

5. Guided Probe — Paragraph A-10 and the software cover these tests.

6. Reconvert instrument — If applicable, convert instrument from a "D" model back to it's original model. Assembly removal and installation instructions are in Section VIII.

7. COMMON ADJUSTMENTS — Make the adjustments common to all family models (paragraph A-13).

8. ANALOG BOARD ADJUSTMENTS — If the instrument is a 1631A/D make the Analog board adjustments, <SKEW> and <DAC> (paragraph A-17).

9. 1631A/D PERFORMANCE — If the instrument is a 1631A/D, applicable function check prodedures, <FUNC>, are covered in paragraph A-17. (If performance verification is necessary, see Appendix C.)

10. COMMON PERFORMANCE — The performance checks for the State and Timing subsystems are covered in software using the ET19776 1630A/D Test Tool (paragraph A-18).

A-4. 1630G TROUBLESHOOTING SUMMARY

The following flow chart and text summarizes troubleshooting of the 1630G. Numbers on the chart correspond to numbers for the text on the adjacent page.

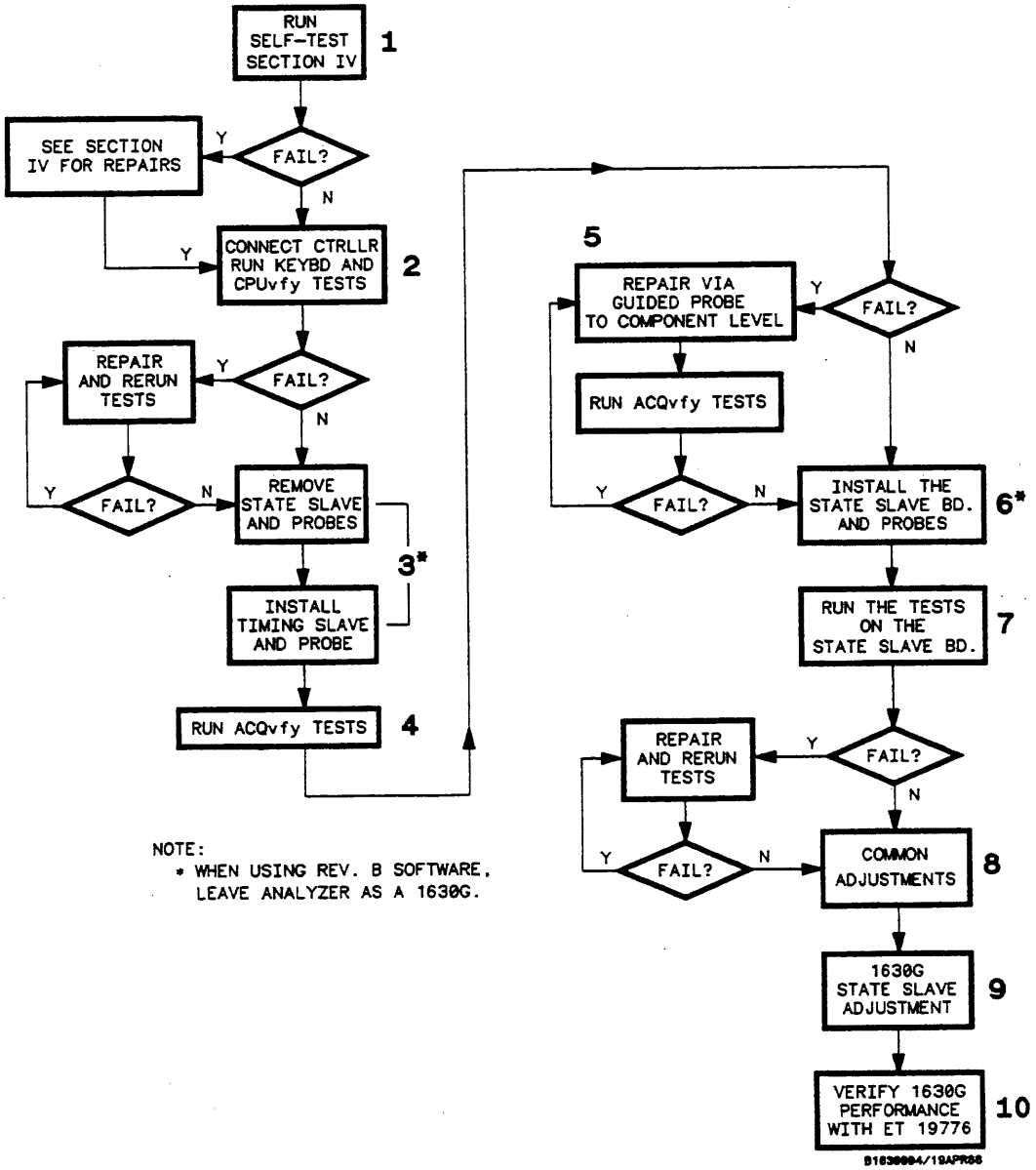


Figure A-1. 1630G Troubleshooting Flow Chart.

Summary Description

1. RUN SELF-TEST — This is described in Section IV, paragraph 4-3.

2. CONNECT CONTROLLER... — This is described in paragraph A-7 and A-8.

3. REMOVE STATE SLAVE-INSTALL TIMING SLAVE... — Convert the instrument to a 1630D (paragraph A-8). Assembly removal and installation instructions are in Section VIII. (**NOTE:** If using Rev. B software, it isn't necessary to convert the instrument; leave it as a 1630G.)

4. RUN < ACQvfy > TESTS — Paragraphs A-8 and A-9 and the software cover these tests.

5. Guided Probe — Paragraph A-10 and the software cover these tests.

6. Reconvert instrument — Convert instrument from 1630D back to a 1630G. Assembly removal and installation instructions are in Section VIII. (**NOTE:** When using Rev. B software it can be left as a 1630G.)

7. State Slave Tests — Run verification tests (paragraph A-16).

8. COMMON ADJUSTMENTS — Make the adjustments common to all family models (paragraph A-13).

9. STATE SLAVE ADJUSTMENT — Make the State Slave adjustment (paragraph A-16).

10. PERFORMANCE CHECKS — The performance checks for the State and Timing subsystems are covered in software using the ET19776 1630A/D Test Tool (paragraph A-18).

A-5. PROGRAM DISK LOADING PROCEDURE

After referring to the desired hardware configuration procedure (Operation, Guided Probe, or calibration), use the following procedure to load and run tests from the controller.

There are two versions of the test software, Rev. A and Rev. B. The tests in both versions are basically the same. Rev. B software fixes some bugs from Rev. A and has been reorganized to make it easier to use.

Most procedural differences concerning the two versions are covered as they occur. Several other things are noteworthy however. Rev. A will run on only Basic 2.0 and Rev. B will run on only Basic 5.0. Rev. B can be used on the Hewlett-Packard series 300 controllers as well as those mentioned.

a. Turn OFF the logic analyzer under test.

b. Set the logic analyzer rear panel address switches (1-8) to "00000001".

c. Turn ON the logic analyzer. The System Specification menu should be displayed.

d. Insert the BASIC 2.0 boot disk (Basic 5.0 when using Rev. B software) into the controller and turn it ON. (NOTE: BASIC EXT. 2.1 is not needed.)

e. Insert 1630/31 Program Disk I (any program disk when using Rev. B software) and type LOAD "Autost".

f. Press EXECUTE and then press RUN.

g. The softkeys in one of the following tables should appear on the controller (Main menu softkeys with Rev. B test software). If they don't, repeat the procedure.

h. Select the desired test and follow the instructions on the screen.

REV A SOFTWARE

SOFTKEY	TEST	TEST USE
< ACQvfy > *	Acquisition subsystem	Operation Verification
< CPUvfy >	CPU subsystem	Operation Verification
< Keybd >	Keyboard test pattern	Operation Verification
< GPROBE > **	Guided Probe	Troubleshooting
< Disply >	Display test pattern	Adjustment
< Strobe >	State board strobe	Adjustment

* If the <ACQvfy> tests are run ofter specifying "stop on failures" the user will be directed to the Guided Board routine. This routine is no longer supported; therefore do not specify "stop on failures" within <ACQvfy>.

** If < GPROBE > is chosen, refer to Guided Probe - Hardware Configuration, para. A-11.

REV B SOFTWARE

MAIN MENU	TEST MENU	TEST DESCRIPTION
< Func >	< Keybd >	Keyboard Tests
	< CPUvfy >	CPU Board Verification
	< ACQvfy >	Acquisition Verification
	< Gprobe >	Guided Probe Diagnostics
	< Func31 >	1631 Analog Functional Tests
	< Gvfy >	State Slave Board Tests
< Adj >	< Display>	Display Adjustment Program
	< Adj1631>	1631 Analog Adjustments
	< ETCAL >	ET19776 Calibration Routine
	< Strobe >	State Master Adjustments
< PV >	< ET >	PV Using ET19776 Tester
	< Analog >	1631 Analog Board Procedure
< Misc > (unsupported software)	< CPU Tests>	Runs CPU kernal test, reset test, and Kernal and bus test
	< GBOARD >	Guided Board Program
	< PARAM31>	PARAM31 Verification Test

A-6. OPERATION VERIFICATION

A-7. Hardware Configuration

This section concerns the hardware configuration necessary to execute Operation Verification tests. Reconfiguration of the instrument under test depends on the version of test software being used.

If Rev. A test software is being used, and the instrument is a 1630A, 1630G, or 1631A, it must be reconfigured to the "D" model using the Timing Slave board and probe provided in the Product Support Package. If Rev. B test software is being used, a 1630G can be left as it is. Just convert an "A" model to a "D" model. The hardware required is as follows:

a. One HP 9826 or 9836.

b. One 1630/31A/D or 1630G logic analyzer (unit under test).

c. For testing 1630/31A (and 1630G with Rev. A software) only:
   Timing Slave board (from Product Support Package).
   Timing Probe (from Product Support Package).

The hardware configuration is as follows:

a. Connect the HP-IB cable from the controller to the logic analyzer.

b. Analyzers needing reconfiguration will be modified for much of the testing, however this is not done until part way through the tests.

c. Follow the Program Disk Loading Procedure.

A-8. Running the Tests

After loading the Program Disk, use the following steps to run tests and determine if the subsystems are operating properly. If a test should fail, use Guided Probe to find the faulty node.

1. < Keybd > — This test displays a keyboard test pattern on the logic analyzer display. Key functions are checked for operation.

2. < CPUvfy > — This test determines if the CPU board is faulty. For this test, install an HP-IL cable in a loop from the HP-IL input to the HP-IL output.

3. Reconfigure Instrument — Reconfigure a 1630A to a 1630D and a 1631A to a 1631D. If Rev. A test software is being used, reconfigure a 1630G to a 1630D. Use the removal and installation instructions in Section VIII. The unit under test is kept reconfigured through completion of any necessary Guided Probe tests.

   a. The Timing Slave board and probe from the Product Support Package are added to a 1630A and 1631A.

   b. When using Rev. A software to test a 1630G, the State Slave board and probes are removed and replaced by the Timing Slave board and probe from the Product Support Package.

4. < ACQvfy > This test determines if the acquisition portion of the logic analyzer is faulty.

a. For this test connect Pod 0-Bit 0 to the PORT BNC on the rear of the instrument, and the Pod 0-Ground to the PORT BNC ground.

b. To assist in determining the actual board that failed, the following list summarizes the functional areas tested by each of the 9 <ACQvfy> tests.

Test #1: tests state pattern RAM and sequence timing pattern detectors for state mode.
Test #2: state master board functional test, also tests timing board main storage RAM.
Test #3: tests state occurence counter.
Test #4: tests J, K, and L, clock circuitry on state board.
Test #5: tests measurement complete shutdown on state board.
Test #6: main timing functional test, also tests state and timing interaction and the BNCs.
Test #7: tests timing delay counter.
Test #8: tests measurement complete shutdown on timing boards.
Test #9: tests asynchronous pattern filter on timing master board; this test will also fail if the oscillator circuitry or timing clock selector circuitry is not working.

c. Each of the first eight <ACQvfy> tests has a corresponding Guided Probe test. For example, if <ACQvfy> tests 3, 4, and 5 fail, the fault should be isolated to the State Master board. Then execute Guided Probe tests 3, 4, and 5 for the State Master board.

A-9. Acquisition Verification; Test #9, Failures

Test 9 of the Acquisition Verification checks the Trigger Duration circuitry on the Timing Master board. To troubleshoot this section of circuitry, first ensure that the logic analyzer passes Acquisition Verification tests 1 to 8.

When Test 9 fails, an 8-bit failure code is displayed. By interpreting this failure code, the failure area of the trigger duration circuit may be isolated. The bits of this code correspond as follows:

BIT	TEST
00000001	1 us
00000010	10 us
00000100	20 us
00001000	50 us
00010000	100 us
00100000	200 us

The following resistor and capacitor combinations on the Timing Master board are used for these tests.

TEST	RESISTOR(S)	CAPACITOR(S)
1us	R3 (1.58K)	C9 (300pF), C7 (3600pF)
10us	R3 (1.58K)	C9 (300pF), C6 (.04uF)
20us	R3 (1.58K), R2 (1.71K), R1 (681)	C9 (300pF), C5 (.4uF)
50us	R3 (1.58K), R2 (1.71K)	C9 (300pF), C5 (.4uF)
100us	R3 (1.58K)	C9 (300pF), C5 (.4uF)
200us	R3 (1.58K), R2 (1.71K), R1 (681)	C9 (300pF), C4 (4uF)

NOTE: The 200 MHz oscillator on the Timing Master board is used as a time base for these tests. A failure code of 00111111 may be due to a failure of this oscillator.

Signatures can be taken for some of the digital ICs in this circuit. To generate stimulus for this signature analysis, use Guided Probe for the Timing Master board, Test #6. This will automatically set up the 5005B signature analyzer (See paragraph A-11 for installation of the 5005B). Take signatures at the following points without additional prompting from the software:

U5I:	pin 12	0097	U4C:	pin 2	8P7A
	pin 13	F2AA		pin 3	8P7A
	pin 14	FA32		pin 4	8P7A
	pin 15	P719		pin 9	8A4U
				pin 13	8P7A
U2D	pin 7	P719		pin 14	0000
	pin 14	6963		pin 15	0000

A-10. GUIDED PROBE

A-11. Hardware Configuration

Guided Probe Troubleshooting requires the following equipment in addition to that noted in the Operation Verification - Hardware Configuration, paragraph A-7. Guided Probe is done with the instrument reconfigured.

a. One HP 5005B Signature Multimeter.

b. Additional HP-IB cable (10833A) to connect HP 5005B to logic analyzer under test.

The hardware configuration is as follows:

a. Connect the additional HP-IB cable from the logic analyzer to the 5005B.

b. Connect HP 5005B timing pod to the test points on the rear of the CPU board as follows: START/ST/SP to TP3, STOP/QUAL and ground to the GND, and CLOCK to TP1.

c. Set HP 5005B HP-IB address switches for "ADDRESSABLE" and select a unique address on the HP-IB bus.

d. Refer to the Program Disk Loading Procedure.

A-12. Running the Tests

After selecting the < GPROBE > softkey the controller will execute the Guided Probe program. The program will then direct the user through a troubleshooting procedure.

a. Press < GPROBE > softkey on the controller. Remember, always read the entire screen before proceeding.

b. The user is then asked which board to troubleshoot by referencing the part number of the board. Select the board suspected to be at fault. (Board isolation is done via the results of <ACQvfy> and/or via a board swap.)

c. The program will direct the user to select a particular test. Select the ACQvfy tests that failed. The software will re-run this test and then allow the user to proceed to <PROBE> or <RETRY> the test. If the user wishes to exit at this point, it is necessary to press SHIFT then RESET. Then the user must type LOAD "Autost" and press EXECUTE, then RUN.

d. If the testing leads to a "special case node", then refer to Appendix B in this manual. Remember, always read the entire screen.

e. Based on results of Guided Probe, repair the board. Re-run <ACQvfy> tests to verify repairs.

f. If the instrument is other than a 1630D, convert it back to it's original model.

   1. For the 1630A and 1631A, remove the Timing Slave board and probe and return them to the Product Support Package.

   2. For the 1631A and 1631D, reinstall the Analog board.

   3. For a 1630G, reinstall the State Slave board and probes.

A-13. COMMON ADJUSTMENTS

The following adjustments are those that are common to every member of the 163X family. The Timing Slave board (1630/31D only) has no additional adjustments. Additional adjustments specifically for the State Slave board (1630G) are covered by procedures in paragraph A-16. Additional adjustments specifically for the Analog board (1631A/D) are covered by procedures in paragraph A-17.

A-14. Hardware Configuration

Following is the hardware necessary to do the adjustments common to all members of the 163X family. For additional required test equipment for each adjustment, see Section V.

a. One HP 9826 or 9836.

b. One 1630A/D/G or 1631A/D logic analyzer (unit under test).

Configure the hardware as follows:

a. Connect an HP-IB cable from the controller to the logic analyzer.

b. Follow the Program Disk Loading Procedure.

A-15. Adjustments

After loading the Program Disk the adjustments below should be done as directed in Section V (Adjustments) of this manual.

Power Supply	The Power supply is adjusted without need for the programming.
CPU	The CPU is adjusted without need for the programming.
< Disply >	The programming loads a display test pattern on the logic analyzer for adjusting the Display Driver board.
< Strobe >	The programming sets up signals that strobe the State Master board for adjusting pulse width and delay.
Timing Master	In earlier instruments the Timing Master board has an adjustment for the 200 MHz oscillator. No programming is used for this adjustment.

A-16. 1630G, STATE SLAVE BOARD TEST AND ADJUSTMENT

The following deals with the testing of the State Slave board in the 1630G. After completing the Keyboard, CPU, and Acquisition tests with the 1630G set up as a 1630D, the instrument is converted back to a 1630G and the State Slave board and probes are tested with the following procedure.

a. Make sure the instrument is configured as a 1630G. (State Slave board and pods installed.)

b. Turn the 1630G ON. The System Specification menu should be displayed.

c. Insert the Basic 2.0 boot disk (Basic 2.1 is not needed) into the controller and turn it ON. If using Rev. B test software, boot Basic 5.0.

d. If using Rev A test software, insert the 1630/31 Program Disk II and type in LOAD"Gvfy ".

   If using Rev. B test software, insert any Program Disk and execute LOAD"Autost". From the Main menu, press < FUNC > softkey. From the FUNCtional menu, press < Gvfy >.

e. The program will now test the State Slave board. If a failure is isolated it will be noted on the screen of the controller. Be sure to read the entire screen for prompts and such.

f. Once the 1630G has passed the tests, perform the Common Adjustments procedure in paragraph A-13.

g. Perform the State Slave Board Adjustment in Section V, paragraph 5-8.

A-17. 1631A/D, ANALOG BOARD ADJUSTMENT AND FUNCTION CHECKS

This section deals with the proper execution of the 1631A/D functional test software. This routine will automatically locate problem areas on the 1631 Analog circuit board. Pass/Fail history is routed to the screen of the controller. In order to route results to the printer it is necessary to have the printer set to address 701.

a. Refer to the Disk Loading Procedure and load the 1631A/D Program Disk.

b. Type LOAD"ADJ1631" and then press EXECUTE then RUN.

   If using Rev. B test software, insert any Program Disk and execute LOAD"Autost". From the Main menu, press < Adj > softkey. From the Adjustment menu, press < Adj1631 >.

c. Perform the <DAC ZERO> and <SKEW> adjustment procedures in Section V, paragraph 5-9.

d. For Rev. A software, type LOAD"FUNC31" then press EXECUTE and RUN to perform 1631 analog board functional tests.

   For Rev. B software, return to the Main menu and press the < FUNC > softkey. From the FUNCtional menu press < FUNC31 >.

e. The user is now directed through the remainder of the routine.

NOTE: The 1631A/D Analog Board is on the Blue-Stripe Exchange Program.

A-18. 1630A/D/G, 1631A/D PERFORMANCE CHECKS

Performance tests on the state and timing systems of the 1630/31 family are done with the ET19776, 1630A/D Test Tool. The ET19776 tests should be performed whenever an instrument is serviced. Performance verification of the analog acquisition system (digitizing oscilloscope) is optional and should be performed if a problem is suspected in the analog system, or upon customer request. See Appendix C for the 1631A/D Analog Acquisition Performance Tests.

Appendix B Table of Contents

Paragraph		Page
B-1.	Introduction	B-1
B-2.	Special Case Testing for State Master Boards	B-1
B-3.	Special Case Nodes In All Tests	B-1
B-4.	Special Case Nodes In All Tests Except #4 and #5	B-2
B-5.	Special Case Nodes Only In Test #4	B-2
B-6.	Special Case Nodes Only In Test #5	B-3
B-7.	Special Case Testing for Timing Master Boards	B-3
B-8.	Special Case Testing for Timing Master Board 01630-66506	B-3
B-9.	Special Case Nodes In All Tests	B-4
B-10.	Special Case Nodes Only In Test #5	B-4

NOTES

APPENDIX B
1630A/D/G, 1631A/D
SPECIAL CASE NODE TESTING

B-1. INTRODUCTION

This special case testing is for nodes that do not fit into the normal flow of guided probe testing. The operator of Guided Probe is prompted to make special measurements, while the tests are in progress in order to verify proper operation of the instrument under test.

When using Rev. B test software, the user will be prompted from the screen with tests and test limits. This section is a useful reference, however in this case it is redundant.

B-2. SPECIAL CASE TESTING FOR STATE MASTER BOARDS

Testing of the State Master board uses disks supplied in the 1630/31 Product Support Package. Use the disk which covers the part number of the State Master board being tested.

The following Special Case Nodes should be measured manually when prompted by the controller during a guided probe session.

Reply to the controller with PASS if the signal appears as described below.

B-3. Special Case Nodes In All Tests

Use an oscilloscope (see table 1-3 for recommended test equipment) to view narrow (≤10 ns) pulses and small swings. A Small swing is about 200 mV each direction above and below Vbb (-1.3V).

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U3M: pin 5	Small swings @ -1.3V	SCOPE
pin 6	Small swings @ -1.3V	SCOPE
pin 9	-1.3V DC Voltage	DVM (5005B)
pin 14,15	Narrow pulse in ALL tests	SCOPE
U5L: pin 2	Narrow pulse in ALL tests	SCOPE
pin 5	Narrow pulse in ALL tests	SCOPE
U5M: pin 5	Small swings @ -1.3V	SCOPE
pin 11	-1.3 DC Voltage	DVM (5005B)
pin 12	Narrow ramp in ALL tests	SCOPE
pin 13	Small swings @ -1.3V	SCOPE
pin 15	Narrow pulse in ALL tests	SCOPE
U5N: pin 9	Narrow pulse in ALL tests	SCOPE
U6J: pin 2,3	Narrow pulse in ALL tests	SCOPE

B-4. Special Case Nodes In All Tests Except #4 and #5

Use an HP 5005B Signature Analyzer to measure the following NON-ECL signatures.

Manually, set the HP 5005B Data HI and LO thresholds to -1.5 V.

Pins on U1A-F,H-J	TEST					
	1	2	3	6	7	8
4, 9, 12	C05A	H825	C1UA	8P7A	056A	CC34
5, 10, 13	0000	C4H3	0000	0000	0000	0000

B-5. Special Case Nodes Only In Test #4

Use an HP 5005B Signature Analyzer to measure the following NON-ECL signatures.

Manually, set the HP 5005B Data HI and LO thresholds to -1.5 V.

IC	PINS	SIG.	IC	PINS	SIG.	IC	PINS	SIG.
U1A-C	4, 9,12	H68C	U1D-F	4, 9,12	8HAU	U1H-J	4, 9,12	UAC6
U6N	4		U6N	9		U6N	12	
U1A-C	5,10,13	47UC	U1D-F	5,10,13	1FHU	U1H-J	5,10,13	6CF6
U6N	5		U6N	10		U6N	13	

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U2B,C: pin 2,3, 14,15	unstable in Test #4	NO SOLUTION
U2E-I: pin 2,3, 14,15	unstable in Test #4	NO SOLUTION
U3A-I: pin 2,3, 22,23	unstable in Test #4	NO SOLUTION

B-6. Special Case Nodes Only In Test #5

Use an HP 5005B Signature Analyzer to measure the following NON-ECL signatures.

Manually, set the HP 5005B Data HI and LO thresholds to -1.5 V.

Pins on U1A-F,H-J	Signature
4, 9, 12	1308
5, 10, 13	0000

In Test #5 the following nodes will provide valid signatures, but in order for the node signal to be TOTALLY correct, narrow (≤10ns) pulses should exist at each node. If one of these nodes occurs in a guided probe printout, verify the TOTAL accuracy of the node by viewing the pulses with an oscilloscope.

U2L: pin 2
U3M: pin 3
U4K: pins 2,14,15
U5K: pins 3,6,14
U5M: pins 3,6
U5N: pins 2,3,14,15
U6K: pins 2,9,14
U7J: pins 14,15
U7K: pin 2
U7I: pins 2,3
U8J: pins 5,6,9,11,14,15
U8K: pins 2,3,4,12,13,14
U8L: pin 1,2,15

B-7. SPECIAL CASE TESTING FOR TIMING MASTER BOARDS

Testing on the Timing Master board uses data disks supplied in the 1630/31 Product Support Package. Use the disk which covers the part number of the Timing Master board that you are testing.

The following Special Case Nodes should be measured manually when prompted by the controller during a guided probe session. Use the oscilloscope (see table 1-3 for recommended test equipment) on the fastest sweep speed to view narrow (less than 10 ns) pulses. Reply to the controller with PASS if the signal appears as described below.

A Small swing is about 200 mV each direction above and below Vbb (-1.3V) and a Narrow pulse is approximately 10 ns.

B-8. Special Case Nodes Only For Timing Master Board 01630-66506

a. U8F/47 is listed as a special case node in the data base, but it is NOT. When asked for user input, probe the node and read the signature.

   If SIG = 4H94 the node passes.
   If SIG ≠ 4H94 the node fails.

b. An error has been found in the 01630-66506 data base. U4G is not properly stored on the data base tape. When instructed to probe U4G/7, the operator should also manually probe U4G/6. The following are the stable signatures for each test:

TEST #	SIGNATURE AT U4G/7
1	151C
2	F4F2
3	PU59
4	1525
5	HU12
6	CF02
7	0H2P
8	48H2

B-9. Special Case Nodes In ALL Tests

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U8C: pin 3	200 MHz	SCOPE
pin 11	100 MHz	"
pin 12	40 MHz	"
pin 13	20 MHz	"
pin 14	10 MHz	"
U8D: pin 3	100 MHz	SCOPE
pin 4	200 MHz	"
pin 11	50 MHz	"
pin 12	20 MHz	"
pin 13	10 MHz	"
U4E: pin 10	-1.3V	DVM
pin 11	-1.3V	"
U2D: pin 5	-1.3V	DVM
pin 11	-1.3V	"
pin 12	-1.3V	"
pin 10	small swings	SCOPE

B-10. Special Case Nodes ONLY In Test #5

The following nodes will provide valid signatures, but in order for the node signal to be TOTALLY correct these narrow pulses must exist. Therefore, if one of these nodes occurs in a Guided Probe printout, verify the TOTAL accuracy of the node with a SCOPE by viewing the pulses.

SPECIAL CASE NODES	SHOULD BE	MEASURE WITH
U8C: pin 3	200 MHz	SCOPE
P1: pin 22	Narrow pulses ≤10nS	"
pin 26	"	"
U9H: pin 3	"	"
pin 14	"	"
pin 15	"	"
U3E: pin 3	"	"
U5I: pin 3	"	"

Appendix C Table of Contents

Paragraph		Page
C-1.	Introduction	C-1
C-2.	Equipment Required	C-1
C-3.	Test Record	C-1
C-4.	Menu Map	C-3
C-5.	Voltage Measurement Accuracy Test	C-4
C-6.	Bandwidth (-3dB) Test	C-6
C-7.	Transition Time Test	C-9
C-8.	Time Base Accuracy Test	C-12
C-9.	Trigger Sensitivity Test	C-14

List of Illustrations

Figure		Page
C-1.	1631A/D Analog Menu Map	C-3

List of Tables

Table		Page
C-1.	Recommended Test Equipment	C-2
C-2.	HP 1631A/D Analog Performance Test Record	C-16

NOTES

APPENDIX C
HP 1631A/D
ANALOG ACQUISITION PERFORMANCE TESTS

C-1. INTRODUCTION

This section describes the Analog Acquisition Performance Tests for the HP 1631A/D. The performance tests verify the analog specifications given in table 1-1 of the HP 1630A/D/G, 1631A/D Service Manual.

Rev. B test software for the 1630/31 family contains a guided program for the tests in this section. To run this program, after loading "Autost", press < PV > in the Main menu, then press < Analog >. The program can provide hardcopy documentation of test results, depending on the choices and entries made while running the program.

C-2. EQUIPMENT REQUIRED

The equipment required to to perform the performance tests is given in table 1. Other equipment may be substituted if it meets or exceeds the critical specifications given in the table.

C-3. TEST RECORD

Results of performance tests may be tabulated on the Performance Test Record (table 2) at the end of this section. The Test Record lists all of the tested specifications and their acceptable limits. The results recorded in incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

NOTE

Allow the instrument to warm up for at least 30 minutes prior to beginning the performance tests.

Table 1. Recommended Test Equipment.

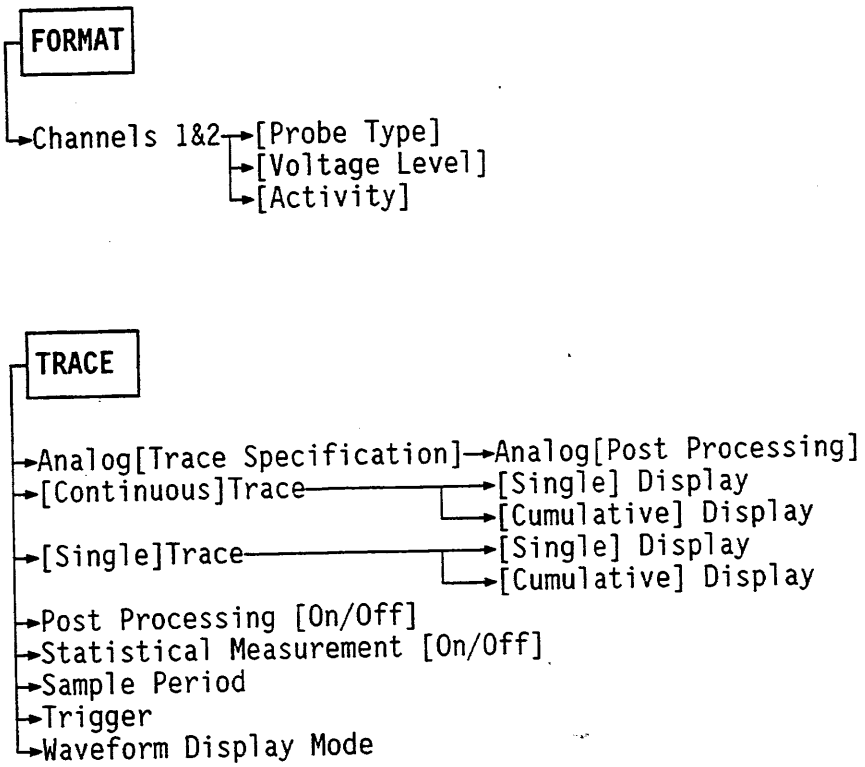
INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	Transition time: ≤1 ns Repetition rate: 1MHz 0-2 Volt Output Offset Output	HP 8082A
Function Generator	Sine and Square Wave 10 KHz to 50 MHz Amplitude: 2 volts 0 to ±2 Volt Offset Output *	HP 8116A
RF Voltmeter	Accuracy: ±3% at 50 MHz	HP 3406A
Time Mark Generator	Time marks: 100 ns Accuracy: ≤1%	Tektronics TG 501
50Ω Sampling Tee	----------	HP Model 10221A
50Ω Terminaton (2)	Accuracy ≤1%	HP 10100C
Adapter (2)	GR874-to-BNC(f)	HP Part No. 1250-0850
Adapter	BNC(m)-to-BNC(m)	HP Part No. 1250-0216
BNC Cable	48-inch	HP 10503A

* If a substitute function generator does not have offset, a power supply and DVM can be used for the Voltage Measurement Accuracy tests (see paragraph C-5).

C-4. MENU MAP

The following Menu Map, part of the menu map found in the HP 1631A/D Operating and Programming Manual, may be used when doing these performance tests. The procedures, however, have been written so that it takes very little experience with the 1631A/D in order to do the tests.

ANALOG INPUTS



ANALOG OUTPUTS

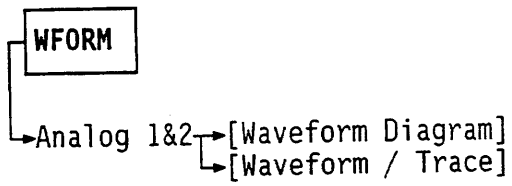


Figure 1. HP 1631A/D Analog Menu Map.

C-5. VOLTAGE MEASUREMENT ACCURACY TEST

Specification:

	Gain Accuracy	+	ADC Accuracy
=	(+/- 2.5% of full scale)	+	(+/- 1.6% of full scale)

Equipment Required:

Function Generator ..... HP Model 8116A
BNC Cable ..... HP 10503A
50Ω Terminator ..... HP Model 10100C

OR

DC Supply ..... HP Model 6214A
DVM ..... HP 3468A
BNC Cable ..... HP 10503A
BNC(f)-to-Dual Banana Adapter ..... HP Part No. 1251-2277

NOTE

You may use either the DC Offset of a function generator (such as the HP 8116A) or a power supply and DVM to do these tests. If using a function generator, be sure to turn off the waveform outputs before doing these tests, and turn off the offset before using the waveform outputs on later tests.

Procedure:

1. Cycle the power on the 1631 to return all menus to default conditions.

2. Press FORMAT, **Analog Format Specification**, and use the CURSOR, NEXT, and NUMERIC keys to set the following parameters on both channels.

```
Probe Type          [1X Probe ]
                  Full Scale:  2.50V
Voltage           [Specified Below]
   Upper Limit       [+] 2.500V
   Lower Limit       [+] 0.000V
```

3. Press WFORM, NEXT keys on the 1631 to obtain the **Analog** [Waveform Diagram] menu. Change the [Time] field to [Volts] [1].

4. Set the DC supply level to +500mV (verify with DVM).

5. Connect a BNC cable from the DC supply to INPUT 1 of the 1631. If you are using the offset output of the 8116A, in order to get the output shown on the 8116A display, you must terminate the cable with a 50 ohm load.

6. Press RUN then STOP keys on the 1631.

7. Using the cursor keys, move the X cursor along the waveform to determine the max and min voltages. The limits should be 400 mV and 600 mV.

8. Change [Volts] [1] to [Volts] [2]. Connect the BNC cable to INPUT 2, press RUN and STOP. Use the X cursor to verify readings between 600 mV and 400 mV.

9. Set the DC supply to -500 mV (verify with DVM).

10. Press FORMAT and change the channel 1 and channel 2 voltage limits to [+] 0.000V (upper limit) and [-] 2.500V (lower limit).

11. Press RUN and STOP. Use the X cursor to verify channel 2 readings between -600 mV and -400 mV.

12. Change [Volts] [2] to [Volts] [1]. Connect the BNC cable to INPUT 1, press RUN and STOP. Use the X cursor to verify readings between -600 mV and -400 mV.

13. Change the DC supply to -2.0V (verify with DVM).

14. Press FORMAT. Change the channel 1 and channel 2 probe types to [10X Probe]. The voltage limits will automatically change to [+] 00.00V (upper limit) and [-] 25.00V (lower limit).

15. Press RUN and STOP. Use the X cursor to verify channel 1 voltage readings between -19.0v and -21.0V.

16. Change [Volts] [1] to [Volts] [2]. Connect the BNC cable to INPUT 2, press RUN and STOP. Use the X cursor to verify voltage readings between -19.00V and -21.00V.

17. Change the DC supply to +2.0V (verify with DVM).

18. Press FORMAT. Change the channel 1 and channel 2 voltage limits to [+] 25.00V (upper limit) and [-] 00.00V (lower limit).

19. Press RUN and STOP. Use the X cursor to verify channel 2 voltage readings between +19.0v and +21.0V.

20. Change [Volts] [2] to [Volts] [1]. Connect the BNC cable to INPUT 1, press RUN and STOP. Use the X cursor to verify voltage readings between +19.0V and +21.0V.

C-6. BANDWIDTH (-3dB) TEST

Specification: DC coupled DC to 50 MHz

Equipment required:

Function Generator ..... HP Model 8116A
RF Voltmeter ..... HP Model 3406A
50Ω Sampling Tee ..... HP Model 10221A
BNC Cable ..... HP 10503A
50Ω Termination ..... HP Model 10100C
GR874-to-BNC(f) Adapter (2) ..... HP Part No. 1250-0850
BNC(m)-to-BNC(m) Adapter ..... HP Part No. 1250-0216

Procedure:

1. Cycle the power on the 1631 to return all menus to default conditions.

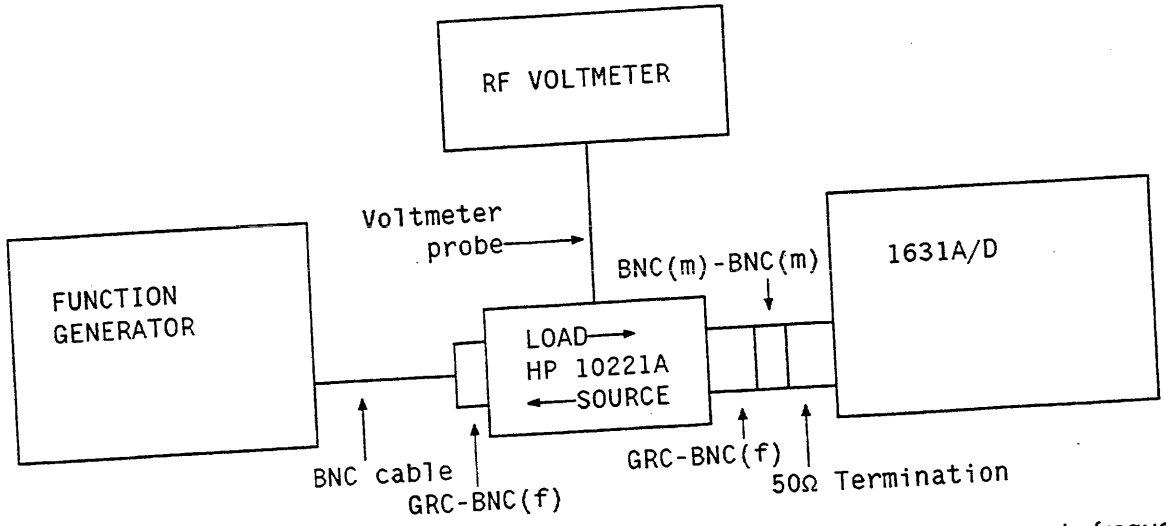
2. Press FORMAT, **Analog Format Specification**, and use the CURSOR, NEXT, and NUMERIC keys to set the following parameters on both channels.

```
Probe Type              [1X Probe ]
                   Full Scale:  2.50V
Voltage             [Specified Below]
   Upper Limit          [+] 1.200V
   Lower Limit          [-] 1.200V
```

3. Press TRACE and set up the **Analog Trace Specification** menu as shown below.

```
[  Single  ] Trace Mode
[Cumulative] Display Mode

Post Processing          [Off]
Statistical Measurements  Off

Sample Period [  1 µs]  Acquisition Time: 1.000 ms


[Start ] Trace 0000 [ns] After Trigger

   Trigger       [      ]
   Edge           [ Rising ]
   Trigger Level  [+] 0.200V

Waveform Display Mode: [Straight Line]
```

4. Configure the system as shown below. Connect the output of the Sampling Tee to INPUT 1 of the 1631.



5. Configure the function generator as follows: sinewave amplitude of 2V peak-to-peak, frequency of 10 kHz, and offset of 0V.

6. Record the reading on the RF Voltmeter (approx. 0.707V RMS).

7. Press RUN on the 1631. The display will show the **Analog** [Waveform / Trace].

8. Move the cursor to the channel [2] field and press the blue SHIFT then DELETE keys to remove channel 2 from the display. (When doing this step for channel 2, move the cursor to the [1] field and press NEXT to display channel 2.)

9. Move the cursor to the top of the display. Press NEXT for **Analog** [Waveform Diagram]. If doing channel 1, Change the [Time] field to [Volts] [1].

10 Measure and record the voltage peak to peak using the X and O cursors.

11. Change the frequency of the function generator to 50 MHz.

12. Adjust the amplitude of the function generator so the reading on the RF Voltmeter is the same as the value recorded in step 6.

13. With the cursor at the top of the display, Press NEXT to get **Analog** [Waveform / Trace]. Change the sample period to [5 ns] and the **Trace Mode** to [Continuous].

14. Go back to the **Analog** [Waveform Diagram] menu, increase the magnification to 40X.

15. Press the RUN key on the 1631, take 25 runs, and press the STOP key. (Press the STOP key when 24 runs shows.)

16. On the display of the 1631, count the number of minor divisions from the highest peak of the accumulated data to the lowest peak and multiply by (.12). This will give the voltage peak to peak of the accumulated data. (This method is used because the cursors will not measure accumulated data.) Divide this value by (.707). The result should be greater than or equal to the value recorded in step 10.

C-7. TRANSITION TIME TEST

Specification: ≤ 6 ns (20% to 80%)

Equipment Required:

Pulse generator ..... HP Model 8082A
BNC Cable ..... HP 10503A
50Ω termination (2) ..... HP Model 10100C

Equipment Setup: 8082A

Pulse period:	1 μsec
Pulse width:	square wave
Transition time:	1 ns
Offset:	on (adjusted below)
Amplitude:	2.0 V
Outputs:	POS/NORM
Ext input level:	NORM
All verniers:	Full CCW, except offset and amplitude.

Procedure:

1. Cycle the power on the 1631 to return all menus to default conditions.

2. Press FORMAT, **Analog Format Specification**, and use the CURSOR, NEXT, and NUMERIC keys to set the following parameters on both channels.

```
Probe Type              [1X Probe ]
                   Full Scale:  2.50V
Voltage             [Specified Below]
   Upper Limit          [+] 2.200V
   Lower Limit          [-] 0.300V
```

3. Press TRACE and set up the **Analog Trace Specification** menu as shown below.

```
[Continuous ] Trace Mode
[  Single   ] Display Mode

Post Processing          [Off]
Statistical Measurements  Off

Sample Period [  5 ns]  Acquisition Time: 5.000 μs


[Start ] Trace 0000 [ns] After Trigger

   Trigger       [      ]
   Edge           [ Rising ]
   Trigger Level  [+] 0.500V

Waveform Display Mode: [  Filtered  ]
```

4. Connect a BNC cable with a 50Ω terminator, from the left-hand output connector on the 8082A to INPUT 1 on the 1631. Connect the other terminator to the other output of the 8082A.

5. Press the RUN and NEXT keys on the 1631.

6. From the **Analog** [Waveform Diagram] menu, change [Time] to [Volts] [1].

7. Place the X cursor in the center of the bottom of the square wave, and place the 0 cursor in the center of the top of the square wave.

8. Adjust the Offset Vernier on the 8082A so that the voltage at X reads as close as possible to 0.0 V.

9. Adjust the Amplitude Vernier on the 8082A so that the voltage at the O cursor reads as close as possible to 2.0 V.

10. Press the STOP key on the 1631.

11. Press TRACE. In the **Analog Trace Specification** menu, turn on **Post Processing** and **Statistical Measurements**.

12. Move the cursor to the top of the menu and press NEXT. Configure the **Analog** [Post Processing] menu as shown below.

    On Acquired Data Place Cursors

    x [On] [First Occurance]
    of [+] 0.400V
    of [Rising] Edge
    of [1]
    [After Start]

    o [On] [First Occurance]
    of [+] 1.600V
    of [Rising] Edge
    of [1]
    after x

    Stop Continuous Runs [When] [Runs] Equals 0040

13. Press the RUN key. This test takes about one minute.

14. After the 40 runs are complete, the **Mean x to o** should be less than or equal to 6.0 ns.

15. Connect the signal source to INPUT 2.

16. Press TRACE for the **Analog** [Post Processing] menu. Change both x and o cursor placements to channel 2.

17. Move the cursor to the top of the display. Press NEXT to get the **Analog [Trace Specification]** menu. Change as follows:

```
Trigger          [    2     ]
Edge             [ Rising ]
Trigger Level    [+] 0.500V
```

18. Press the RUN key.

19. After the 40 runs are complete, the **Mean x to o** should be less than or equal to 6.0 ns.

C-8. TIME BASE ACCURACY TEST

Specification: single-shot +/- 1.5 ns for 5 ns sample period
+/- 1 sample period for sample periods of 10 ns or greater

continuous +/- .15 times sample period, based on 100 averages

Equipment required:

Time Mark Generator ..... Tektronics TG 501
BNC Cable ..... HP 10503A
50Ω termination ..... HP Model 10100C

Procedure:

1. Cycle the power on the 1631 to return all menus to default conditions.

2. Press FORMAT, **Analog Format Specification**, and use the CURSOR, NEXT, and NUMERIC keys to set the following parameters on channel 1.

```
Probe Type              [1X Probe ]
                   Full Scale:  2.50V
Voltage             [Specified Below]
   Upper Limit         [+] 2.300V
   Lower Limit         [-] 0.200V
```

3. Press TRACE and set up the **Analog Trace Specification** menu as shown below.

```
[Continuous ] Trace Mode
[  Single   ] Display Mode

Post Processing          [On ]
Statistical Measurements [On ]

Sample Period [  5 ns]  Acquisition Time: 5.000 µs


[Start ] Trace 0000 [ns] After Trigger

   Trigger       [     1     ]
   Edge           [ Rising ]
   Trigger Level  [+] 0.200V

Waveform Display Mode: [  Filtered  ]
```

4. Return the cursor to the top of the display and press NEXT. Configure the **Analog** [Post Processing] menu as shown below.

   On Acquired Data Place Cursors

   x
   [On] [First Occurance]
   of [+] 0.200V
   of [Rising] Edge
   of [1]
   [After Tracepoint]

   o
   [On] [First Occurance]
   of [+] 0.200V
   of [Rising] Edge
   of [1]
   after x

   Stop Continuous Runs [When] [Runs] Equals 0100

5. Return to the **Analog** [Trace Specification] menu. Change **Trace Mode** from [Continuous] to [Single].

6. Set the output of the Time Mark Generator to .1 μs.

7. Connect a BNC cable from the output of the Time Mark Generator to INPUT 1 of the 1631 through a 50Ω terminator.

8. Press the RUN key. Press NEXT to get the **Analog** [Waveform Diagram] menu. The time X to O should be between 98.5 ns and 101.5 ns.

9. Change the **Sample Period** to [20 ns].

10. Press the RUN key. The time X to O should be between 80 and 120 ns.

11. Press TRACE. In the **Analog** [Trace Specification] menu, change **Trace Mode** from [Single] to [Continuous].

12. Press WFORM. In the **Analog** [Waveform Diagram] menu, change the **Sample Period** to [5 ns] and change [Mean & Dev.] to [Max. & Min.].

13. Press RUN. This test takes about three minutes to complete. Upon completion, the **Max x to o** should be less than or equal to 101.5 ns, and the **Min x to o** should be greater than or equal to 98.5 ns.

C-9. TRIGGER SENSITIVITY TEST

Specification: Square wave up to 10 MHz, .2 of full-scale for ch. 1 & 2
50 mV p-to-p for external

Up to 50 MHz, .3 of full-scale for ch. 1 & 2
100 mV p-to-p for external

Equipment required:

Function Generator ..... HP Model 8116A
BNC Cable ..... HP 10503A
50Ω termination ..... HP Model 10100C

Procedure:

1. Cycle the power on the 1631 to return all menus to default conditions.

2. Press FORMAT, **Analog Format Specification**, and use the CURSOR, NEXT, and NUMERIC keys to set the following parameters on both channels.

```
Probe Type          [1X Probe ]
                 Full Scale:  2.50V
Voltage           [Specified Below]
   Upper Limit       [+] 1.250V
   Lower Limit       [-] 1.250V
```

3. Press TRACE and set up the trigger in the **Analog Trace Specification** menu as shown below.

```
Trigger          [    1     ]
Edge             [ Rising ]
Trigger Level    [+] 0.000V
```

4. Connect a BNC cable terminated with a 50Ω load to the signal 8116A output. Set up the signal generator as follows:

Frequency:	10 MHz (square wave)
Duty Cycle:	50%
Amplitude:	500 mV
Offset:	000 V

5. Connect the signal to INPUT 1 of the 1631 and Press RUN. The 1631 should trigger (**Continuous Trace In Process**). (*)

6. Press STOP. Connect the function generator signal to INPUT 2. Press TRACE and change **Trigger** [1] to **Trigger** [2].

7. Press RUN and the 1631 should trigger. Press STOP. (*)

8. Set the amplitude of the 8116A to 50.0 mV.

9. Connect the signal to the EXT TRIG input. Press TRACE and set the following trigger specifications.

```
Trigger          [External ]   External Probe Type [1X Probe ]
Edge             [ Rising ]
Trigger Level    [+] 0.000V
```

10. Press RUN, and the 1631 should trigger. (*)

11. Increase the frequency of the 8116A to 50 MHz and the amplitude to 100 mV.

12. Press RUN and the 1631 should trigger. Press STOP. (*)

13. Set the amplitude of the 8116A to 750 mV.

14. Press Trace and set the trigger source to channel 1. Connect the signal to INPUT 1.

15. Press RUN and the 1631 should trigger. Press STOP. (*)

16. Press Trace and set the trigger source to channel 2. Connect the signal to INPUT 2.

17. Press RUN and the 1631 should trigger. Press STOP. (*)

(*) *To find where the actual trigger sensitivity limit occurs, do not press STOP. Gradually decrease the amplitude of the signal generator until the 1631 stops triggering (***Waiting for Analog Trigger***). Read the output level of the signal generator to find the low trigger limit.*

Table 2. HP 1631A/D Analog Performance Test Record.

Instrument Serial No.:_____ **Date:**_____

TEST	LIMITS	RESULT		
VOLTAGE MEASUREMENT ACCURACY			VMIN	VMAX
	400mV to 600mV	CH.1	_____	_____
		CH.2	_____	_____
	-400mV to -600mV	CH.2	_____	_____
		CH.1	_____	_____
	-19V to -21V	CH.1	_____	_____
		CH.2	_____	_____
	+19V to +21V	CH.2	_____	_____
		CH.1	_____	_____
BANDWIDTH			PASS	FAIL
	50 MHz	CH.1	_____	_____
		CH.2	_____	_____
TRANSITION TIME	≤6 ns	CH.1	_____	
		CH.2	_____	
TIMEBASE ACCURACY	Single Shot			
	5 ns sample period			
	98.5 ns to 101.5 ns		_____	
	20 ns sample period			
	80 ns to 120 ns		_____	
	Continuous			
	Max x to o			
	≤ 101.5 ns		_____	
	Min x to o			
	≥ 98.5 ns		_____	
TRIGGER SENSITIVITY	10 MHz		PASS	FAIL
	CH1/CH2 .2 of full scale	CH.1	_____	_____
		CH.2	_____	_____
	EXTERNAL 50 mV p-to-p	EXT	_____	_____
	50 MHz			
	EXTERNAL 100 mV p-to-p	EXT	_____	_____
	CH1/CH2 .3 of full scale	CH.1	_____	_____
		CH.2	_____	_____

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